National Semiconductor

October 1999

54FCT574
Octal D-Type Flip-Flop with TRI-STATE® Outputs

General Description

The 'FCT574 is an octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The device is functionally identical to the 'FCT374 except for the pinouts.

Features

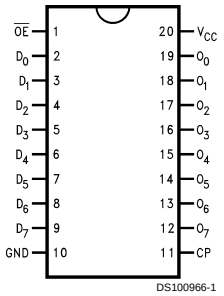
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors
- Functionally identical to 'FCT374
- TRI-STATE outputs for bus-oriented applications
- Output sink capability of 32 mA, source capability of 12 mA
- TTL input and output level compatible
- CMOS power consumption
- Standard Microcircuit Drawing (SMD) 5962-8951301

Ordering Code

Military	Package Number	Package Description
54FCT574DMQB	J20A	20-Lead Ceramic Dual-In-Line
54FCT574FMQB	W20A	20-Lead Cerpack
54FCT574LMQB	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

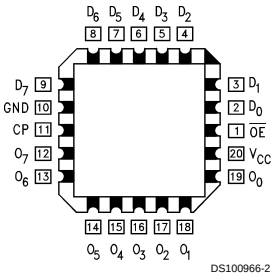
Connection Diagrams

Pin Assignment for DIP and Flatpak



DS100966-1

Pin Assignment for LCC



DS100966-2

Pin Descriptions

Pin Names	Description
D_0–D_7	Data Inputs
CP	Clock Pulse Input (Active Rising Edge)
$\overline{OE}$	TRI-STATE Output Enable Input (Active LOW)
O_0–O_7	TRI-STATE Outputs

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Functional Description

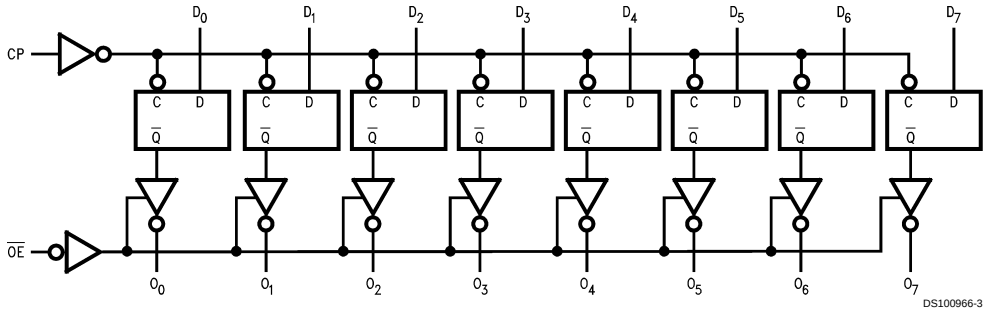
The 'FCT574 consists of eight edge-triggered flip-flops with individual D-type inputs and TRI-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs are in a high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H or L	L	NC	Z	Hold
H	H or L	H	NC	Z	Hold
H	N	L	L	Z	Load
H	N	H	H	Z	Load
L	N	L	L	L	Data Available
L	N	H	H	H	Data Available
L	H or L	L	NC	NC	No Change in Data
L	H or L	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
N = LOW-to-HIGH Transition
NC = No Change

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Storage Temperature	−65˚C to +150˚C
Ambient Temperature under Bias	−55˚C to +125˚C
Junction Temperature under Bias	
Ceramic	−55˚C to +175˚C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in	
the Disabled or Power-Off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55˚C to +125˚C
Supply Voltage	
Military	+4.5V to +5.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

DC Electrical Characteristics

Symbol	Parameter		FCT574 Min	FCT574 Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0		V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54FCT	4.3		V	Min	I_{OH} = −300 µA
		54FCT	2.4		V	Min	I_{OH} = −12 mA
V_{OL}	Output LOW Voltage	54FCT		0.2	V	Min	I_{OL} = 300 µA
		54FCT		0.5	V	Min	I_{OL} = 32mA
I_{IH}	Input HIGH Current			5 5	µA	Max	V_{IN} = 2.7V (Note 3) V_{IN} = V_{CC}
I_{IL}	Input LOW Current			−5 −5	µA	Max	V_{IN} = 0.5V (Note 3) V_{IN} = 0.0V
I_{OZH}	Output Leakage Current			10	µA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}$ = 2.0V
I_{OZL}	Output Leakage Current			−10	µA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}$ = 2.0V
I_{OS}	Output Short-Circuit Current		−60		mA	Max	V_{OUT} = 0.0V
I_{CCQ}	Power Supply Current			1.5	mA	Max	V_{IN} = 0.2V or V_{IN} = 5.3V, f_I = 0MHz
ΔI_{CC}	Power Supply Current			2.0	mA	Max	V_{IN} = 3.4V
I_{CCT}	Additional I_{CC}/Input			6.0	mA	Max	V_I = V_{CC} − 2.1V or V_{IN} = GND, f_{CP} = 10MHz, Outputs open, $\overline{OE}$ = GND, one bit toggling at f_I = 5MHz, 50% duty cycle
				5.5	mA	Max	V_I = 5.3V or V_{CC} = 0.2V, f_{CP} = 10MHz, Outputs open, $\overline{OE}$ = GND, one bit toggling at f_I = 5MHz, 50% duty cycle
I_{CCD}	Dynamic I_{CC}	No Load		0.40	mA/ MHz	Max	Outputs Open, $\overline{OE}$ = GND, One bit toggling, 50% duty cycle, V_{IN} = 5.3V or V_{IN} = 0.2V

Note 3: Guaranteed, but not tested.

AC Electrical Characteristics

Symbol	Parameter	54FCT T_A = −55°C to +125°C V_{CC} = 4.5V to 5.5V C_L = 50 pF Min	Max	Units	Fig. No.
t_{PLH}	Propagation Delay	2.0	11.0	ns	*Figure 4*
t_{PHL}	CP to O_n	2.0	11.0		
t_{PZH}	Output Enable Time	1.5	14.0	ns	*Figure 6*
t_{PZL}		1.5	14.0		
t_{PHZ}	Output Disable Time	1.5	8.0	ns	*Figure 6*
t_{PLZ}		1.5	8.0		

AC Operating Requirements

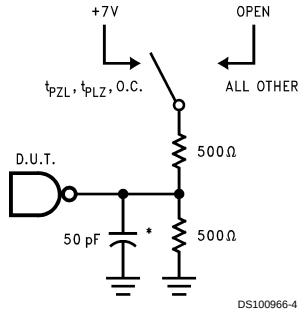
Symbol	Parameter	54FCT T_A = −55°C to +125°C V_{CC} = 4.5V to 5.5V C_L = 50 pF Min	Max	Units	Fig. No.
t_s(H)	Setup Time, HIGH	3.5		ns	*Figure 7*
t_s(L)	or LOW D_n to CP	3.5			
t_h(H)	Hold Time, HIGH	2.0		ns	*Figure 7*
t_h(L)	or LOW D_n to CP	2.0			
t_w(H)	Pulse Width, CP,	7.0		ns	*Figure 5*
t_w(L)	HIGH or LOW	7.0			

Capacitance

Symbol	Parameter	Typ	Units	Conditions T_A = 25°C
C_{IN}	Input Capacitance	5.0	pF	V_{CC} = 0V
C_{OUT} (Note 4)	Output Capacitance	9.0	pF	V_{CC} = 5.0V

Note 4: C_{OUT} is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

AC Loading



*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

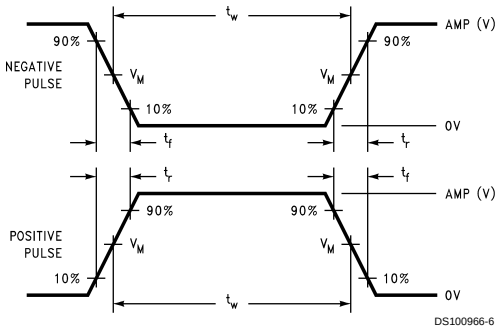


FIGURE 2. V_M = 1.5V

Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 3. Test Input Signal Requirements

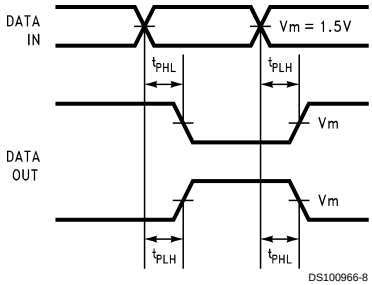


FIGURE 4. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

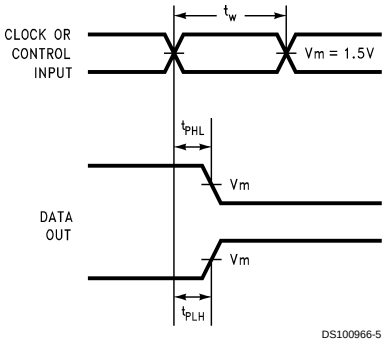


FIGURE 5. Propagation Delay, Pulse Width Waveforms

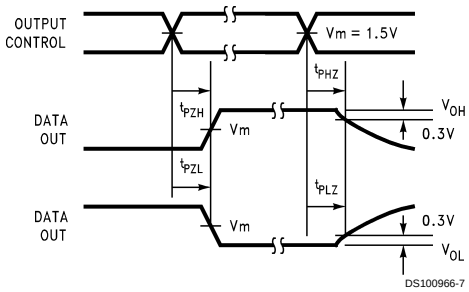


FIGURE 6. TRI-STATE Output HIGH and LOW Enable and Disable Times

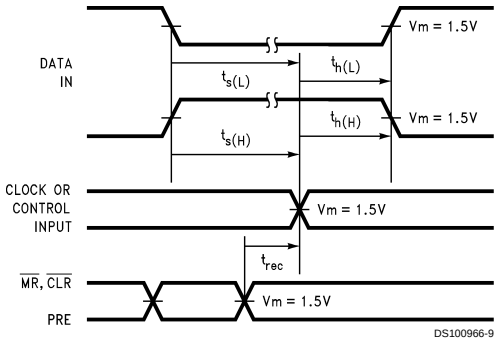
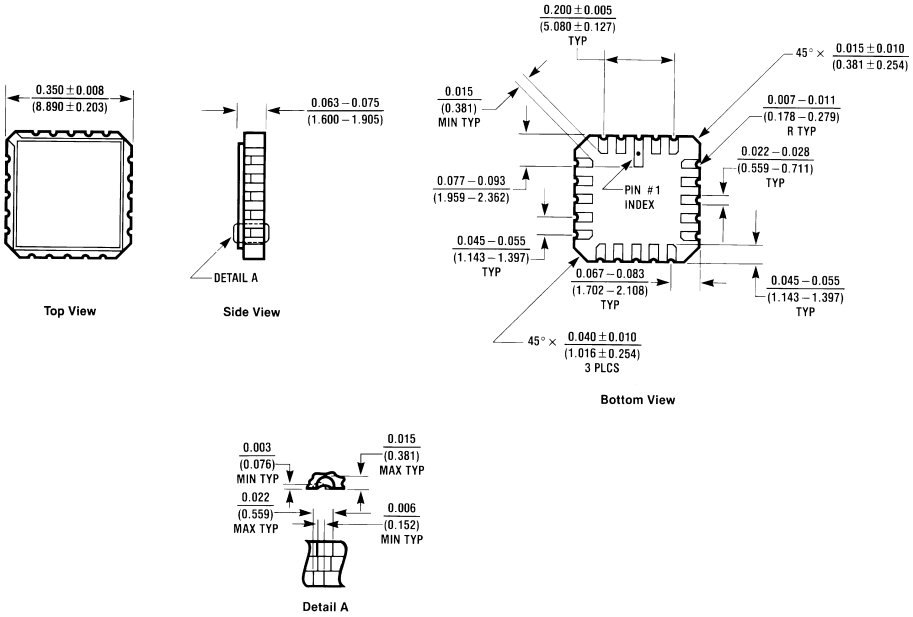
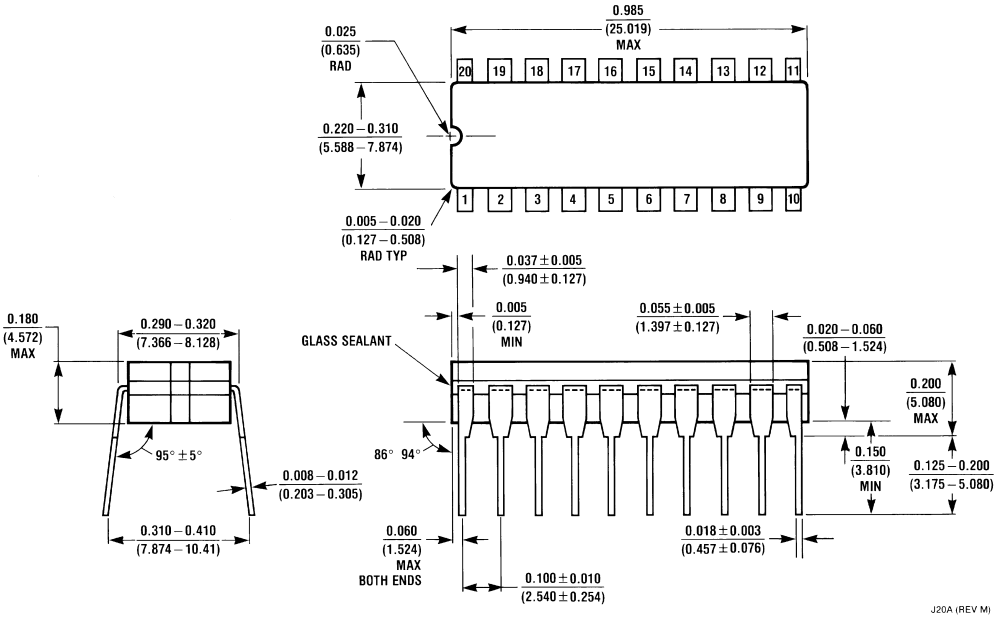


FIGURE 7. Setup Time, Hold Time and Recovery Time Waveforms

Physical Dimensions inches (millimeters) unless otherwise noted

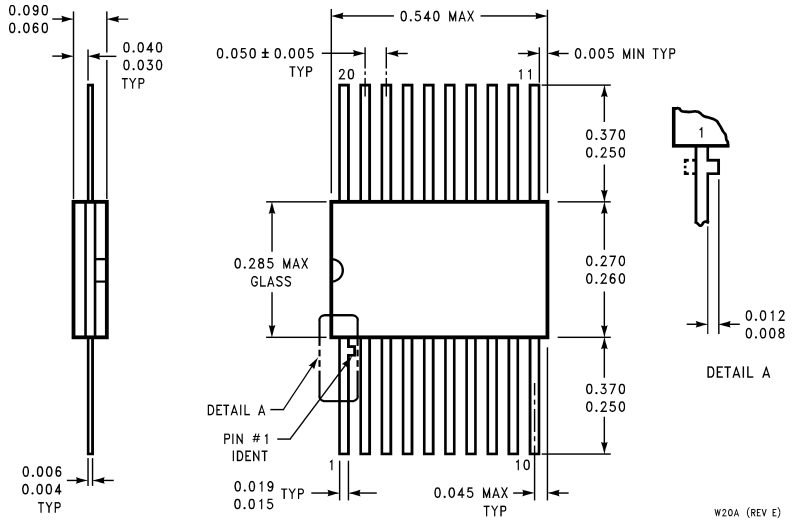


20-Terminal Ceramic Chip Carrier (L)
NS Package Number E20A



20-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J20A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



20-Lead Ceramic Flatpak (F)
NS Package Number W20A

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