

54F/74F161A • 54F/74F163A Synchronous Presettable Binary Counter

General Description

The 'F161A and 'F163A are high-speed synchronous modulo-16 binary counters. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multi-stage counters. The 'F161A has an asynchronous Master-Reset input that overrides all other inputs and forces the outputs LOW. The 'F163A has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock. The 'F161A and 'F163A are high-speed versions of the 'F161 and 'F163.

Features

- Synchronous counting and loading
- High-speed synchronous expansion
- Typical count frequency of 120 MHz
- Guaranteed 4000V minimum ESD protection

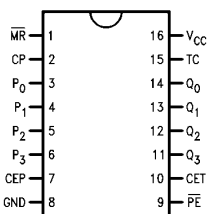
Commercial	Military	Package Number	Package Description
74F161APC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F161ADM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F161ASC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F161ASJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F161AFM (Note 2)	W16A	16-Lead Cerpack
	54F161ALM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74F163APC		N16E	16-Lead (0.300" Wide) Molded Dual-In-Line
	54F163ADM (Note 2)	J16A	16-Lead Ceramic Dual-In-Line
74F163ASC (Note 1)		M16A	16-Lead (0.150" Wide) Molded Small Outline, JEDEC
74F163ASJ (Note 1)		M16D	16-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54F163AFM (Note 2)	W16A	16-Lead Cerpack
	54F163ALM (Note 2)	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

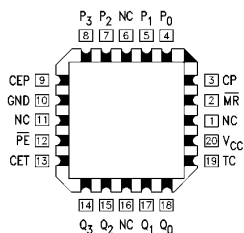
Connection Diagrams

Pin Assignment
for DIP, SOIC and Flatpak
'F161A



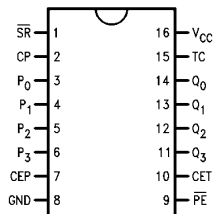
TL/F/9486-1

Pin Assignment
for LCC
'F161A



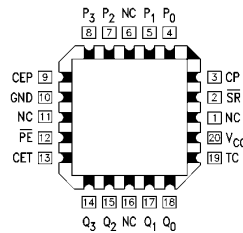
TL/F/9486-2

Pin Assignment
for DIP, SOIC and Flatpak
'F163A



TL/F/9486-7

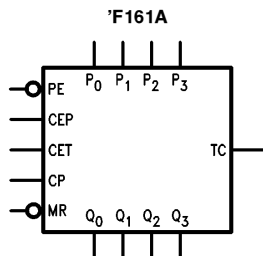
Pin Assignment
for LCC
'F163A



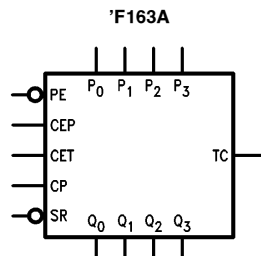
TL/F/9486-8

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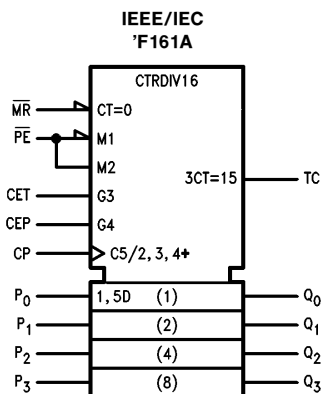
Logic Symbols



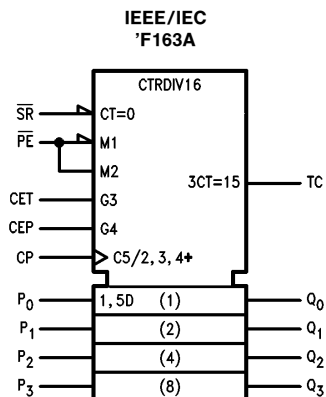
TL/F/9486-3



TL/F/9486-9



TL/F/9486-6



TL/F/9486-10

Unit Loading/Fan Out

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
CEP	Count Enable Parallel Input	1.0/1.0	20 μA/ -0.6 mA
CET	Count Enable Trickle Input	1.0/2.0	20 μA/ -1.2 mA
CP	Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μA/ -0.6 mA
MR ('F161A)	Asynchronous Master Reset Input (Active LOW)	1.0/1.0	20 μA/ -0.6 mA
SR ('F163A)	Synchronous Reset Input (Active LOW)	1.0/2.0	20 μA/ -1.2 mA
P ₀ -P ₃	Parallel Data Inputs	1.0/1.0	20 μA/ -0.6 mA
PE	Parallel Enable Input (Active LOW)	1.0/2.0	20 μA/ -1.2 mA
Q ₀ -Q ₃	Flip-Flop Outputs	50/33.3	-1 mA/20 mA
TC	Terminal Count Output	50/33.3	-1 mA/20 mA

Functional Description

The 'F161A and 'F163A count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the 'F161A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F161A), synchronous reset ('F163A), parallel load, count-up and hold. Five control inputs—Master Reset (\overline{MR} , 'F161A), Synchronous Reset (\overline{SR} , 'F163A), Parallel Enable (\overline{PE}), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on \overline{MR} overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on \overline{SR} overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on \overline{PE} overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the

flip-flops on the next rising edge of CP. With \overline{PE} and \overline{MR} ('F161A) or \overline{SR} ('F163A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'F161A and 'F163A use D-type edge triggered flip-flops and changing the \overline{SR} , \overline{PE} , CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and the counter is in state 15. To implement synchronous multi-stage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = CEP • CET • \overline{PE}

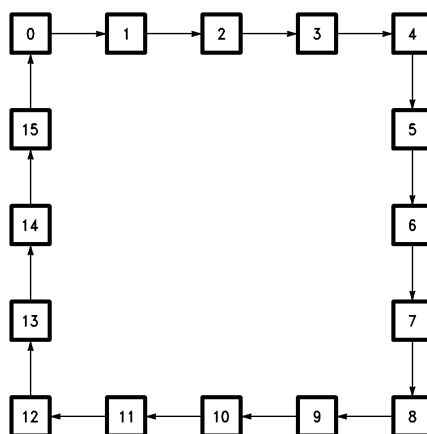
$$TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$$

Mode Select Table

* \overline{SR}	\overline{PE}	CET	CEP	Action on the Rising Clock Edge (↗)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

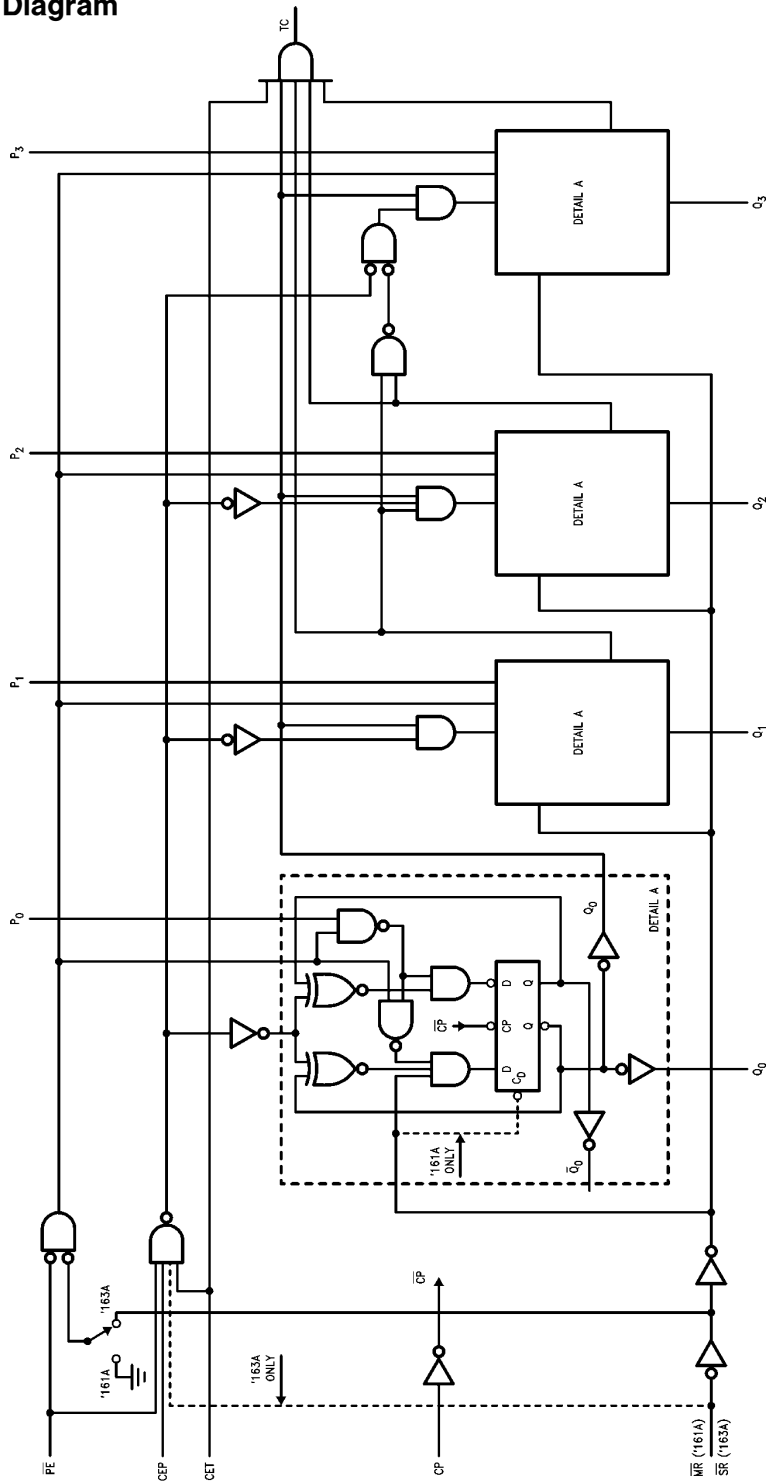
*For 'F163A only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



TL/F/9486-5

Block Diagram



TL/F/9486-4

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE® Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

ESD Last Passing Voltage (Min) 4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC}	2.5 2.5 2.7		V	Min	I _{OH} = −1 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6 −1.2	mA mA	Max Max	V _{IN} = 0.5V (CEP, CP, \overline{MR} , P ₀ –P ₃) V _{IN} = 0.5V (CET, \overline{PE} , \overline{SR})
I _{OS}	Output Short-Circuit Current		−60	−150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		37	55	mA	Max	

AC Electrical Characteristics

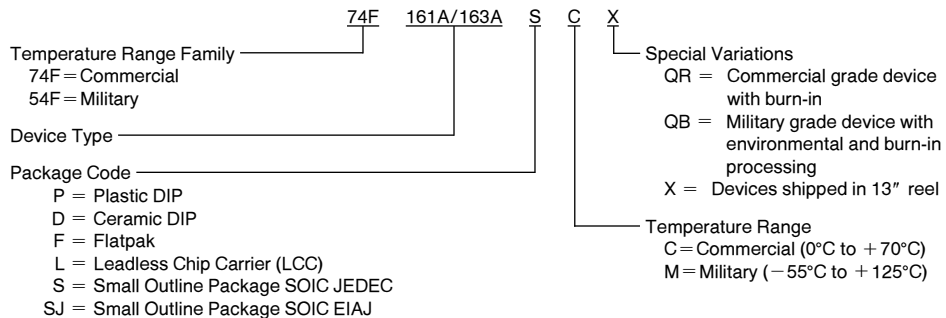
Symbol	Parameter	74F			54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Mil}$ $C_L = 50\text{ pF}$		$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$		
		Min	Typ	Max	Min	Max	Min	Max	
f_{max}	Maximum Count Frequency	100	120		75		90		MHz
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{\text{PE}}$ Input HIGH)	3.5	5.5	7.5	3.5	9.0	3.5	8.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{\text{PE}}$ Input LOW)	3.5	7.5	10.0	3.5	11.5	3.5	11.0	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n ($\overline{\text{PE}}$ Input LOW)	4.0	6.0	8.5	4.0	10.0	4.0	9.5	ns
t_{PLH} t_{PHL}	Propagation Delay CP to TC	4.0	6.0	8.5	4.0	10.0	4.0	9.5	
t_{PLH} t_{PHL}	Propagation Delay CP to TC	5.0	10.0	14.0	5.0	16.5	5.0	15.0	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC	5.0	10.0	14.0	5.0	15.5	5.0	15.0	ns
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5	4.5	7.5	2.5	9.0	2.5	8.5	ns
t_{PHL}	Propagation Delay $\overline{\text{MR}}$ to Q_n ('F161A)	2.5	4.5	7.5	2.5	9.0	2.5	8.5	ns
t_{PHL}	Propagation Delay $\overline{\text{MR}}$ to TC ('F161A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns
t_{PHL}	Propagation Delay $\overline{\text{MR}}$ to TC ('F161A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns

AC Operating Requirements

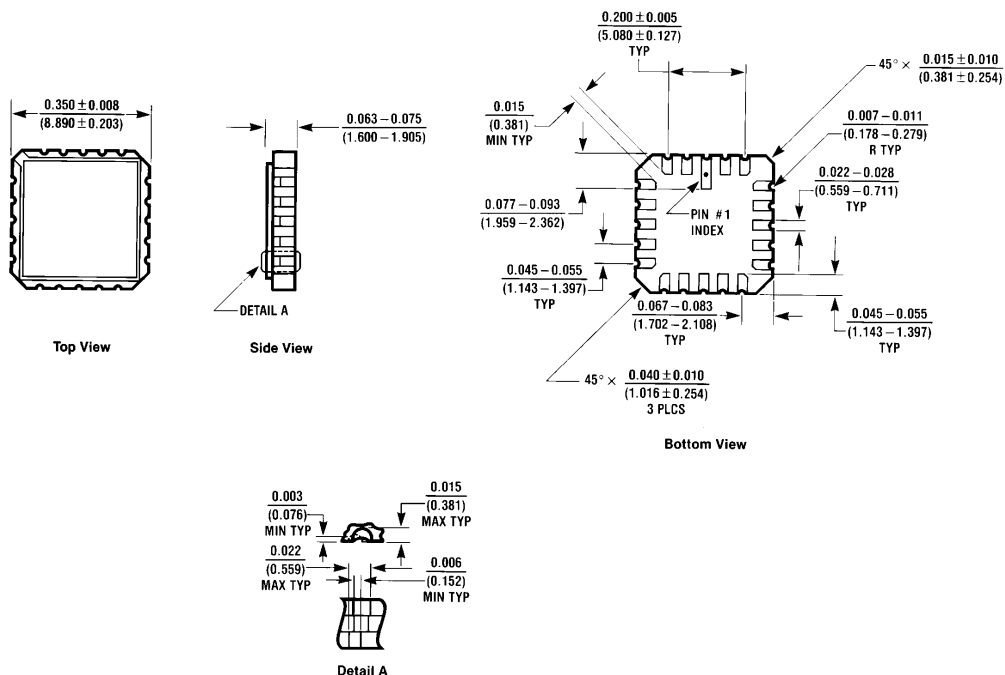
Symbol	Parameter	74F		54F		74F		Units
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Mil}$		$T_A, V_{CC} = \text{Com}$		
		Min	Max	Min	Max	Min	Max	
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW P_n to CP	5.0		5.5		5.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW P_n to CP	5.0		5.5		5.0		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW $\overline{\text{PE}}$ or $\overline{\text{SR}}$ to CP	2.0		2.5		2.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{PE}}$ or $\overline{\text{SR}}$ to CP	2.0		2.5		2.0		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW CEP or CET to CP	11.0		13.5		11.5		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW $\overline{\text{PE}}$ or $\overline{\text{SR}}$ to CP	8.5		10.5		9.5		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW CEP or CET to CP	2.0		3.6		2.0		ns
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW CEP or CET to CP	0		0		0		
$t_w(\text{H})$ $t_w(\text{L})$	Clock Pulse Width (Load) HIGH or LOW	11.0		13.0		11.5		ns
$t_w(\text{H})$ $t_w(\text{L})$	Clock Pulse Width (Count) HIGH or LOW	5.0		6.0		5.0		
$t_w(\text{H})$ $t_w(\text{L})$	Clock Pulse Width (Load) HIGH or LOW	0		0		0		ns
$t_w(\text{H})$ $t_w(\text{L})$	Clock Pulse Width (Count) HIGH or LOW	4.0		5.0		4.0		
$t_w(\text{L})$	$\overline{\text{MR}}$ Pulse Width, LOW ('F161A)	6.0		8.0		7.0		ns
t_{rec}	Recovery Time $\overline{\text{MR}}$ to CP ('F161A)	5.0		5.0		5.0		ns

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



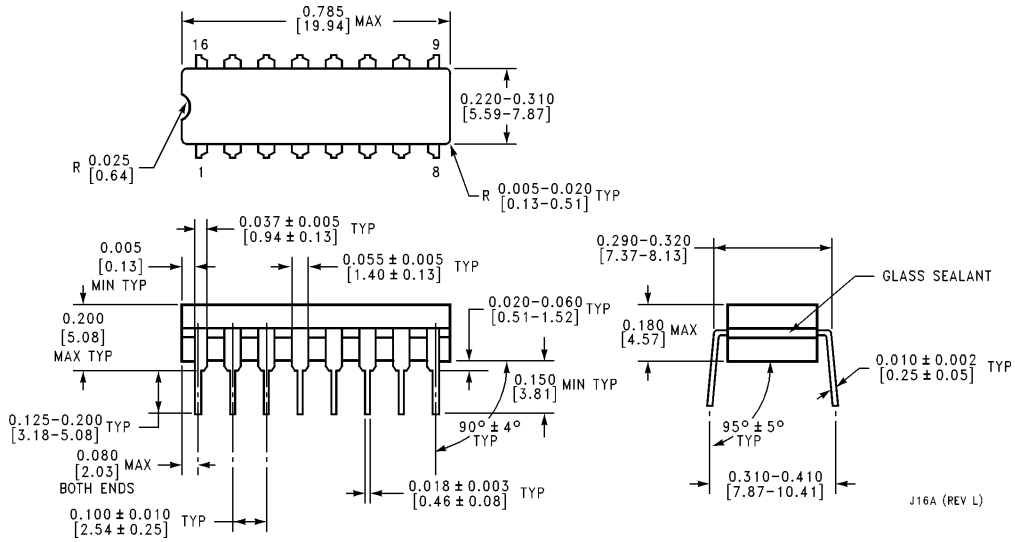
Physical Dimensions inches (millimeters)



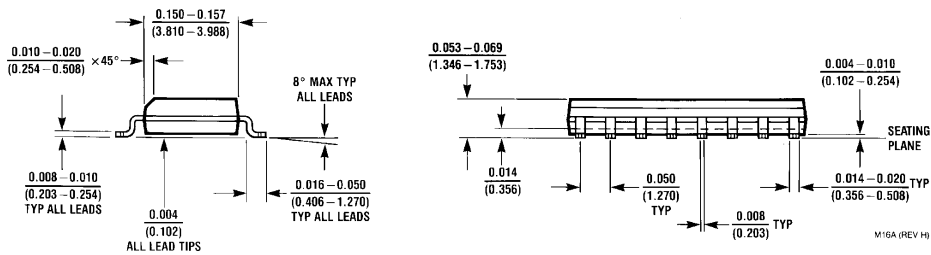
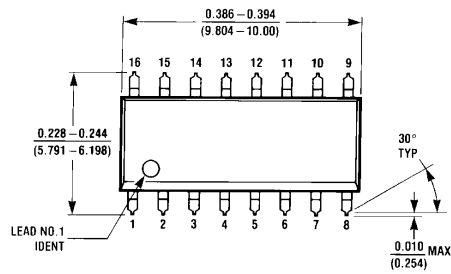
20-Lead Ceramic Leadless Chip Carrier (L)
NS Package Number E20A

E20A (REV D)

Physical Dimensions inches (millimeters) (Continued)

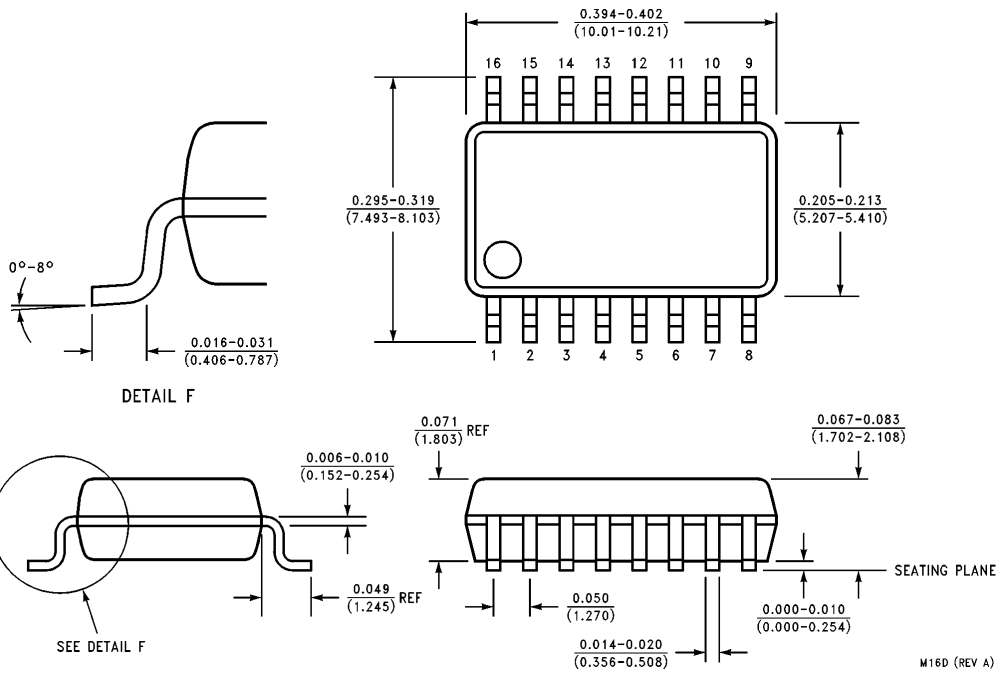


**16-Lead Ceramic Dual-In-Line Package (D)
NS Package Number J16A**

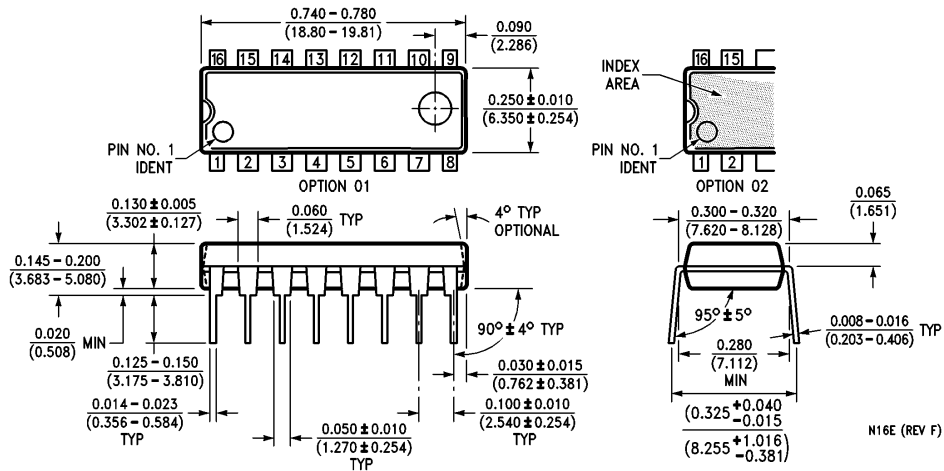


**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)
NS Package Number M16A**

Physical Dimensions inches (millimeters) (Continued)

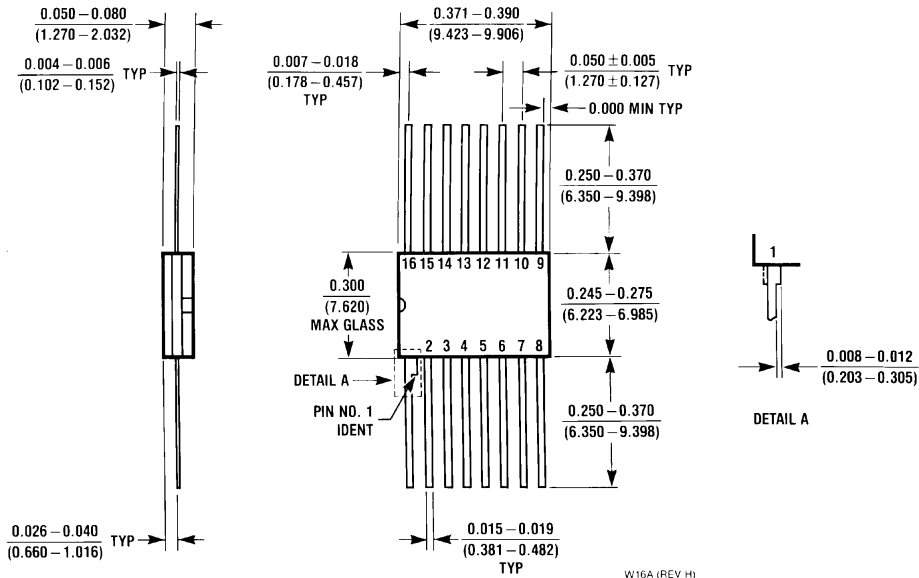


**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)
NS Package Number M16D**



**16-Lead (0.300" Wide) Molded Dual-In-Line Package (P)
NS Package Number N16E**

Physical Dimensions inches (millimeters) (Continued)



**16-Lead Ceramic Flatpak (F)
NS Package Number W16A**

W16A (REV H)

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National Semiconductor Corporation
2900 Semiconductor Drive
P.O. Box 58090
Santa Clara, CA 95052-8090
Tel: 1(800) 272-9959
TWX: (910) 339-9240

National Semiconductor GmbH
Livny-Gargan-Str. 10
D-82256 Fürstenfeldbruck
Germany
Tel: (81-41) 35-0
Telex: 527849
Fax: (81-41) 35-1

National Semiconductor Japan Ltd.
Sumitomo Chemical
Engineering Center
Bldg. 7F
1-7-1, Nakase, Mihama-Ku
Chiba-City,
Ciba Prefecture 261
Tel: (043) 299-2300
Fax: (043) 299-2500

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semicondutores Do Brazil Ltda.
Rue Deputado Lacorda Franco
120-3A
Sao Paulo-SP
Brazil 05418-000
Tel: (55-11) 212-5066
Telex: 391-1131931 NSBR BR
Fax: (55-11) 212-1181

National Semiconductor (Australia) Pty. Ltd.
Building 16
Business Park Drive
Monash Business Park
Nottingham, Melbourne
Victoria 3168 Australia
Tel: (3) 558-9999
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