

# DATA SHEET

**74LV154**

**4-to-16 line decoder/demultiplexer**

Product specification  
Supersedes data of 1997 Mar 07  
IC24 Data Handbook

1998 Apr 28

## 4-to-16 line decoder/demultiplexer

## 74LV154

## FEATURES

- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between  $V_{CC} = 2.7$  V and  $V_{CC} = 3.6$  V
- Typical  $V_{OLP}$  (output ground bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- Typical  $V_{OHV}$  (output  $V_{OH}$  undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_{amb} = 25^{\circ}\text{C}$
- 16-line demultiplexing capability
- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- 2-input enable gate for strobing or expansion
- Output capability: standard
- $I_{CC}$  category: MSI

## DESCRIPTION

The 74LV154 is a low-voltage CMOS device and is pin and function compatible with 74HC/HCT154.

The 74LV154 decoders accept four active HIGH binary address inputs ( $A_0$  to  $A_3$ ) and provide 16 mutually exclusive active LOW outputs ( $\bar{Y}_0$  to  $\bar{Y}_{15}$ ).

The 2-input enable inputs ( $\bar{E}_0$ ,  $\bar{E}_1$ ) can be used to strobe the decoder to eliminate the normal decoding "glitches" on the outputs, or it can be used for expansion of the decoder.

The enable input has two AND'ed inputs which must be LOW to enable the outputs.

The 74LV154 can be used as a 1-to-16 demultiplexer by using one of the enable inputs as the multiplexed data input.

When the other enable is LOW, the addressed output will follow the state of the applied data.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25^{\circ}\text{C}$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay $A_n$ , $\bar{E}_n$ to $\bar{Y}_n$	$C_L = 15$ pF; $V_{CC} = 3.3$ V	11	ns
$C_I$	Input capacitance		3.5	pF
$C_{PD}$	Power dissipation capacitance per gate	$V_I = \text{GND to } V_{CC}^1$	60	pF

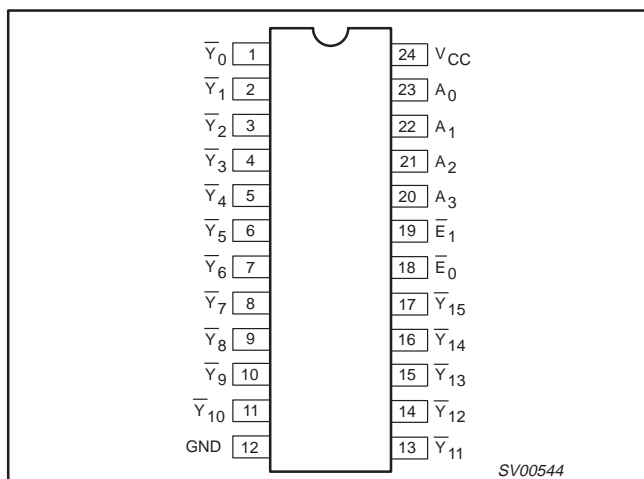
## NOTE:

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic DIL	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV154 N	74LV154 N	SOT101-1
24-Pin Plastic SO	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV154 D	74LV154 D	SOT137-1
24-Pin Plastic SSOP Type II	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV154 DB	74LV154 DB	SOT340-1
24-Pin Plastic TSSOP Type I	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	74LV154 PW	74LV154PW DH	SOT355-1

## PIN CONFIGURATION



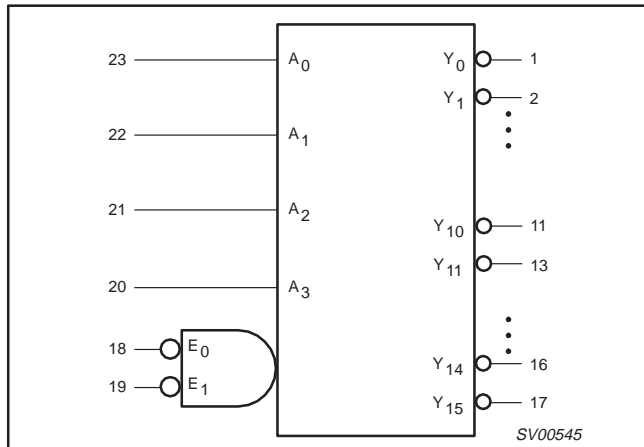
## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 13, 14, 15, 16, 17	$\bar{Y}_0$ to $\bar{Y}_{15}$	Outputs (active LOW)
18, 19	$\bar{E}_0$ , $\bar{E}_1$	Enable inputs (active LOW)
12	GND	Ground (0 V)
23, 22, 21, 20	$A_0$ to $A_3$	Address inputs
16	$V_{CC}$	Positive supply voltage

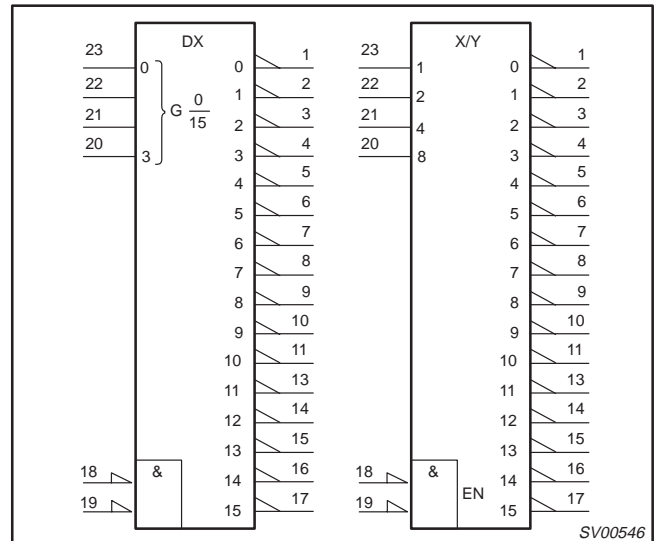
# 4-to-16 line decoder/demultiplexer

# 74LV154

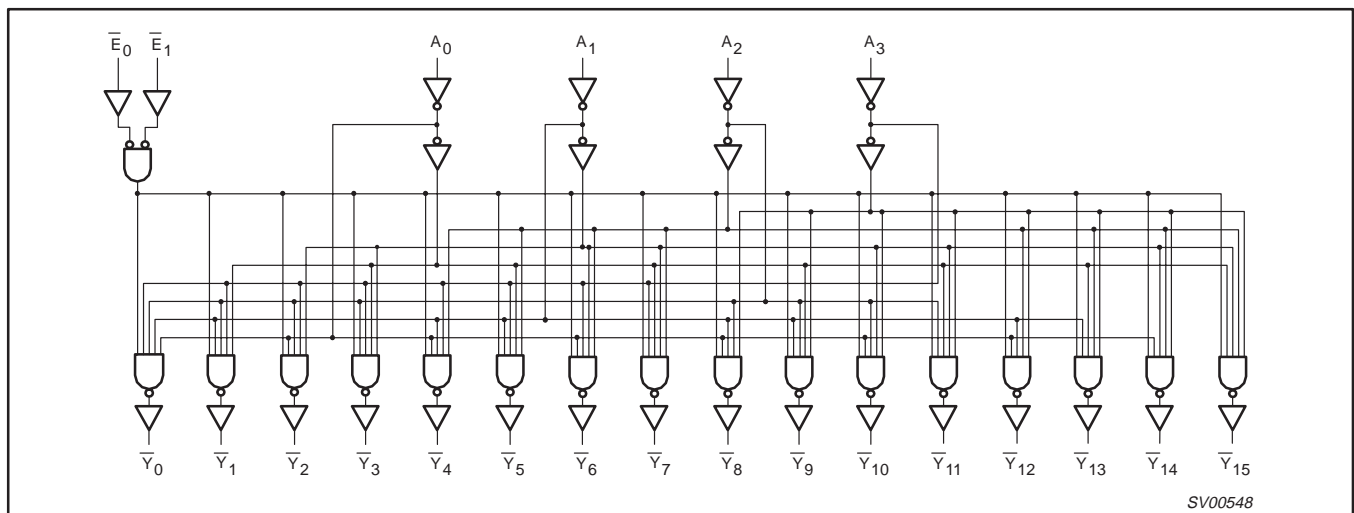
## LOGIC SYMBOL



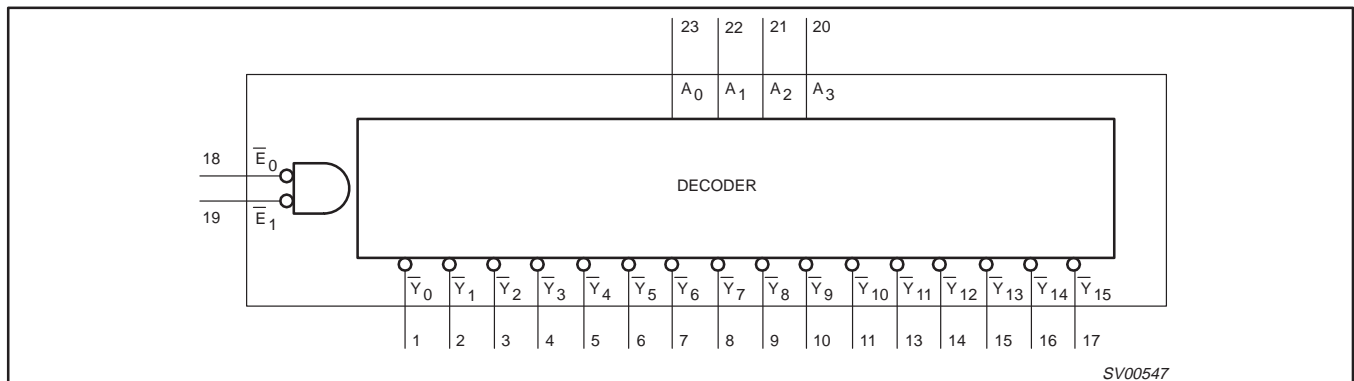
## LOGIC SYMBOL (IEEE/IEC)



## LOGIC DIAGRAM



## FUNCTIONAL DIAGRAM



## 4-to-16 line decoder/demultiplexer

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## FUNCTION TABLE

		INPUTS					OUTPUTS															
$\bar{E}_0$	$\bar{E}_1$	$A_0$	$A_1$	$A_2$	$A_3$	$\bar{Y}_0$	$\bar{Y}_1$	$\bar{Y}_2$	$\bar{Y}_3$	$\bar{Y}_4$	$\bar{Y}_5$	$\bar{Y}_6$	$\bar{Y}_7$	$\bar{Y}_8$	$\bar{Y}_9$	$\bar{Y}_{10}$	$\bar{Y}_{11}$	$\bar{Y}_{12}$	$\bar{Y}_{13}$	$\bar{Y}_{14}$	$\bar{Y}_{15}$	
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L

## NOTES:

H = HIGH voltage level  
L = LOW voltage level  
X = don't care

## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC}$	DC supply voltage	See Note 1	1.0	3.3	3.6	V
$V_I$	Input voltage		0	–	$V_{CC}$	V
$V_O$	Output voltage		0	–	$V_{CC}$	V
$T_{amb}$	Operating ambient temperature range in free air	See DC and AC characteristics	–40 –40		+85 +125	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.0V$ to $2.0V$ $V_{CC} = 2.0V$ to $2.7V$ $V_{CC} = 2.7V$ to $3.6V$	– – –	– – –	500 200 100	ns/V

## NOTE:

1. The LV is guaranteed to function down to  $V_{CC} = 1.0V$  (input levels GND or  $V_{CC}$ ); DC characteristics are guaranteed from  $V_{CC} = 1.2V$  to  $V_{CC} = 3.6V$ .

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**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

In accordance with the Absolute Maximum Rating System (IEC 134).

Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$\pm I_{IK}$	DC input diode current	$V_I < -0.5$ or $V_I > V_{CC} + 0.5V$	20	mA
$\pm I_{OK}$	DC output diode current	$V_O < -0.5$ or $V_O > V_{CC} + 0.5V$	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	$-0.5V < V_O < V_{CC} + 0.5V$	25	mA
$\pm I_{GND}$ , $\pm I_{CC}$	DC $V_{CC}$ or GND current for types with – standard outputs		50	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: -40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

**DC ELECTRICAL CHARACTERISTICS**

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$V_{IH}$	HIGH level Input voltage	$V_{CC} = 1.2 V$	0.9			0.9		V
		$V_{CC} = 2.0 V$	1.4			1.4		
		$V_{CC} = 2.7$ to $3.6 V$	2.0			2.0		
$V_{IL}$	LOW level Input voltage	$V_{CC} = 1.2 V$			0.3		0.3	V
		$V_{CC} = 2.0 V$			0.6		0.6	
		$V_{CC} = 2.7$ to $3.6 V$			0.8		0.8	
$V_{OH}$	HIGH level output voltage; all outputs	$V_{CC} = 1.2 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$		1.2				V
		$V_{CC} = 2.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	1.8	2.0		1.8		
		$V_{CC} = 2.7 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	2.5	2.7		2.5		
		$V_{CC} = 3.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 100\mu A$	2.8	3.0		2.8		
$V_{OH}$	HIGH level output voltage; STANDARD outputs	$V_{CC} = 3.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $-I_O = 6mA$	2.40	2.82		2.20		V
$V_{OL}$	LOW level output voltage; all outputs	$V_{CC} = 1.2 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0				V
		$V_{CC} = 2.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 2.7 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
		$V_{CC} = 3.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 100\mu A$		0	0.2		0.2	
$V_{OL}$	LOW level output voltage; STANDARD outputs	$V_{CC} = 3.0 V$ ; $V_I = V_{IH}$ or $V_{IL}$ ; $I_O = 6mA$		0.25	0.40		0.50	V
$I_I$	Input leakage current	$V_{CC} = 3.6 V$ ; $V_I = V_{CC}$ or GND			1.0		1.0	$\mu A$

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## DC ELECTRICAL CHARACTERISTICS (Continued)

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$I_{CC}$	Quiescent supply current; MSI	$V_{CC} = 3.6\text{ V}; V_I = V_{CC}$ or GND; $I_O = 0$			20.0		160	$\mu\text{A}$
$\Delta I_{CC}$	Additional quiescent supply current per input	$V_{CC} = 2.7\text{ V to } 3.6\text{ V}; V_I = V_{CC} - 0.6\text{ V}$			500		850	$\mu\text{A}$

**NOTE:**

1. All typical values are measured at  $T_{amb} = 25^\circ\text{C}$ .

## AC CHARACTERISTICS

GND = 0V;  $t_r = t_f \leq 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 1\text{ K}\Omega$

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				-40 to +85 °C			-40 to +125 °C		
				MIN	TYP <sup>1</sup>	MAX	MIN	MAX	
$t_{PHL}/t_{PLH}$	Propagation delay $A_n$ to $\bar{Y}_n$	Figures 1, 2	$V_{CC}(V)$						ns
			1.2		65				
			2.0		22	43		51	
			2.7		16	31		38	
			3.0 to 3.6		12 <sup>2</sup>	25		30	
$t_{PHL}/t_{PLH}$	Propagation delay $\bar{E}_n$ to $\bar{Y}_n$	Figures 1, 2	$V_{CC}(V)$						ns
			1.2		70				
			2.0		24	44		54	
			2.7		18	33		40	
			3.0 to 3.6		13 <sup>2</sup>	26		32	

**NOTES:**

1. Unless otherwise stated, all typical values are measured at  $T_{amb} = 25^\circ\text{C}$ .
2. Typical values are measured at  $V_{CC} = 3.3\text{ V}$ .

## AC WAVEFORMS

$V_M = 1.5\text{ V}$  at  $V_{CC} \geq 2.7\text{ V}$ ;

$V_M = 0.5 \times V_{CC}$  at  $V_{CC} < 2.7\text{ V}$ ;

$V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.

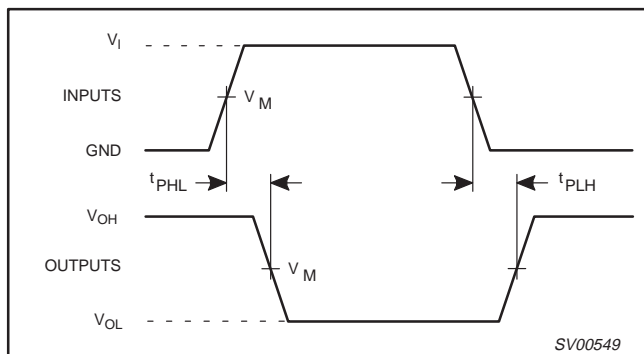


Figure 1. Address input ( $A_n$ ) to output ( $\bar{Y}_n$ ) propagation delays.

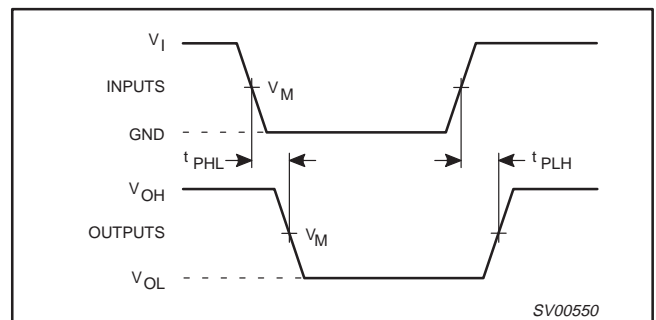


Figure 2. Enable input ( $\bar{E}_n$ ) to output ( $\bar{Y}_n$ ) propagation delays.

# 4-to-16 line decoder/demultiplexer

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## TEST CIRCUIT

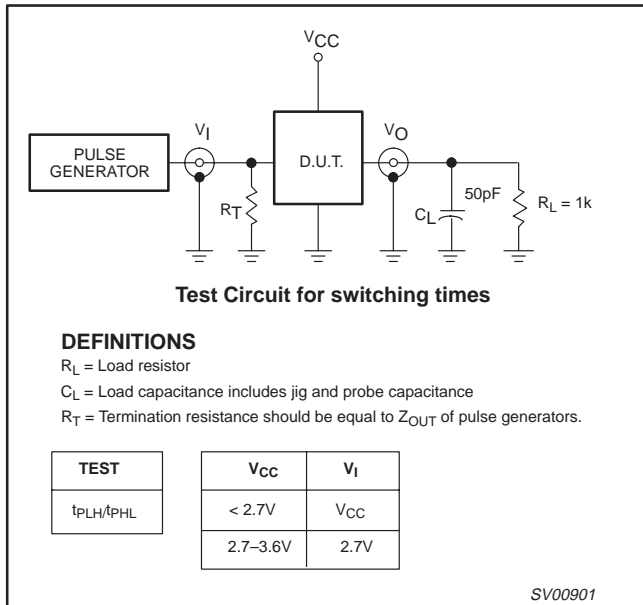


Figure 3. Load circuitry for switching times.

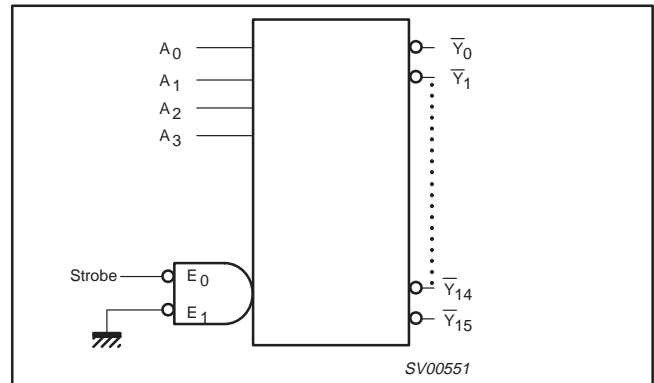


Figure 4. 1-of-16 decoder; LOW level output is selected.

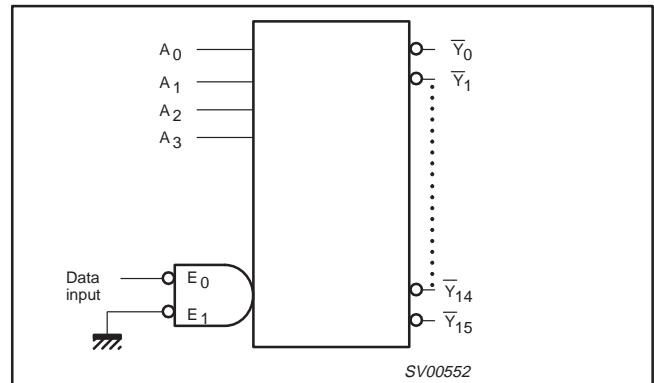


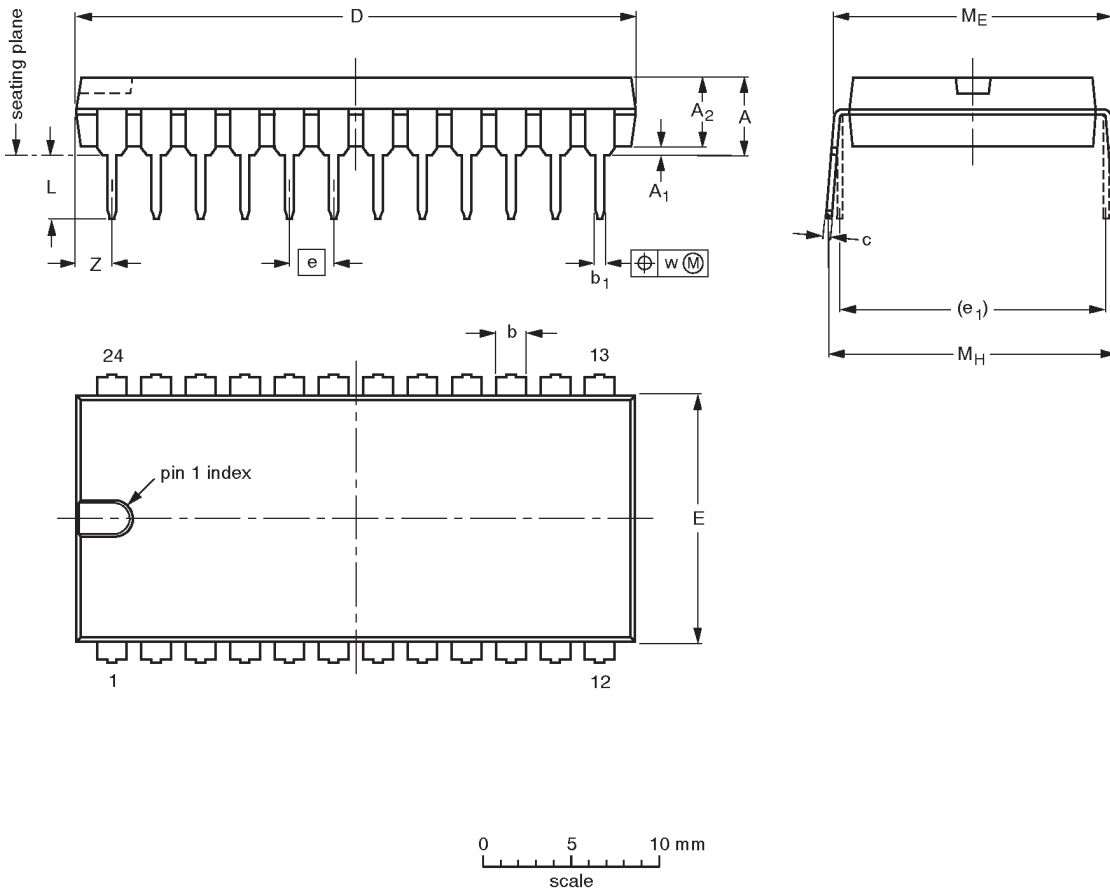
Figure 5. 1-of-16 demultiplexer; logic level on selected outputs follow the logic level on the data input.

# 4-to-16 line decoder/demultiplexer

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**DIP24: plastic dual in-line package; 24 leads (600 mil)**

**SOT101-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	5.1	0.51	4.0	1.7 1.3	0.53 0.38	0.32 0.23	32.0 31.4	14.1 13.7	2.54	15.24	3.9 3.4	15.80 15.24	17.15 15.90	0.25	2.2
inches	0.20	0.020	0.16	0.066 0.051	0.021 0.015	0.013 0.009	1.26 1.24	0.56 0.54	0.10	0.60	0.15 0.13	0.62 0.60	0.68 0.63	0.01	0.087

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

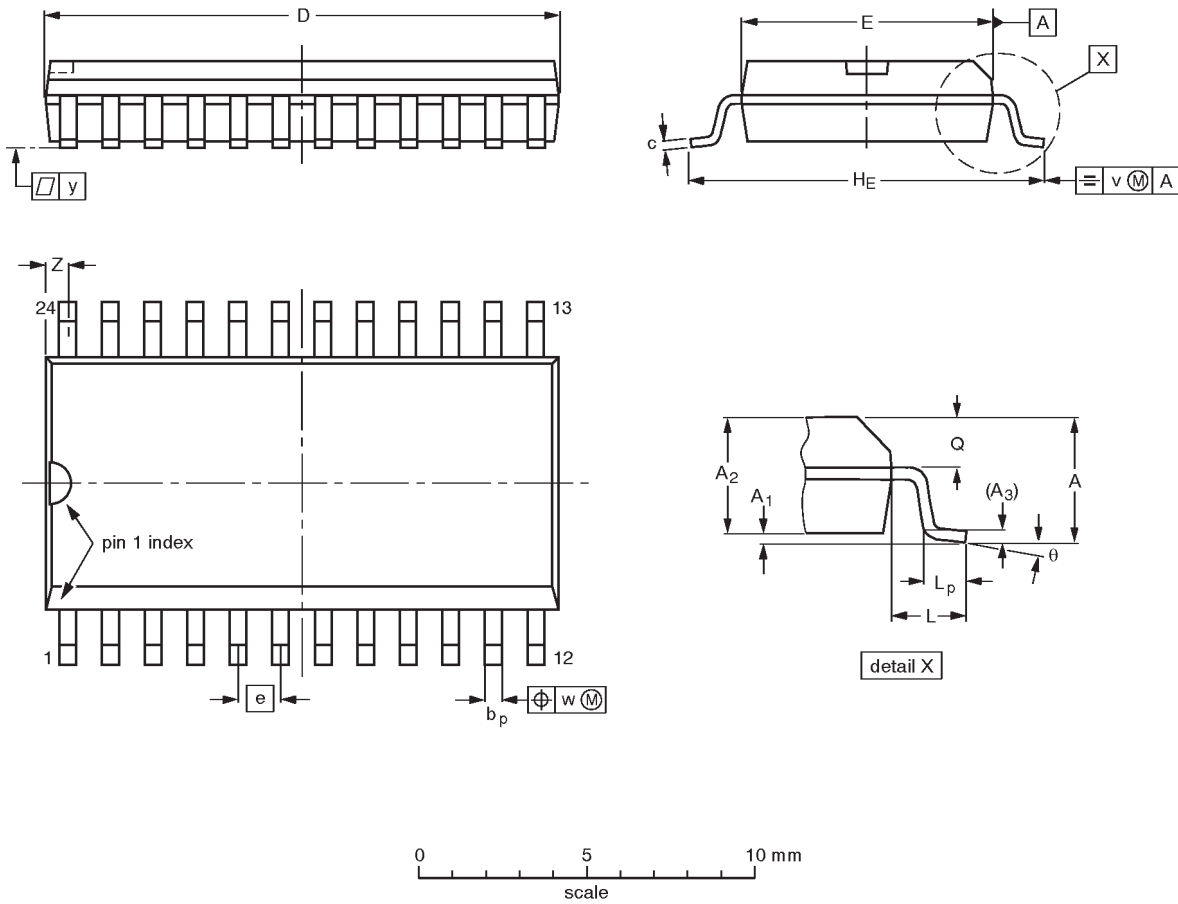
OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ		
SOT101-1	051G02	MO-015AD			92-11-17 95-01-23

# 4-to-16 line decoder/demultiplexer

# 74LV154

**SO24:** plastic small outline package; 24 leads; body width 7.5 mm

**SOT137-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

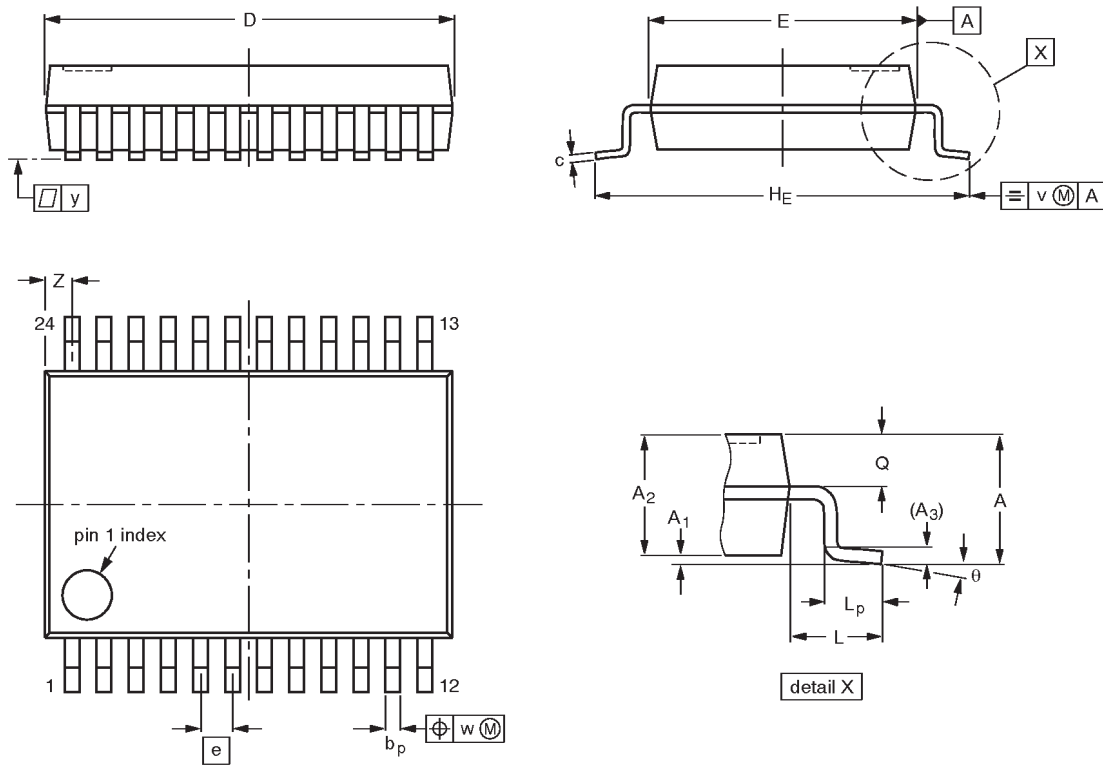
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				-92-11-17 95-01-24

# 4-to-16 line decoder/demultiplexer

# 74LV154

**SSOP24:** plastic shrink small outline package; 24 leads; body width 5.3 mm

**SOT340-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

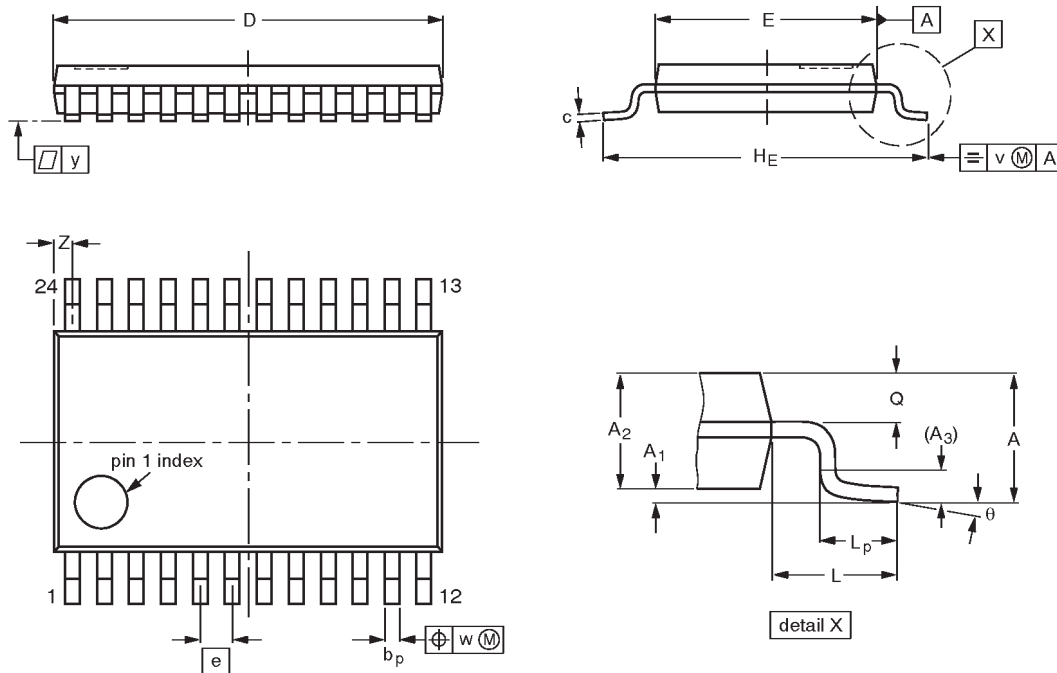
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				93-09-08 95-02-04

# 4-to-16 line decoder/demultiplexer

# 74LV154

**TSSOP24:** plastic thin shrink small outline package; 24 leads; body width 4.4 mm

**SOT355-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				93-06-16 95-02-04

## 4-to-16 line decoder/demultiplexer

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## DEFINITIONS

Data Sheet Identification	Product Status	Definition
<i>Objective Specification</i>	<b>Formative or in Design</b>	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
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