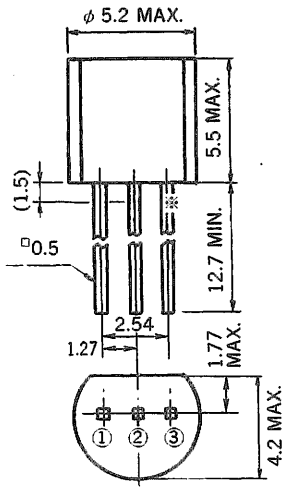
NEC
ELECTRON DEVICE

TRIAC

AC0V8DGM

0.8 A MOLD TRIAC

PACKAGE DIMENSIONS
(Unit : mm)



PIN CONNECTION
1. T_1 Terminal
2. Gate
3. T_2 Terminal
※ Measure point of Case Temperature

DESCRIPTION

The AC0V8DGM is all diffused type TRIAC granted RMS On-state Current 0.8 Amps, with rated voltages up to 400 volts.

This is designed specifically to be driven by low-level logic in any gating mode.

FEATURES

- The AC0V8DGM offers sensitive gate specs of 5 and 10 mA, in all four quadrants.
- You can fill the gap between microprocessor controls and the power-output requirements.
- This is housed in the popular TO-92 package.
- The package features excellent environmental stress and temperature cycling.

APPLICATIONS

Solid-state relays, microprocessor interfacing, TTL logic and various solid-state switch designs alone or with larger TRIAC.

MAXIMUM RATINGS

ITEM	SYMBOL	MAXIMUM RATINGS	UNIT	NOTE
Repetitive Peak off Voltage	V_{DRM}	400	V	
Non-repetitive Peak off Voltage	V_{DSM}	500	V	
RMS On-State Current	$I_{T(RMS)}$	0.8 (T_C = 68 °C)	A	Fig. 12, 13
Peak Surge On-State Current	I_{TSM}	7 (50 Hz), 8 (60 Hz)	A	Fig. 2
Fusing Current	$\int i^2 T dt$	0.2 (1 ms ≦ t ≦ 10 ms)	A^2s	
Peak Gate Power Dissipation	P_{GM}	1	W	
Average Gate Power Dissipation	$P_{G(AV)}$	0.1	W	
Peak Gate Current	I_{GM}	±1	A	
Junction Temperature	T_j	125	°C	
Storage Temperature	T_{stg}	−55 to +150	°C	

ELECTRICAL CHARACTERISTICS (T_j = 25 °C)

ITEM		SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Peak Off-State Current		I_{DRM}	$V_{DM} = V_{DRM}$	T_j = 25 °C	–	–	10	μA	
				T_j = 125 °C	–	–	100		
On-State Voltage		V_{TM}	I_{TM} = 1.2 A		–	–	1.5	V	Fig. 1
Critical Rate of Rise of Off-State Voltage		dv/dt	T_j = 125 °C, $V_{DM} = \frac{2}{3} V_{DRM}$ Gate Open Circuited Exponential Waveform		–	50	–	V/μs	
*DC Gate Trigger Current	MODE I	I_{GT}	V_{DM} = 12 V R_L = 100 Ω	G; Positive, T_2; Positive	–	–	5	mA	Fig. 4, 5
	II			G; Negative, T_2; Positive	–	–	10		
	III			G; Negative, T_2; Negative	–	–	5		
	IV			G; Positive, T_2; Negative	–	–	10		
DC Gate Trigger Voltage	MODE I	V_{GT}	V_{DM} = 12 V R_L = 100 Ω	G; Positive, T_2; Positive	–	–	1.0	V	Fig. 4, 5
	II			G; Negative, T_2; Positive	–	–	1.5		
	III			G; Negative, T_2; Negative	–	–	1.0		
	IV			G; Positive, T_2; Negative	–	–	1.5		
Gate Non-Trigger Voltage		V_{GD}	T_j = 125 °C $V_{DM} = \frac{1}{2} V_{DRM}$		0.1	–	–	V	
DC Holding Current		I_H	V_D = 24 V, I_{TM} = 1 A		–	5	10	mA	
Critical Rate of Rise of Commutating Off-State Voltage		(dv/dt)c	T_j = 125 °C, I_{TM} = 1.2 A $(di_T/dt)c$ = –0.5 A/ms V_{DM} = 400 V		1	–	–	V/μs	
Steady State		$R_{th(j-c)}$	Junction to Case		–	–	65	°C/W	
Thermal Resistance		$R_{th(j-a)}$	Junction to Ambient		–	–	200	°C/W	Fig. 14

* All four quardrants: 5 mA Max. Selected types available from factory.

Fig. 1 $i_T - V_T$ CHARACTERISTIC

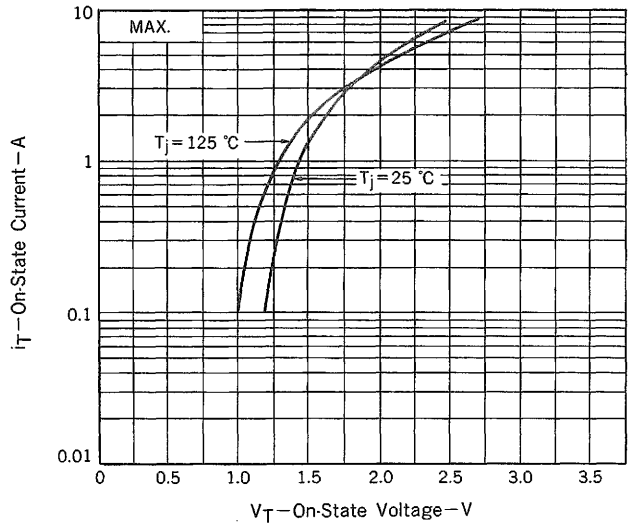


Fig. 2 I_{TSM} RATING

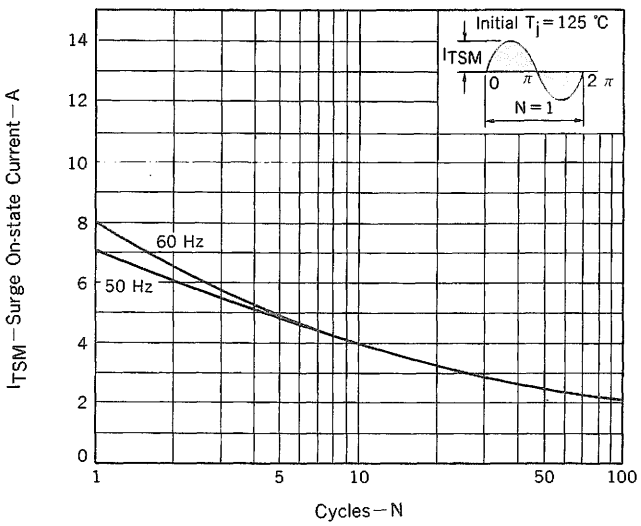


Fig. 3 $V_G - I_G$ RATING

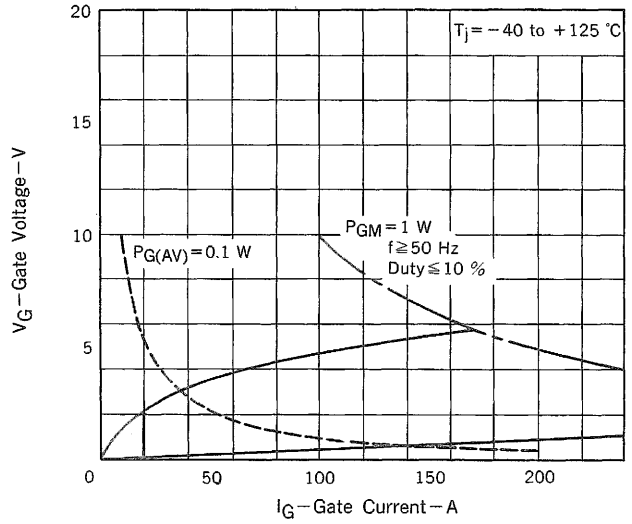


Fig. 4 GATE CHARACTERISTIC

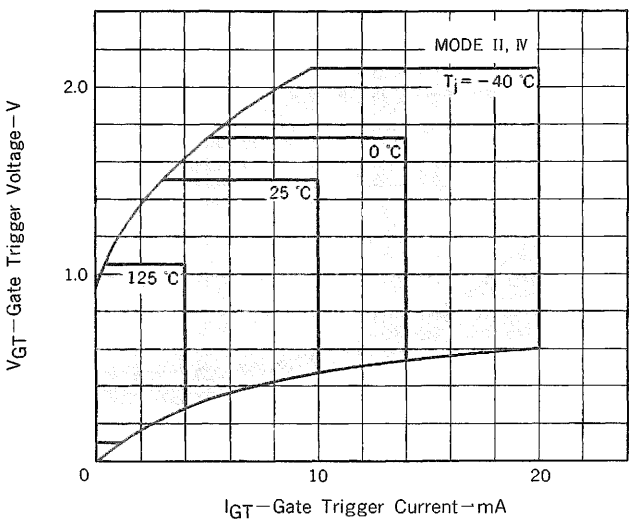


Fig. 5 GATE CHARACTERISTIC

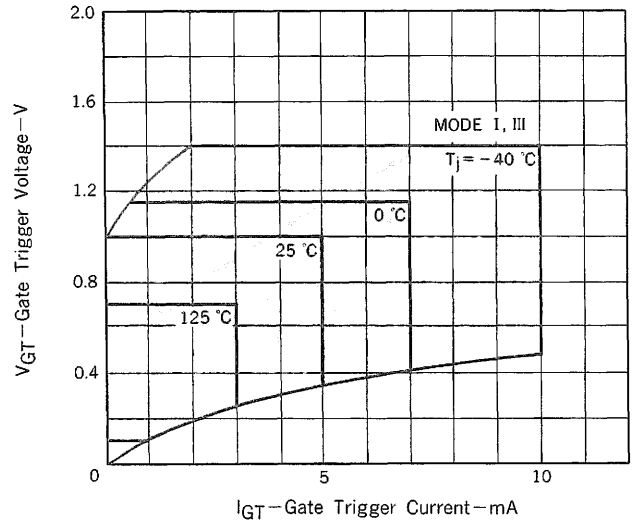


Fig. 6 $I_{GT} - T_a$ TYPICAL DISTRIBUTION

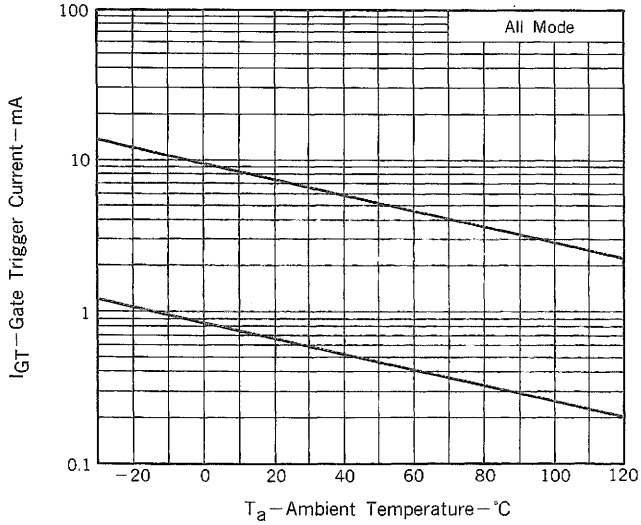


Fig. 7 V_{GT} – T_a TYPICAL DISTRIBUTION

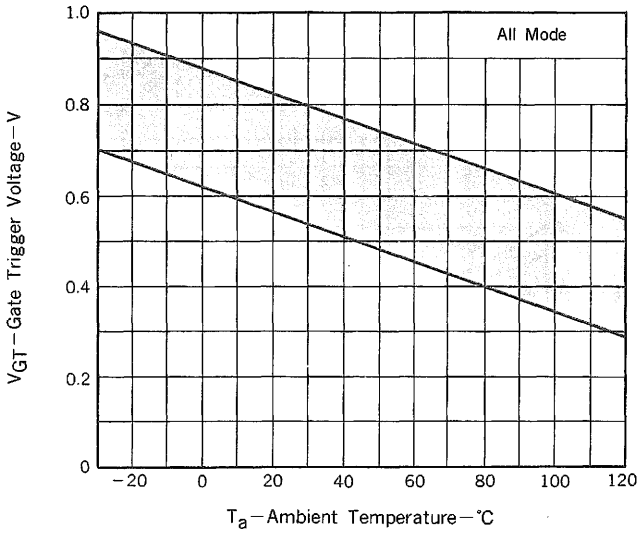


Fig. 8 i_{GT} – τ TYPICAL DISTRIBUTION

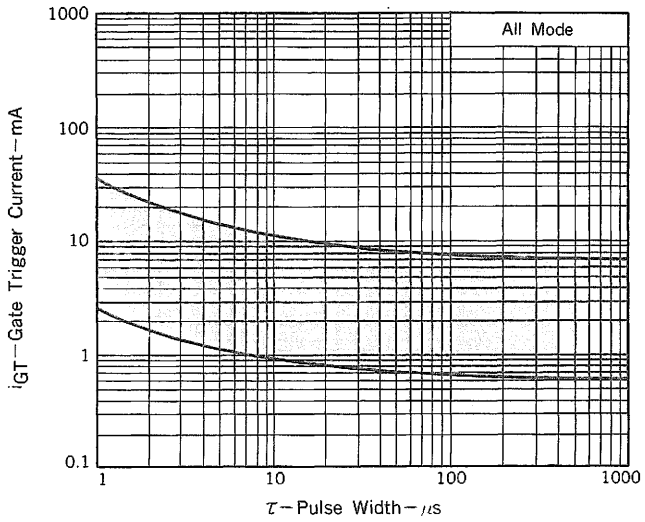


Fig. 9 v_{GT} – τ TYPICAL DISTRIBUTION

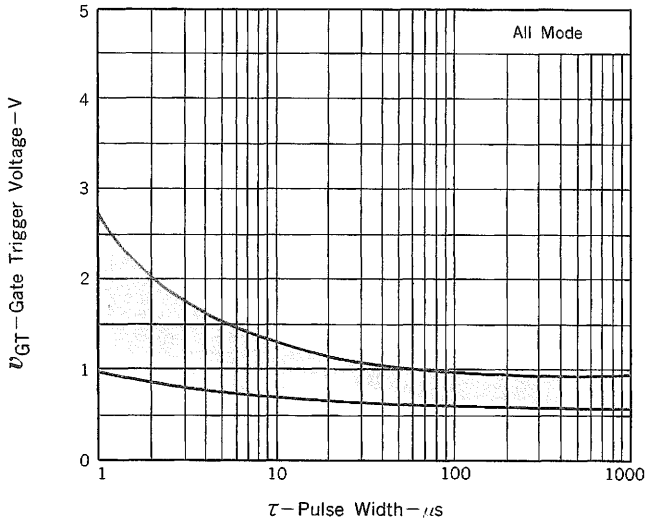


Fig. 10 I_H – T_a TYPICAL DISTRIBUTION

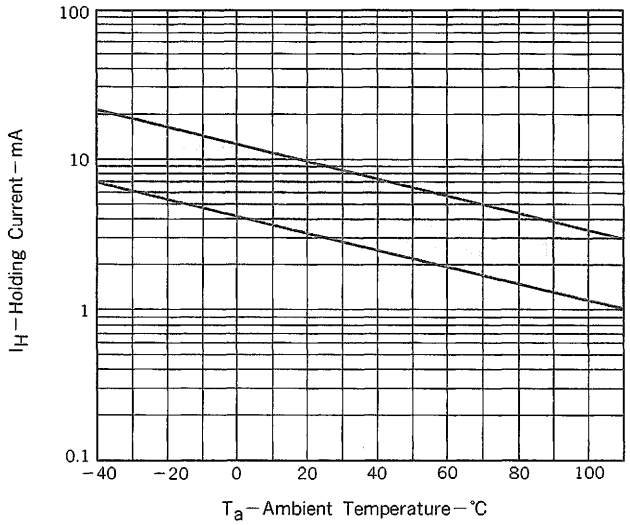


Fig. 11 $P_{T(AV)}$ – $I_{T(RMS)}$ CHARACTERISTIC

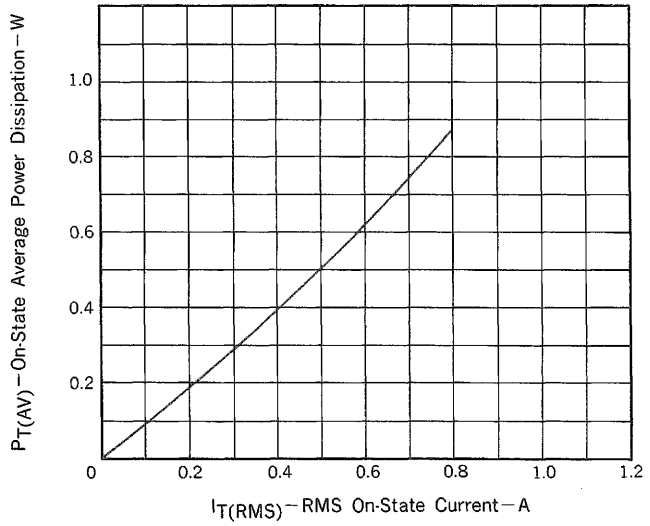


Fig. 12 T_c – $I_{T(RMS)}$ RATING

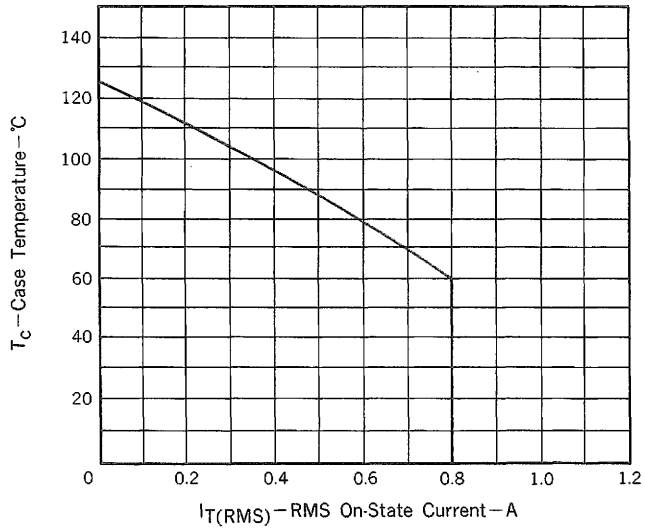


Fig. 13 $T_a - I_{T(RMS)}$ RATING

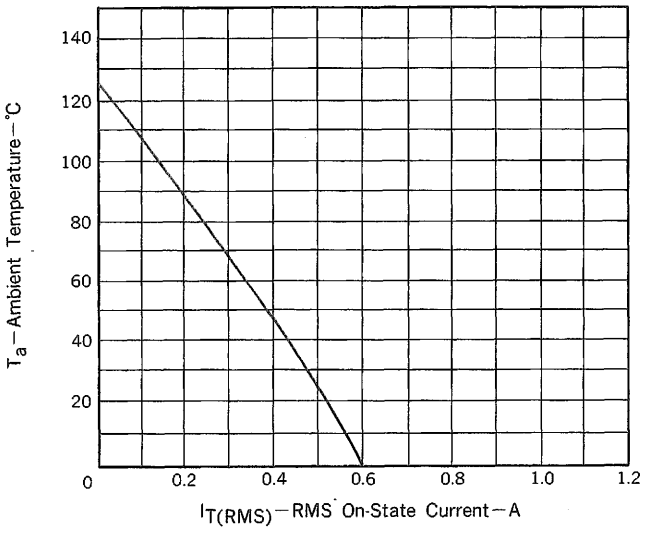
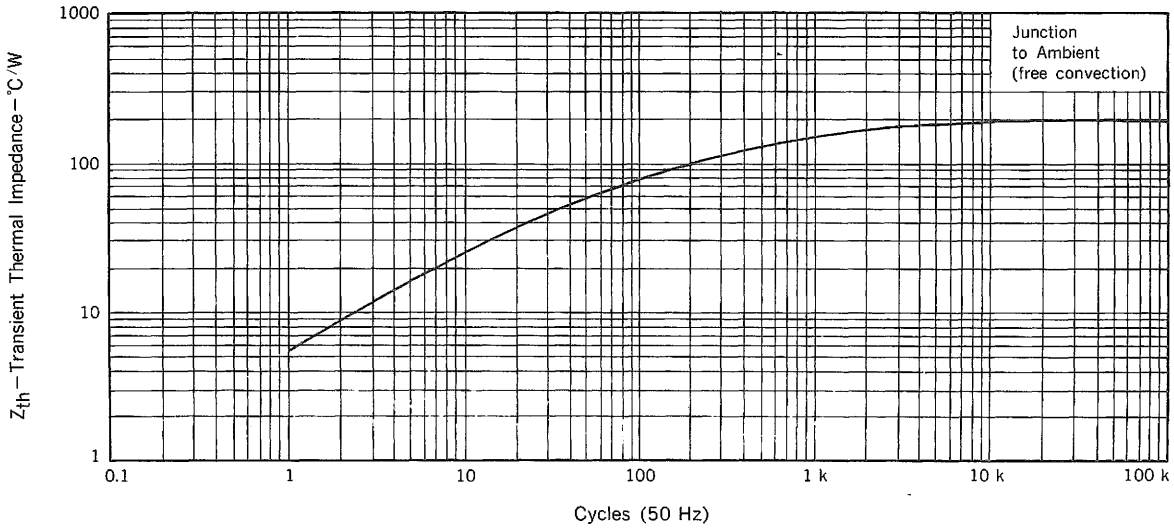


Fig. 14 Z_{th} CHARACTERISTIC



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