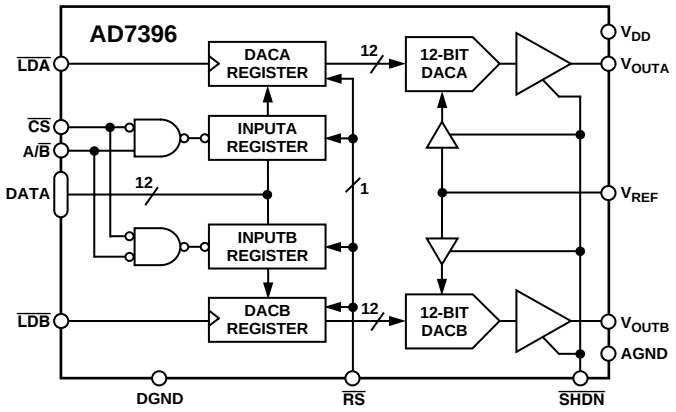
3 V, Parallel Input Dual 12-Bit/10-Bit DACs

AD7396/AD7397

FEATURES
Micropower: 100 μA/DAC
0.1 μA Typical Power Shutdown
Single Supply +2.7 V to +5.5 V Operation
Compact 1.1 mm Height TSSOP 24-Lead Package
AD7396: 12-Bit Resolution
AD7397: 10-Bit Resolution
0.9 LSB Differential Nonlinearity Error

APPLICATIONS
Automotive Output Span Voltage
Portable Communications
Digitally Controlled Calibration
PC Peripherals

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The AD7396/AD7397 series of dual, 12-bit and 10-bit voltage-output digital-to-analog converters are designed to operate from a single +3 V supply. Built using a CBCMOS process, these monolithic DACs offer the user low cost and ease of use in single supply +3 V systems. Operation is guaranteed over the supply voltage range of +2.7 V to +5.5 V, making this device ideal for battery operated applications.

A 12-bit wide data latch loads with a 45 ns write time allowing interface to fast processors without wait states. The double buffered input structure allows the user to load the input registers one at a time, then a single load strobe tied to both $\overline{LDA}$+$\overline{LDB}$ inputs will simultaneously update both DAC outputs. $\overline{LDA}$ and $\overline{LDB}$ can also be independently activated to immediately update their respective DAC registers. An address input (A/$\overline{B}$) decodes DACA or DACB when the chip select $\overline{CS}$ input is strobed. Additionally, an asynchronous $\overline{RS}$ input sets the output to zero-scale at power on or upon user demand. Power shutdown to submicroamp levels is directly controlled by the active low $\overline{SHDN}$ pin. While in the power shutdown state register data can still be changed even though the output buffer is in an open circuit state. Upon return to the normal operating state the latest data loaded in the DAC register will establish the output voltage.

Both parts are offered in the same pinout, allowing users to select the amount of resolution appropriate for their applications without circuit card changes.

The AD7396/AD7397 are specified for operation over the extended industrial (–40°C to +85°C) temperature range. The AD7397AR is specified for the –40°C to +125°C automotive temperature range. AD7396/AD7397s are available in plastic DIP, and 24-lead SOIC packages. The AD7397ARU is available for ultracompact applications in a thin 1.1 mm height TSSOP 24-lead package.

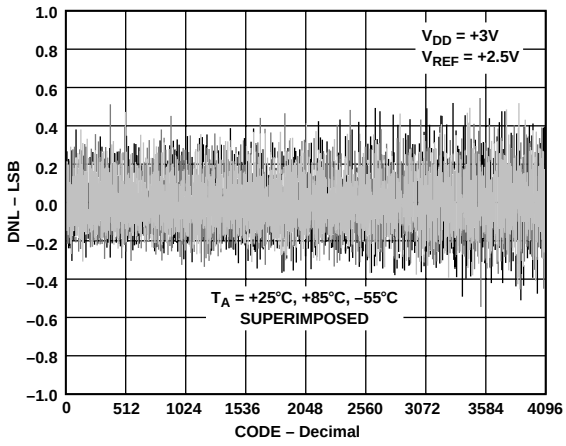


Figure 1. DNL vs. Digital Code at Temperature

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AD7396/AD7397–SPECIFICATIONS

AD7396 12-BIT

ELECTRICAL CHARACTERISTICS (@ $V_{REF\ IN}$ = +2.5 V, –40°C < T_A < +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	+3 V ± 10%	+5 V ± 10%	Units
STATIC PERFORMANCE					
Resolution[1]	N		12	12	Bits
Relative Accuracy[2]	INL	T_A = +25°C	±1.75	±1.75	LSB max
Relative Accuracy[2]	INL	T_A = –40°C, +85°C	±2.0	±2.0	LSB max
Differential Nonlinearity[2]	DNL	T_A = +25°C, Monotonic	±0.9	±0.9	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H, T_A = +25°C, +85°C	4.0	4.0	mV max
Zero-Scale Error	V_{ZSE}	Data = 000_H, T_A = –40°C	8.0	8.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = +25°C, +85°C, Data = FFF_H	±8	±8	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = –40°C, Data = FFF_H	±20	±20	mV max
Full-Scale Tempco[3]	TCV_{FS}		–45	–45	ppm/°C typ
REFERENCE INPUT					
V_{REF} Range	V_{REF}		$0/V_{DD}$	$0/V_{DD}$	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (Source)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 800_H, ΔV_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD} – 0.6	4.0	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Chip Select Write Width	t_{CS}		45	35	ns min
DAC Select Setup	t_{AS}		30	15	ns min
DAC Select Hold	t_{AH}		0	0	ns min
Data Setup	t_{DS}		30	15	ns min
Data Hold	t_{DH}		20	10	ns min
Load Setup	t_{LS}		20	20	ns min
Load Hold	t_{LH}		10	10	ns min
Load Pulsewidth	t_{LDW}		30	30	ns min
Reset Pulsewidth	t_{RSW}		40	30	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to FFF_H to 000_H	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	µs typ
Shutdown Recovery Time	t_{SDR}		90	80	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nV/s typ
Digital Feedthrough	Q		15	15	nV/s typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} +1 V p-p, Data = 000_H, f = 100 kHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load	125/200	125/200	µA typ/max
Shutdown Supply Current	I_{DD_SD}	$\overline{SHDN}$ = 0, V_{IL} = 0 V, No Load	0.1/1.5	0.1/1.5	µA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	600	1000	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES

[1]One LSB = V_{REF}/4096 V for the 12-bit AD7396.

[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.

[3]These parameters are guaranteed by design and not subject to production testing.

[4]Typicals represent average readings measured at +25°C.

[5]All input control signals are specified with $t_R = t_F$ = 2 ns (10% to 90% of +3 V) and timed from a voltage level of +1.6 V.

[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

AD7397 10-BIT ELECTRICAL CHARACTERISTICS (@ $V_{REF\ IN}$ = +2.5 V, –40°C < T_A < +85°C, unless otherwise noted)

Parameter	Symbol	Conditions	+3 V ± 10%	+5 V ± 10%	Units
STATIC PERFORMANCE					
Resolution[1]	N		10	10	Bits
Relative Accuracy[2]	INL	T_A = +25°C	±1.75	±1.75	LSB max
Relative Accuracy[2]	INL	T_A = –40°C, +85°C, +125°C	±2.0	±2.0	LSB max
Differential Nonlinearity[2]	DNL	Monotonic	±1	±1	LSB max
Zero-Scale Error	V_{ZSE}	Data = 000_H	9.0	9.0	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = +25°C, +85°C, +125°C, Data = $3FF_H$	±42	±42	mV max
Full-Scale Voltage Error	V_{FSE}	T_A = –40°C, Data = $3FF_H$	±48	±48	mV max
Full-Scale Tempco[3]	TCV_{FS}		–45	–45	ppm/°C typ
REFERENCE INPUT					
V_{REF} Range	V_{REF}		$0/V_{DD}$	$0/V_{DD}$	V min/max
Input Resistance	R_{REF}		2.5	2.5	MΩ typ[4]
Input Capacitance[3]	C_{REF}		5	5	pF typ
ANALOG OUTPUT					
Output Current (Source)	I_{OUT}	Data = 200_H, ΔV_{OUT} = 5 LSB	1	1	mA typ
Output Current (Sink)	I_{OUT}	Data = 200_H, ΔV_{OUT} = 5 LSB	3	3	mA typ
Capacitive Load[3]	C_L	No Oscillation	100	100	pF typ
LOGIC INPUTS					
Logic Input Low Voltage	V_{IL}		0.5	0.8	V max
Logic Input High Voltage	V_{IH}		V_{DD} – 0.6	4.0	V min
Input Leakage Current	I_{IL}		10	10	µA max
Input Capacitance[3]	C_{IL}		10	10	pF max
INTERFACE TIMING[3, 5]					
Chip Select Write Width	t_{CS}		45	35	ns min
DAC Select Setup	t_{AS}		30	15	ns min
DAC Select Hold	t_{AH}		0	0	ns min
Data Setup	t_{DS}		30	15	ns min
Data Hold	t_{DH}		20	10	ns min
Load Setup	t_{LS}		20	20	ns min
Load Hold	t_{LH}		10	10	ns min
Load Pulsewidth	t_{LDW}		30	30	ns min
Reset Pulsewidth	t_{RSW}		40	30	ns min
AC CHARACTERISTICS					
Output Slew Rate	SR	Data = 000_H to $3FF_H$ to 000_H	0.05	0.05	V/µs typ
Settling Time[6]	t_S	To ±0.1% of Full Scale	70	60	µs typ
Shutdown Recovery Time	t_{SDR}		90	80	µs typ
DAC Glitch	Q	Code $7FF_H$ to 800_H to $7FF_H$	65	65	nV/s typ
Digital Feedthrough	Q		15	15	nV/s typ
Feedthrough	V_{OUT}/V_{REF}	V_{REF} = 1.5 V_{DC} +1 V p-p, Data = 000_H, f = 100 kHz	–63	–63	dB typ
SUPPLY CHARACTERISTICS					
Power Supply Range	$V_{DD\ RANGE}$	DNL < ±1 LSB	2.7/5.5	2.7/5.5	V min/max
Positive Supply Current	I_{DD}	V_{IL} = 0 V, No Load	125/200	125/200	µA typ/max
Shutdown Supply Current	I_{DD_SD}	$\overline{SHDN}$ = 0, V_{IL} = 0 V, No Load	0.1/1.5	0.1/1.5	µA typ/max
Power Dissipation	P_{DISS}	V_{IL} = 0 V, No Load	600	1000	µW max
Power Supply Sensitivity	PSS	ΔV_{DD} = ±5%	0.006	0.006	%/% max

NOTES
[1]One LSB = V_{REF}/4096 V for the 10-bit AD7397.
[2]The first two codes (000_H, 001_H) are excluded from the linearity error measurement.
[3]These parameters are guaranteed by design and not subject to production testing.
[4]Typicals represent average readings measured at +25°C.
[5]All input control signals are specified with t_R = t_F = 2 ns (10% to 90% of +3 V) and timed from a voltage level of +1.6 V.
[6]The settling time specification does not apply for negative going transitions within the last 3 LSBs of ground.

Specifications subject to change without notice.

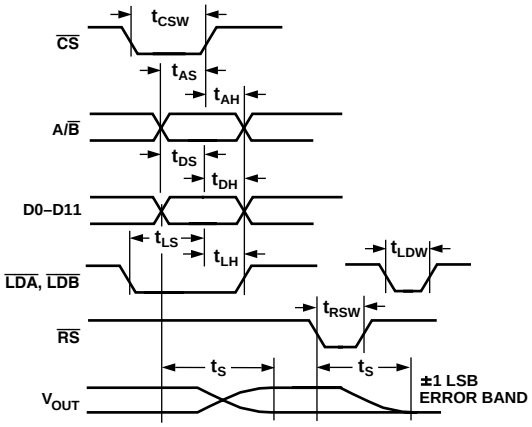


Figure 2. Timing Diagram

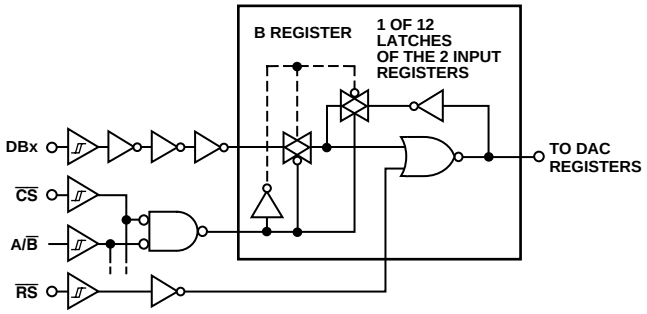


Figure 3. Digital Control Logic

Table I. Control Logic Truth

$\overline{CS}$	A/$\overline{B}$	$\overline{LDA}$	$\overline{LDB}$	$\overline{RS}$	$\overline{SHDN}$	Input Register	DAC Register
L	L	H	H	H	X	Write to B	Latched with Previous Data
L	H	H	H	H	X	Write to A	Latched with Previous Data
L	L	H	L	H	X	Write to B	B Transparent
L	H	L	H	H	X	Write to A	A Transparent
H	X	L	L	H	X	Latched	A and B Transparent
H	X	^	^	H	X	Latched	Latched with New Data from Input REG
X	X	X	X	L	X	Reset to Zero Scale	Reset to Zero Scale
H	X	X	X	^	X	Latched to Zero	Latched to Zero

^Denotes positive edge. The $\overline{SHDN}$ pin has no effect on the digital interface data loading; however, while in the $\overline{SHDN}$ state ($\overline{SHDN}$ = 0) the output amplifiers V_{OUTA} and V_{OUTB} exhibit an open circuit condition. Note, the $\overline{LDx}$ inputs are level-sensitive, the respective DAC registers are in a transparent state when $\overline{LDx}$ = "0."

ABSOLUTE MAXIMUM RATINGS*

V_{DD} to GND . . . . . –0.3 V, +8 V
V_{REF} to GND . . . . . –0.3 V, V_{DD}
Logic Inputs to GND . . . . . –0.3 V, +8 V
V_{OUT} to GND . . . . . –0.3 V, V_{DD} + 0.3 V
AGND to DGND . . . . . –0.3 V, +2 V
I_{OUT} Short Circuit to GND . . . . . +50 mA
Package Power Dissipation . . . . . (T_J max – T_A)/θ_{JA}
Thermal Resistance θ_{JA}
24-Lead Plastic DIP Package (N-24) . . . . . +63°C/W
24-Lead SOIC Package (R-24) . . . . . +70°C/W
24-Lead Thin Shrink Surface Mount (RU-24) . . +143°C/W
Maximum Junction Temperature (T_J max) . . . . . +150°C
Operating Temperature Range . . . . . –40°C to +85°C
AD7397AN, AD7397AR Only . . . . . –40°C to +125°C
Storage Temperature Range . . . . . –65°C to +150°C
Lead Temperature
N-24 (Soldering, 10 sec) . . . . . +300°C
R-24 (Vapor Phase, 60 sec) . . . . . +215°C
RU-24 (Infrared, 15 sec) . . . . . +224°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

Model	Res (LSB)	Temperature Ranges	Package Descriptions	Package Options
AD7396AN	12	–40°C to +85°C	24-Lead P-DIP	N-24
AD7396AR	12	–40°C to +85°C	24-Lead SOIC	R-24
AD7397AN	10	–40°C to +125°C	24-Lead P-DIP	N-24
AD7397AR	10	–40°C to +125°C	24-Lead SOIC	R-24
AD7397ARU	10	–40°C to +85°C	24-Lead Thin Shrink Small Outline Package (TSSOP)	RU-24

The AD7396/AD7397 contains 1365 transistors. The die size measures 89 mil × 106 mil = 9434 sq mil.

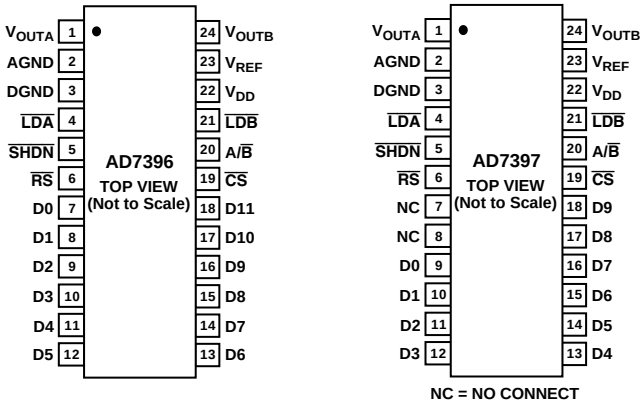
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD7396/AD7397 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN FUNCTION DESCRIPTIONS

Pin No.	Name	
1	V_{OUTA}	DAC A Voltage Output.
2	AGND	Analog Ground.
3	DGND	Digital Ground.
4	$\overline{LDA}$	Load DAC A Register Strobe. Transfers input register data to the DAC A register. Active low inputs, Level sensitive latch. May be connected together with $\overline{LDB}$ to double-buffer load both DAC registers simultaneously.
5	$\overline{SHDN}$	Power Shutdown Active Low Input. DAC register contents are saved as long as power stays on the V_{DD} pin.
6	$\overline{RS}$	Resets Input and DAC Register to Zero Condition. Asynchronous active low input.
7–18	D0–D11	Twelve Parallel Input Data Bits. D11 = MSB Pin 18, D0 = LSB Pin 7, AD7396.
7, 8	NC	No Connect Pins 7 and 8 On the AD7397 Only.
9–18	D0–D9	Ten Parallel Input Data Bits. D9 = MSB Pin 18, D0 = LSB Pin 9, AD7397 Only.
19	$\overline{CS}$	Chip Select Latch Enable, Active Low.
20	A/$\overline{B}$	DAC Input Register Address Select DACA = 1 or DACB = 0.
21	$\overline{LDB}$	Load DAC B Register Strobe. Transfers input register data to the DAC B register. Active low inputs, Level sensitive latch. May be connected together with $\overline{LDA}$ to double-buffer load both DAC registers simultaneously.
22	V_{DD}	Positive Power Supply Input. Specified range of operation +2.7 V to +5.5 V.
23	V_{REF}	DAC Reference Input Pin. Establishes DAC full-scale voltage.
24	V_{OUTB}	DAC B Voltage Output.

PIN CONFIGURATIONS



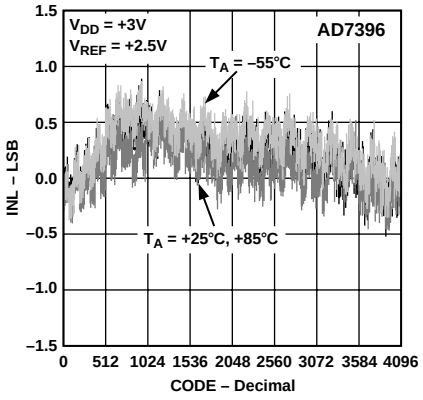


Figure 4. AD7396 INL vs. Code and Temperature

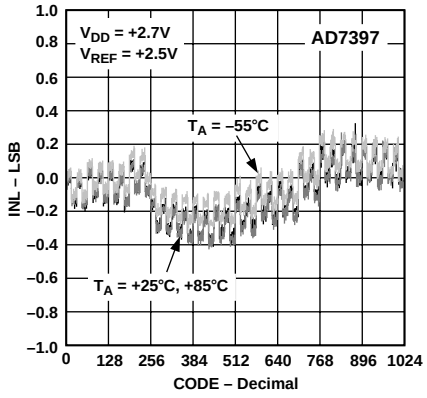


Figure 5. AD7397 INL vs. Code and Temperature

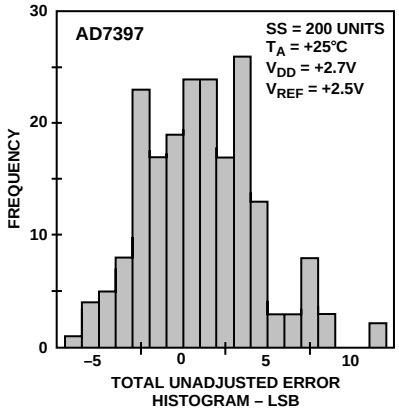


Figure 6. AD7397 TUE Histogram

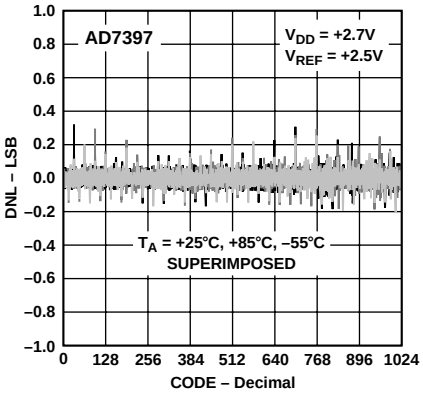


Figure 7. AD7397 DNL vs. Code and Temperature

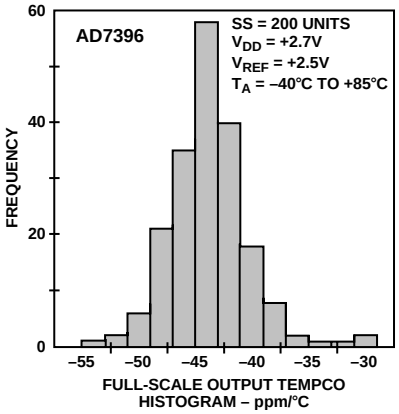


Figure 8. AD7396 Full-Scale Tempco Histogram

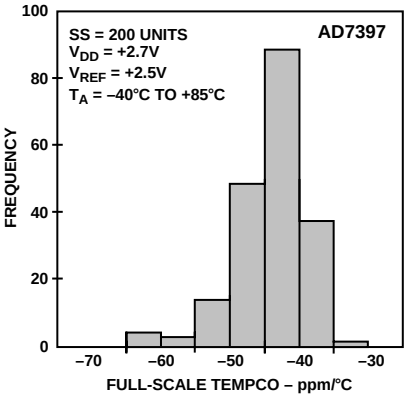


Figure 9. AD7397 Full-Scale Tempco Histogram

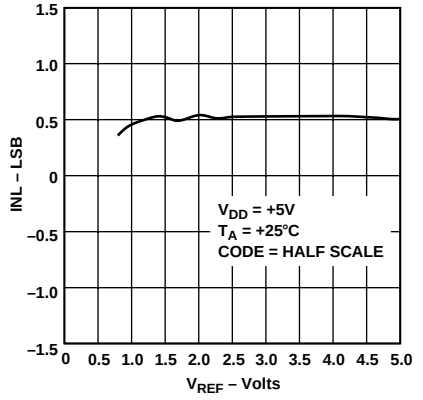


Figure 10. INL Error vs. Reference Voltage

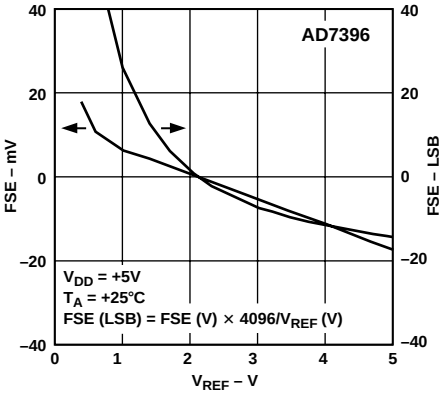


Figure 11. Full-Scale Error vs. Reference Voltage

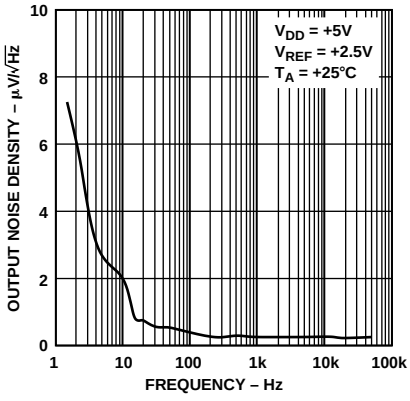


Figure 12. Output Noise Voltage Density vs. Frequency

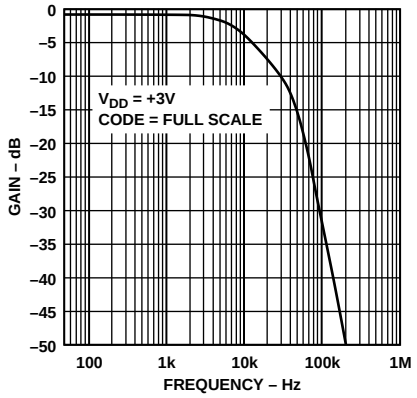


Figure 13. Reference Multiplying Gain vs. Frequency

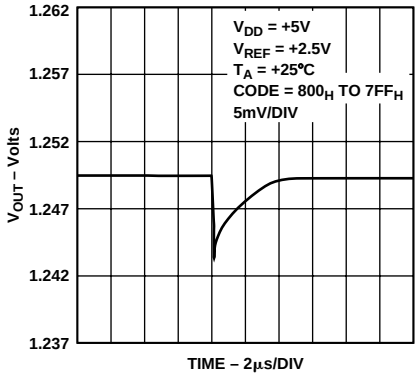


Figure 14. Midscale Transition Performance

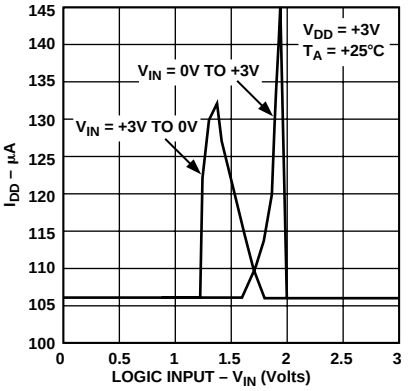


Figure 15. I_{DD} vs. Logic Input Voltage

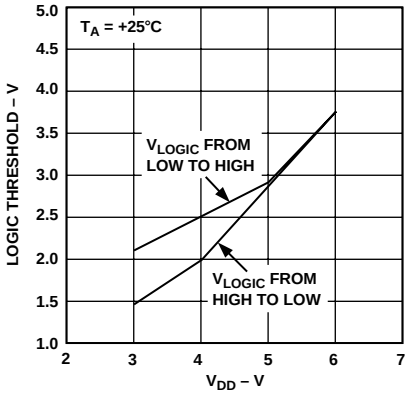


Figure 16. Logic Threshold Voltage vs. V_{DD}

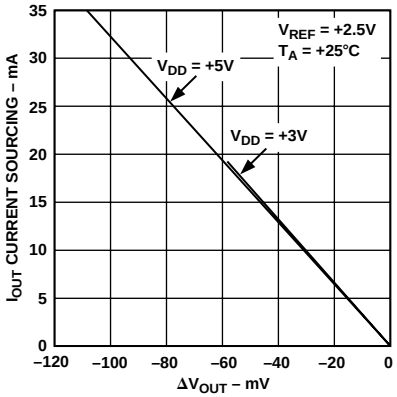


Figure 17. I_{OUT} Source Current vs. ΔV_{OUT}

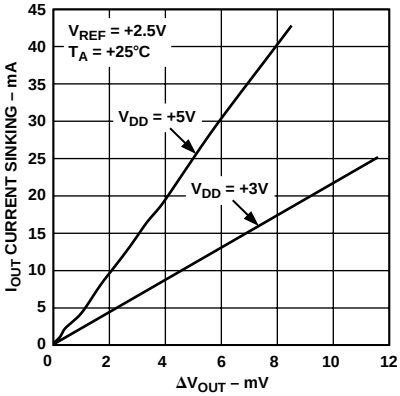


Figure 18. I_{OUT} Sink Current vs. ΔV_{OUT}

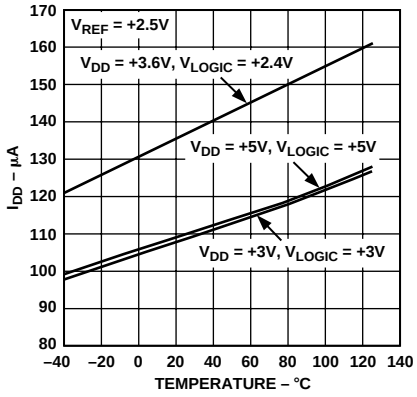


Figure 19. I_{DD} vs. Temperature

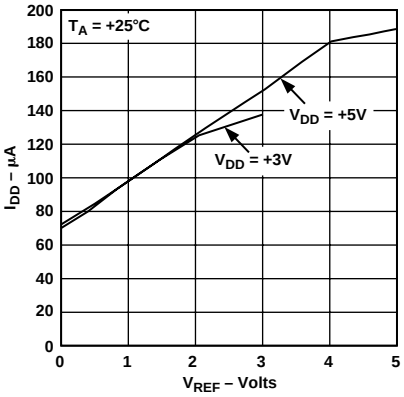


Figure 20. I_{DD} vs. Reference Voltage

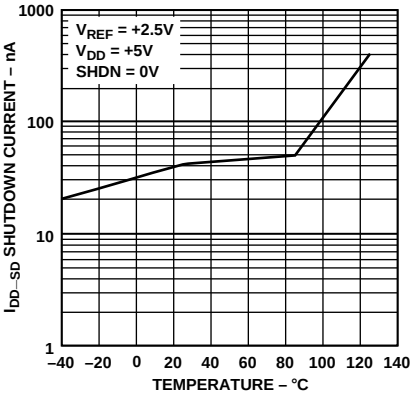


Figure 21. Shutdown Current vs. Temperature

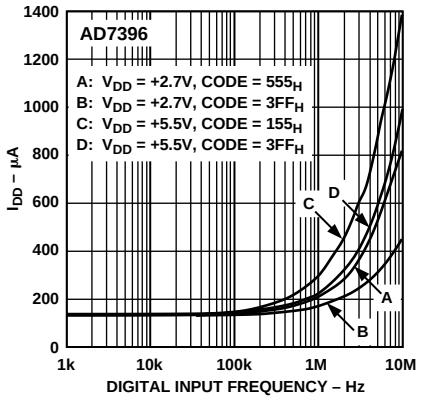


Figure 22. I_{DD} vs. Digital Input Frequency

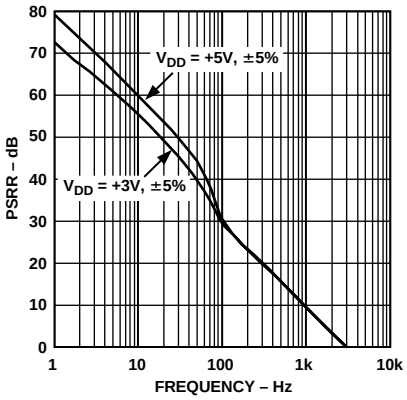


Figure 23. PSRR vs. Frequency

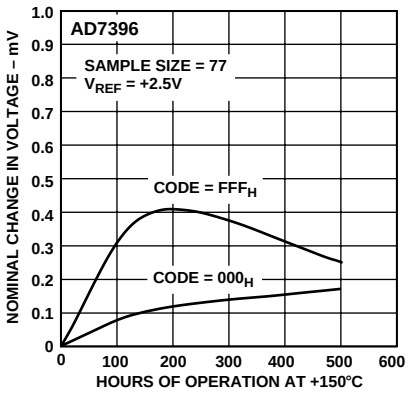


Figure 24. Long-Term Drift Accelerated by Burn-In

OPERATION

The AD7396 and AD7397 are a set of pin compatible, 12-bit and 10-bit digital-to-analog converters. These single-supply operation devices consume less than 200 µA of current while operating from power supplies in the +2.7 V to +5.5 V range, making them ideal for battery operated applications. They contain a voltage-switched, 12-bit/10-bit, digital-to-analog converter, rail-to-rail output op amps, and a parallel-input DAC register. The external reference input has constant 2.5 MΩ input resistance independent of the digital code setting of the DAC. In addition, the reference input can be tied to the same supply voltage as V_{DD} resulting in a maximum output voltage span of 0 to V_{DD}. The parallel data interface consists of 12 data bits, DB0–DB11, for the AD7396, 10 data bits, DB0–DB9, for the AD7397, and a $\overline{CS}$ write strobe. An $\overline{RS}$ pin is available to reset the DAC register to zero scale. This function is useful for power-on reset or system failure recovery to a known state. Additional power savings are accomplished by activating the $\overline{SHDN}$ pin resulting in a 1.5 µA maximum consumption sleep mode. As long as the supply voltage, remains data will be retained in the DAC and input register to supply the DAC output when the part is taken out of shutdown.

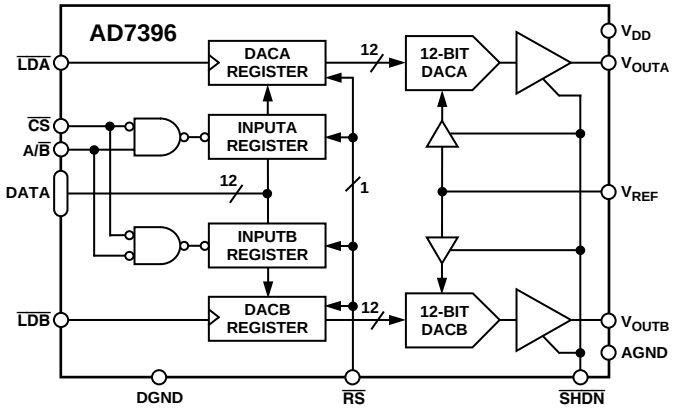


Figure 25. Functional Block Diagram

D/A CONVERTER SECTION

The voltage switched R-2R DAC generates an output voltage dependent on the external reference voltage connected to the REF pin according to the following equation:

$$V_{OUT} = V_{REF} \times D/2^N \quad (1)$$

where D is the decimal data word loaded into the DAC register, and N is the number of bits of DAC resolution. In the case of the 10-bit AD7397 using a 2.5 V reference, Equation 1 simplifies to:

$$V_{OUT} = 2.5 \times D/1024 \quad (2)$$

Using Equation 2, the nominal midscale voltage at V_{OUT} is 1.25 V for D = 512; full-scale voltage is 2.497 V. The LSB step size is = 2.5 × 1/1024 = 0.0024 V.

For the 12-bit AD7396 operating from a 5.0 V reference equation [1] becomes:

$$V_{OUT} = 5.0 \times D/4096 \quad (3)$$

Using Equation 3, the AD7396 provides a nominal midscale voltage of 2.50 V for D = 2048, and a full-scale output of 4.998 V. The LSB step size is = 5.0 × 1/4096 = 0.0012 V.

AMPLIFIER SECTION

The internal DAC's output is buffered by a low power consumption precision amplifier. The op amp has a 60 µs typical settling time to 0.1% of full scale. There are slight differences in settling time for negative slewing signals versus positive. Also, negative transition settling time to within the last 6 LSBs of zero volts has an extended settling time. The rail-to-rail output stage of this amplifier has been designed to provide precision performance while operating near either power supply. Figure 26 shows an equivalent output schematic of the rail-to-rail-amplifier with its N-channel pull-down FETs that will pull an output load directly to GND. The output sourcing current is provided by a P-channel pull-up device that can source current to GND terminated loads.

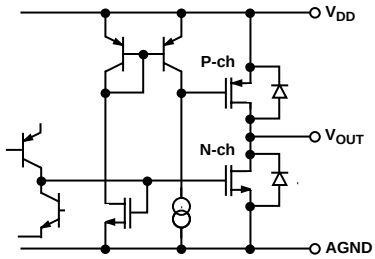


Figure 26. Equivalent Analog Output Circuit

The rail-to-rail output stage provides ±1 mA of output current. The N-channel output pull-down MOSFET shown in Figure 26 has a 35 Ω ON resistance, which sets the sink current capability near ground. In addition to resistive load driving capability, the amplifier has also been carefully designed and characterized for up to 100 pF capacitive load driving capability.

REFERENCE INPUT

The reference input terminal has a constant input resistance independent of digital code, which results in reduced glitches on the external reference voltage source. The high 2.5 MΩ input resistance minimizes power dissipation within the AD7396/AD7397 D/A converters. The V_{REF} input accepts input voltages ranging from ground to the positive-supply voltage V_{DD}. One of the simplest applications, which saves an external reference voltage source, is connection of the V_{REF} terminal to the positive V_{DD} supply. This connection results in a rail-to-rail voltage output span maximizing the programmed range. The reference input will accept AC signals as long as they are kept within the supply voltage range, $0 < V_{REF\ IN} < V_{DD}$. The reference bandwidth and integral nonlinearity error performance are plotted in the Typical Performance Characteristics section, see Figures 10 and 13. The ratiometric reference feature makes the AD7396/AD7397 an ideal companion to ratiometric analog-to-digital converters such as the AD7896.

POWER SUPPLY

The very low power consumption of the AD7396/AD7397 is a direct result of a circuit design optimizing the use of a CBCMOS process. By using the low power characteristics of CMOS for the logic, and the low noise, tight matching of the complementary bipolar transistors, excellent analog accuracy is achieved. One advantage of the rail-to-rail output amplifiers used in the AD7396/AD7397 is the wide range of usable supply voltage. The part is fully specified and tested for operation from +2.7 V to +5.5 V.

POWER SUPPLY BYPASSING AND GROUNDING

Precision analog products such as the AD7396/AD7397 require a well filtered power source. Since the AD7396/AD7397 operates from a single +3 V to +5 V supply, it seems convenient to simply tap into the digital logic power supply. Unfortunately, the logic supply is often a switch-mode design, which generates noise in the 20 kHz to 1 MHz range. In addition, fast logic gates can generate glitches, hundred of millivolts in amplitude, due to wiring resistance and inductance. The power supply noise generated thereby means that special care must be taken to assure that the inherent precision of the DAC is maintained. Good engineering judgment should be exercised when addressing the power supply grounding and bypassing of the 12-bit AD7396.

The AD7396 should be powered directly from the system power supply. Whether or not a separate power supply trace is available generous supply bypassing will reduce supply line-induced errors. Local supply bypassing consisting of a 10 µF tantalum electrolytic in parallel with a 0.1 µF ceramic capacitor is recommended in all applications (Figure 27).

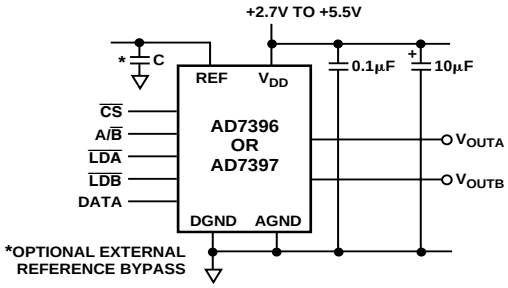


Figure 27. Recommended Supply Bypassing

INPUT LOGIC LEVELS

All digital inputs are protected with a Zener-type ESD protection structure (Figure 28) that allows logic input voltages to exceed the V_{DD} supply voltage. This feature can be useful if the user is driving one or more of the digital inputs with a 5 V CMOS logic input-voltage level while operating the AD7396/AD7397 on a +3 V power supply. If this mode of interface is used, make sure that the V_{OL} of the 5 V CMOS meets the V_{IL} input requirement of the AD7396/AD7397 operating at 3 V. See Figure 16 for a graph for digital logic input threshold versus operating V_{DD} supply voltage.

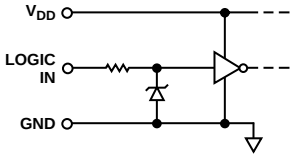


Figure 28. Equivalent Digital Input ESD Protection

In order to minimize power dissipation from input-logic levels that are near the V_{IH} and V_{IL} logic input voltage specifications, a Schmitt trigger design was used that minimizes the input-buffer current consumption compared to traditional CMOS input stages. Figure 15 shows a plot of incremental input voltage versus supply current showing that negligible current consumption takes place when logic levels are in their quiescent state. The normal crossover current still occurs during logic transitions. A secondary advantage of this Schmitt trigger is the prevention of false triggers that would occur with slow moving logic transitions when a standard CMOS logic interface or opto-isolators are used. The logic inputs DB11–DB0, A/$\overline{B}$ $\overline{CS}$, $\overline{RS}$, $\overline{SHDN}$ all contain Schmitt trigger circuits.

DIGITAL INTERFACE

The AD7396/AD7397 has a double-buffered, parallel-data input. A functional block diagram of the digital section is shown in Figure 25, while Table I contains the truth table for the logic control inputs. The chip select ($\overline{CS}$) and A/$\overline{B}$ pins control loading of data from the data inputs on pins DB11–DB0 into the internal Input Register. The $\overline{CS}$ active low input places data into the decoded A/$\overline{B}$ input register. When $\overline{CS}$ returns to logic high within the data setup-and-hold time specifications the new value of data in the input register will be latched. See Truth Table for complete set of conditions. New data can only be transferred to the corresponding DAC register when its LDx pin is strobed active low. The LDx inputs are level-sensitive (DAC Registers are transparent latches) and can be tied active low

allowing any new Input Register data updates to directly control the DAC output voltages for single-buffered applications. For doubled-buffered applications where both DAC outputs, V_{OUTA} and V_{OUTB}, need to be changed simultaneously to a new value, the two inputs, $\overline{LDA}$ and $\overline{LDB}$, can be tied together and pulsed active low in a synchronous manner.

RESET ($\overline{RS}$) PIN

Forcing the asynchronous $\overline{RS}$ pin low will set the Input and DAC registers to all zeros and the DAC output voltage will be zero volts. The reset function is useful for setting the DAC outputs to zero at power-up or after a power supply interruption. Test systems and motor controllers are two of many applications that benefit from powering up to a known state. The external reset pulse can be generated by the microprocessor's power-on RESET signal, from the microprocessor, or by an external resistor and capacitor. RESET has a Schmitt trigger input which results in a clean reset function when using external resistor/capacitor generated pulses. See Table I, Control-Logic Truth.

POWER SHUTDOWN ($\overline{SHDN}$)

Maximum power savings can be achieved by using the power shutdown control function. This hardware-activated feature is controlled by the active low input $\overline{SHDN}$ pin. This pin has a Schmitt trigger input which helps to desensitize it to slowly changing inputs. By placing a logic low on this pin the internal consumption of the AD7397 or AD7397 is reduced to nanoamp levels, guaranteed to 1.5 μA maximum over the operating temperature range. If power is present at all times on the V_{DD} pin while in the shutdown mode, the internal DAC register will retain the last programmed data value. This data will be used when the part is returned to the normal active state by placing the DAC back to its programmed voltage setting. Shutdown recovery time measures 80 μs. In the shutdown state the DAC output amplifier exhibits an open-circuit high-resistance state. Any load connected will stabilize at its termination voltage. If the power shutdown feature is not needed then the user should tie the $\overline{SHDN}$ pin to the V_{DD} voltage thereby disabling this function.

UNIPOLAR OUTPUT OPERATION

This is the basic mode of operation for the AD7396. As shown in Figure 29, the AD7396 has been designed to drive loads as low as 5 kΩ in parallel with 100 pF. The code table for this operation is shown in Table II.

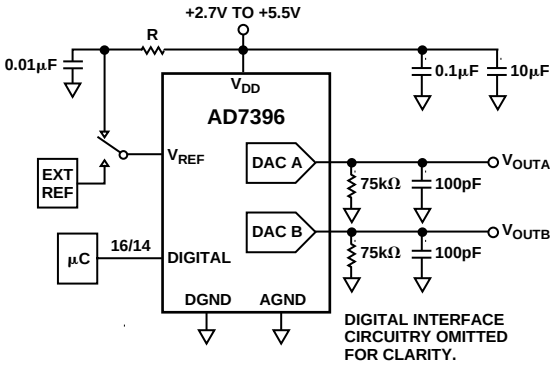


Figure 29. Unipolar Output Operation

Table II. Unipolar Code Table

Hexadecimal Number In DAC Register	Decimal Number In DAC Register	Output Voltage (V) (V_{REF} = 2.5 V)
FFF	4095	2.4994
801	2049	1.2506
800	2048	1.2500
7FF	2047	1.2494
000	0	0

The circuit can be configured with an external reference plus power supply, or powered from a single dedicated regulator or reference, depending on the application performance requirements.

BIPOLAR OUTPUT OPERATION

Although the AD7397 has been designed for single supply operation, the output can easily be configured for bipolar operation. A typical circuit is shown in Figure 30. This circuit uses a clean regulated +5 V supply for power, which also provides the circuit's reference voltage. Since the AD7397 output span swings from ground to very near +5 V, it is necessary to choose an external amplifier with a common-mode input voltage range that extends to its positive supply rail. The micropower consumption OP196 has been designed just for this purpose and results in only 50 μA of maximum current consumption. Connection of the equal-value 470 kΩ resistors results in a differential amplifier mode of operation with a voltage gain of two, which produces a circuit output span of ten volts, that is, –5 V to +5 V. As the AD7397 DAC is programmed from zero-code 000_H to midscale 200_H to full-scale $3FF_H$, the circuit output voltage V_O is set at –5 V, 0 V and +5 V (–1 LSB). The output voltage V_O is coded in offset binary according to Equation 3.

$$V_{OUT} = [(D/512)–1] \times 5 \quad (4)$$

where D is the decimal code loaded in the AD7397 DAC register. Note that the LSB step size is 10/1024 = 10 mV. This circuit has been optimized for micropower consumption including the 470 kΩ gain setting resistors, which should have low temperature coefficients to maintain accuracy and matching (preferably the same resistor material, such as metal film). If better stability is required, the power supply could be substituted with a precision reference voltage such as the low dropout REF195, which can easily supply the circuit's 262 μA of current and still provide additional power for the load connected to V_O. The micropower REF195 is guaranteed to source 10 mA output drive current, but consumes only 50 μA internally. If higher resolution is required, the AD7396 can be used with the addition of two more bits of data inserted into the software coding, which would result in a 2.5 mV LSB step size. Table III shows examples of nominal output voltages, V_O, provided by the bipolar operation circuit application.

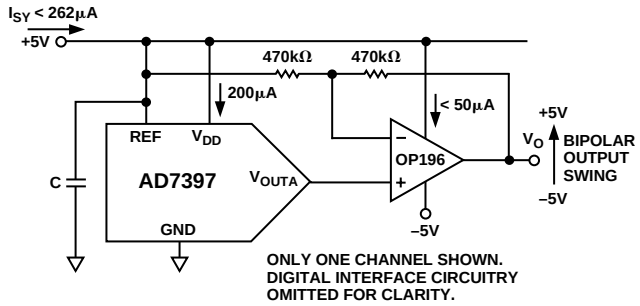


Figure 30. Bipolar Output Operation

Table III. Bipolar Code Table

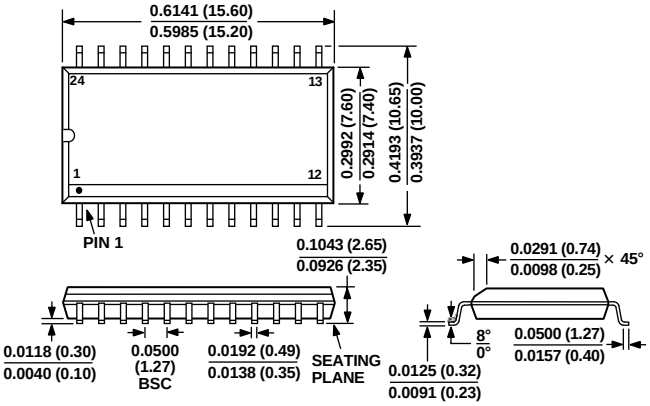
Hexadecimal Number In DAC Register	Decimal Number In DAC Register	Analog Output Voltage (V)
3FF	1023	4.9902
201	513	0.0097
200	512	0.0000
1FF	511	–0.0097
000	0	–5.0000

C3425–8–10/98

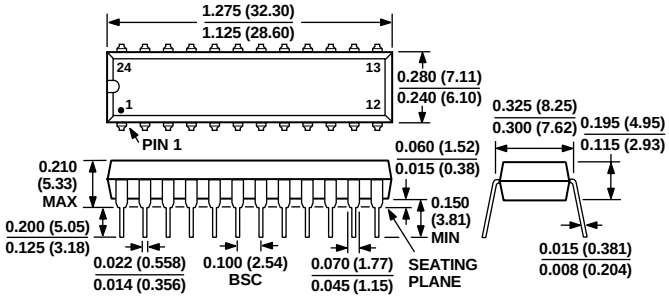
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

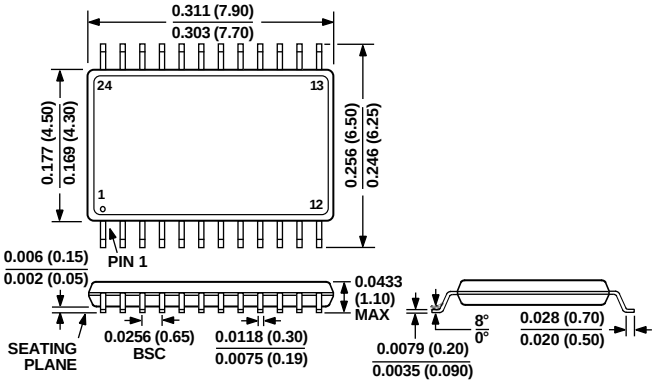
24-Lead SOIC Package
(R-24)



24-Lead Narrow Body Plastic DIP Package
(N-24)



24-Lead Thin Surface Mount TSSOP Package
(RU-24)



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