AN3321K, AN3321S

VTR Playback Video Signal Processing Circuits

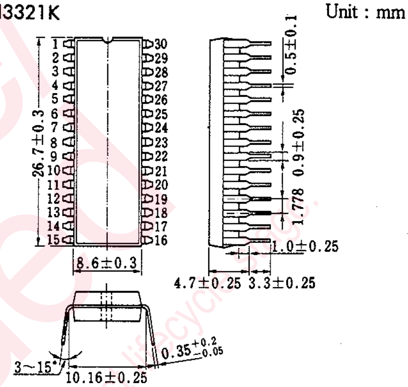
■ Outline

The AN3321K and the AN3321S are integrated circuits designed for VTR playback video signal processing circuits.

■ Features

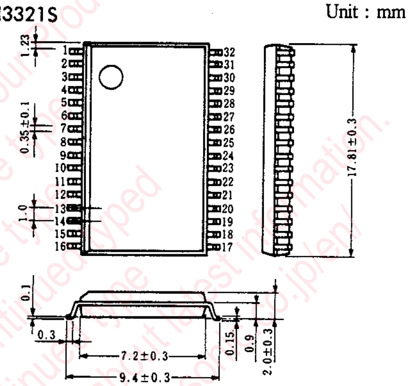
- Operated by low supply power voltage : V_{CC}=5V
- Built-in line noise canceler circuit.
- Built-in picture control circuit

AN3321K Unit : mm



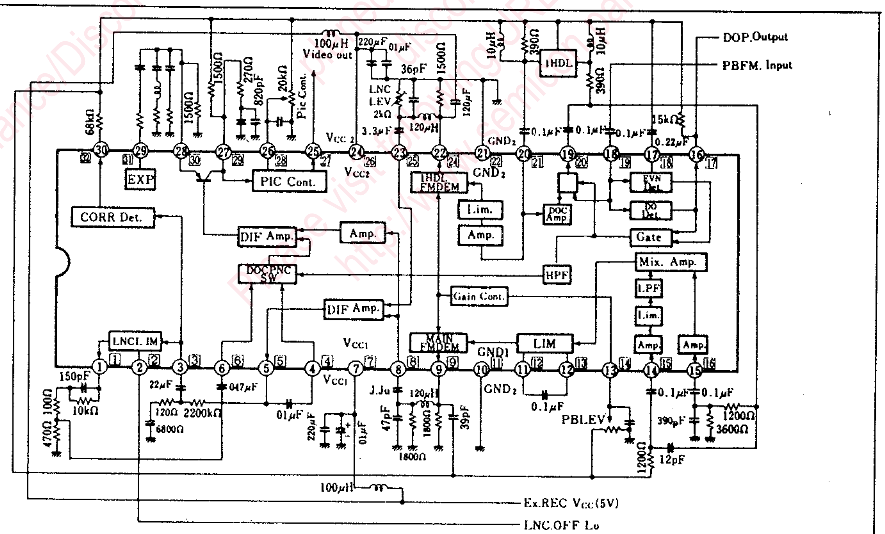
30-Lead Shrunk DIL Plastic Package

AN3321S Unit : mm



32-Lead PANAFLAT Package (VSO-32D)

■ Block Diagram



□Shows the Pin No. of AN3321S

■ Absolute Maximum Ratings (Ta=25℃)

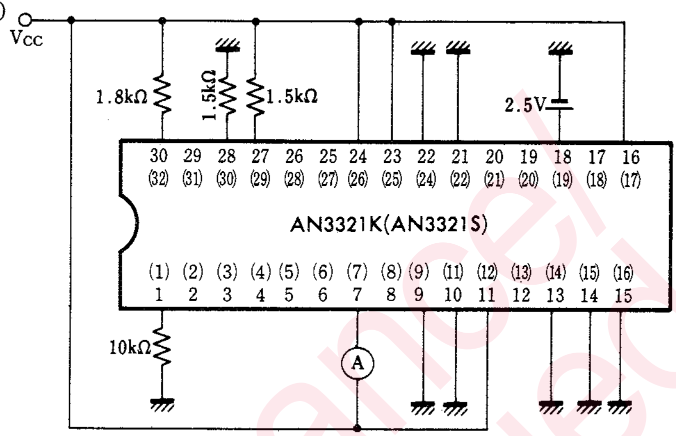
Item		Symbol	Rating	Unit
Supply Voltage		V_{CC}	6	V
Power Dissipation (Ta=70℃)		P_D	280	mW
Operating Ambient Temperature		T_{opr}	−20~+70	℃
Storage Temperature	AN3321K	T_{stg}	−55~+150	℃
	AN3321S		−55~+125	

■ Electrical Characteristics (V_{CC}=5V, Ta=25℃)

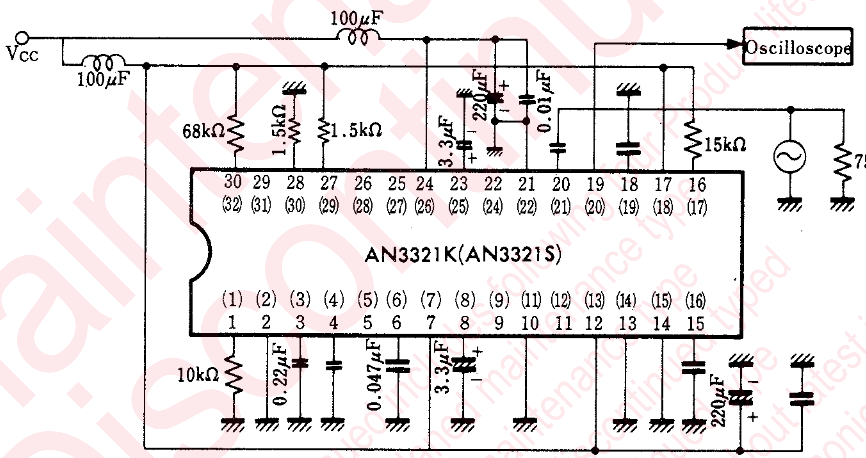
Item		Symbol	Test Circuit	Condition	min.	typ.	max.	Unit
Circuit Current		I_7	1		23		36	mA
DOC Amp. Gain	AN3321K	G_{19}	2	Pin ⑳ Input (60mV_{P-P}, 4MHz)	13		16	dB
	AN3321S	G_{20}						
DOC Sensitivity ON	AN3321K	S_{16}	3	Pin ⑱ Input (4MHz) 0dB=350mV_{P-P}	−14.8		−11.3	dB
	AN3321S	S_{17}						
DOC Sensitivity OFF (Hysteresis)	AN3321K	ΔS_{16}	3	Pin ⑱ Input (4MHz) 0dB=350mV_{P-P}	−5		−0.5	dB
	AN3321S	ΔS_{17}						
Sub FM Demodulation Det. Sensitivity	AN3321K	S_{22}	4	Pin ⑳ Input (50mV_{P-P}) 0dB=250mV_{P-P}	2.5			dB
	AN3321S	S_{24}						
Sub FM Demodulation Det. Limitation	AN3321K	L_{f22}	4	Pin ⑳ Input (50mV_{P-P})	7			MHz
	AN3321S	L_{f24}						
Main FM Demodulation Det. Sensitivity		S_9	5	Pin ⑮ Input (150mV_{P-P}) 0dB=250mV_{P-P}	2.5			dB
Main FM Demodulation Det. Limitation		L_{f9}	5	Pin ⑮ Input (150mV_{P-P})	7			MHz
Difference Det. Amp. Gain A		G_{5-1}	6	Pin ㉓ Input (100mV_{P-P}, 1MHz)	14.3		17.3	dB
Difference Det. Amp. Gain B		G_{5-2}	6	Pin ⑧ Input (100mV_{P-P}, 1MHz)	12.8		15.8	dB
Differential+ MIX Amp. Gain	AN3321K	G_{25-1}	7	Pin ⑧ Input (100mV_{P-P}, 1MHz)	7.6		10.6	dB
	AN3321S	G_{27-1}						
MIX Amp. Ratio	AN3321K	G_{28}	7	Pin ⑥ Input V_{CC}=4.3V (500mV_{P-P}, 1MHz)	−5		−2	dB
	AN3321S	G_{30}						
Line Noise Canceler Switch Changeover Level Difference	AN3321K	ΔV_{28}	8	Pin⑰ Control pulse (5V/0V, 125KHz)	−5		5	mV
	AN3321S	ΔV_{30}						
Line Noise Canceler Switch Crosstalk	AN3321K	CT_{28}	9	Pin ④, Pin ⑥ Input (500mV_{P-P}, 1MHz)			−40	dB
	AN3321S	CT_{30}						
Line Noise Canceler Limiter Gain		G_1	10	Pin ③ Input (40mV_{P-P}, 1MHz)	16.3		19.8	dB
Picture Control Gain	AN3321K	G_{25-2}	11	Pin ㉗ Input (250mV_{P-P}, 1MHz)	−1.5		0.5	dB
	AN3321S	G_{27-2}						
Picture Control Frequency Characteristics A	AN3321K	f_{25-1}	11	Pin ㉗ Input (250mV_{P-P}, 1MHz)			−0.5	dB
	AN3321S	f_{27-1}						
Picture Control Frequency Characteristics B	AN3321K	f_{25-2}	11	Pin ㉗ Input (250mV_{P-P}, 1MHz)	4			dB
	AN3321S	f_{27-2}						

Note : Operating Supply voltage range $V_{CC(opr)}$=4.5~5.5V

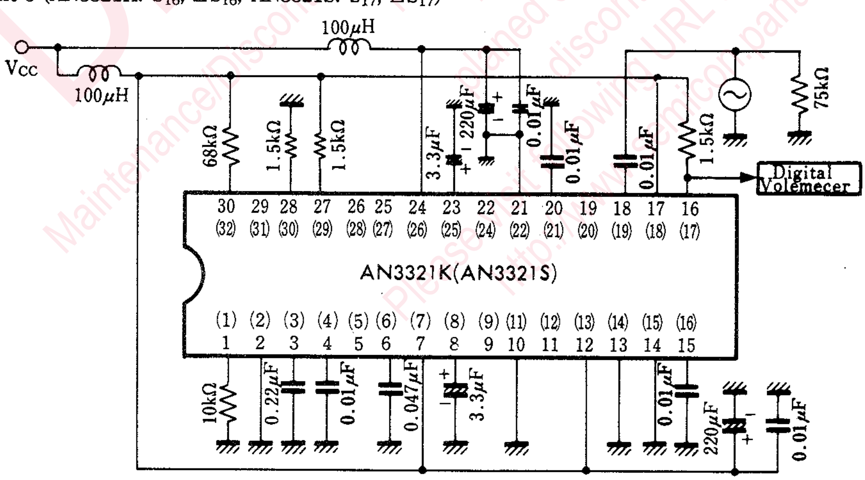
Test Circuit 1 (I_7)



Test Circuit 2 (AN3321K: G_{19}, AN3321S: G_{20})



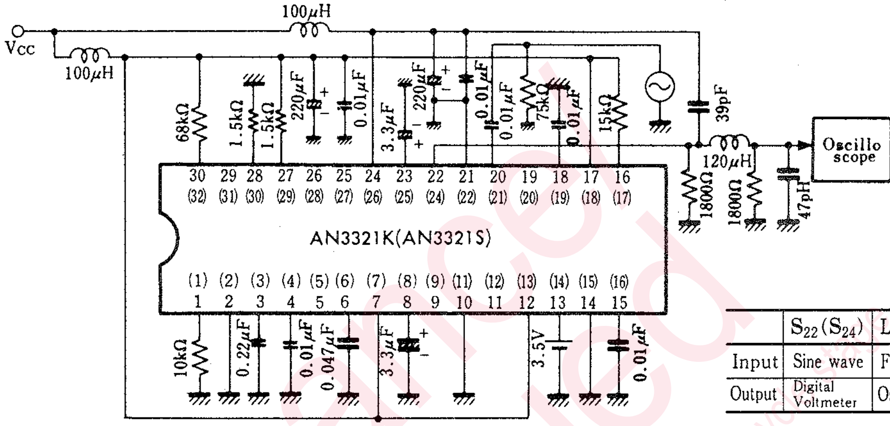
Test Circuit 3 (AN3321K: S_{16}, ΔS_{16}, AN3321S: S_{17}, ΔS_{17})



- $S_{16}(S_{17})$: Input level when Pin ⑯ output becomes Lo
- $\Delta S_{16}(\Delta S_{17})$: Differnce between input level and value above Pin ⑯ output

( ) show the Pin No. of AN3321S

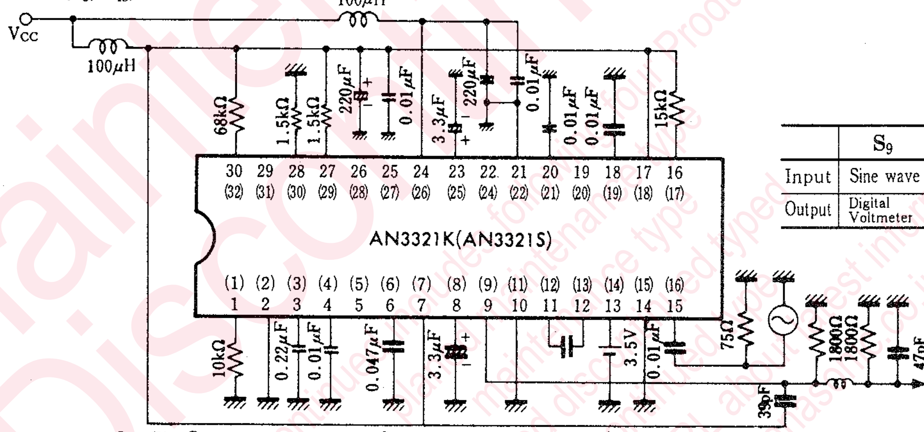
Test Circuit 4 (AN3321K: S_{22}, L_{f22}, AN3321S: S_{24}, L_{f24})



	S_{22} (S_{24})	Lf_{22} (Lf_{24})
Input	Sine wave	FM sweep
Output	Digital Voltmeter	Oscilloscope

- S_{22}(S_{24}) : Pin ㉒ (Pin ㉔) output difference of ⑳ (㉑) input frequency: 3.5MHz／4.5MHz is multiplied by F11 (differential+Mix. amp. gain).
- Lf_{22}, (Lf_{24}) : Pin ⑳ (㉑) input limit frequency when pin ㉒ (㉔) output is changed into linear.

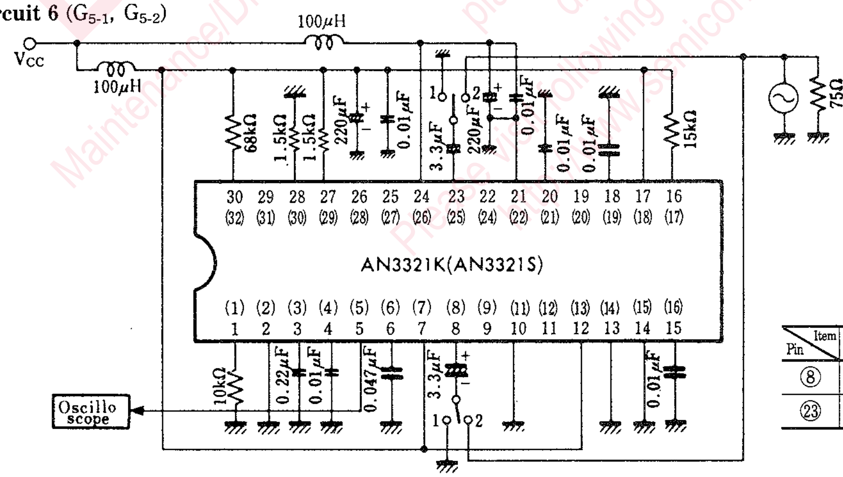
Test Circuit 5 (S_9, L_{f9})



	S_9	Lf_9
Input	Sine wave	FM sweep
Output	Digital Voltmeter	Oscilloscope

- S_9 : Pin ⑮ output difference of ⑨ input frequency 3.5MHz／4.5MHz is multiplied by F11 (differential+Mix. amp. gain).
- Lf_9, : Pin ⑨ input limit frequency when pin ⑮ output is changed into linear.

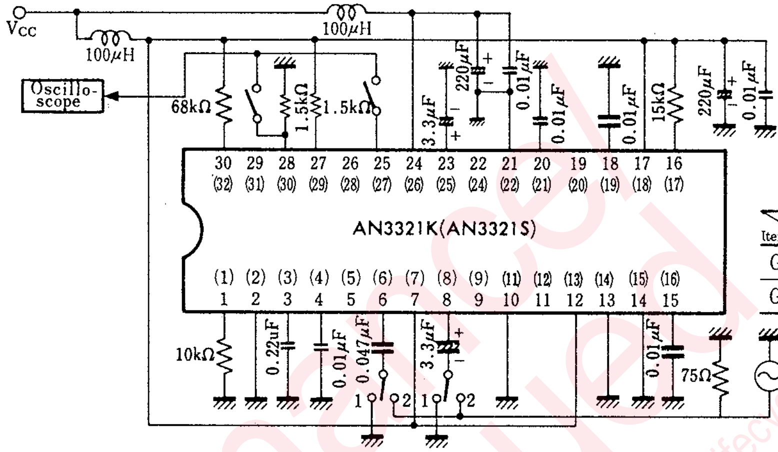
Test Circuit 6 (G_{5-1}, G_{5-2})



Pin \ Item	G_{5-1}	G_{5-2}
⑧	1	2
㉓	2	1

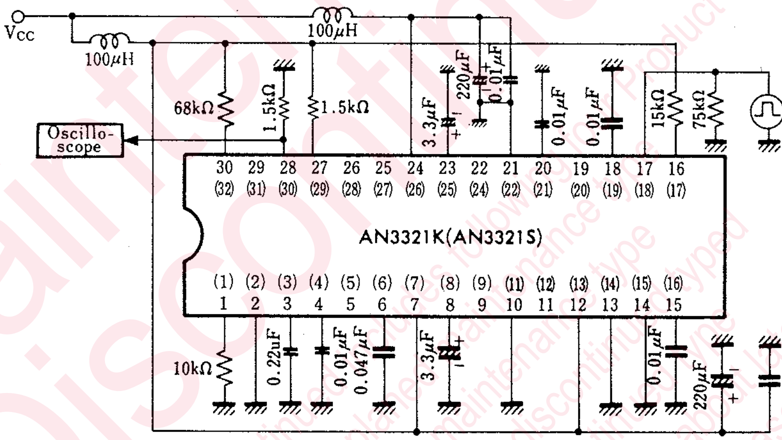
( ) shows the Pin. No. of AN3321S.

Test Circuit 7 (AN3321K: G_{25-1}, G_{28}, AN3321S: G_{27-1}, G_{30})

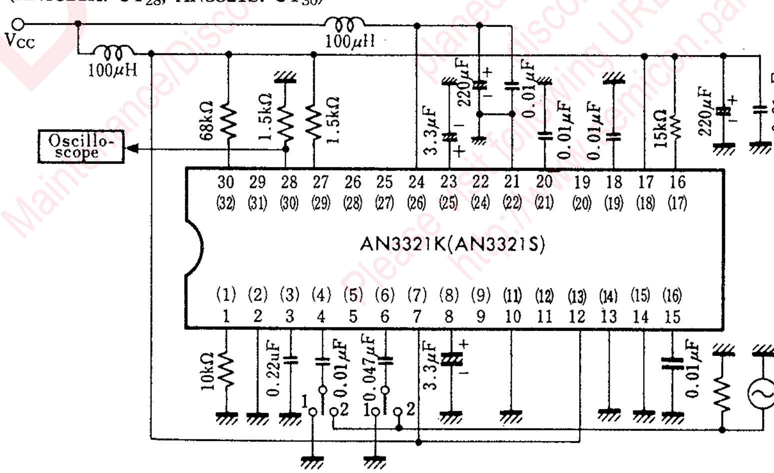


Item \ Pin	⑥	⑧	Output Pin
G_{25-1}	1	2	㉕
G_{28}	2	1	㉘

Test Circuit 8 (AN3321K: ΔV_{28}, AN3321S: ΔV_{30})



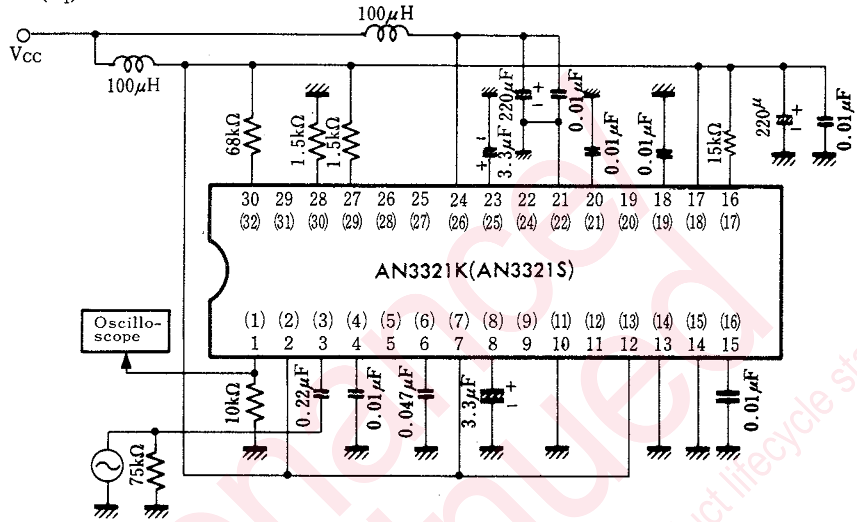
Test Circuit 9 (AN3321K: CT_{28}, AN3321S: CT_{30})



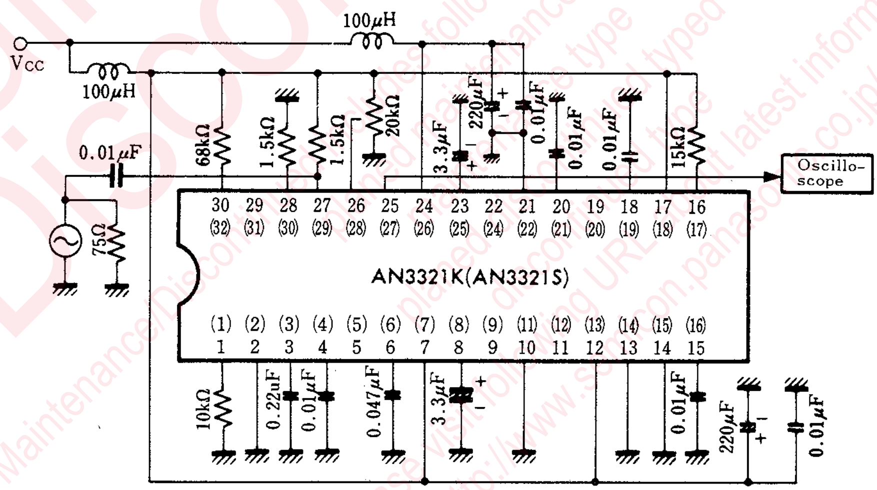
- CT_{28}(CT_{30}) : f element ratio for Pin ④ input to Pin ㉘ (㉚) output f element for Pin ⑥

( ) Shows the Pin No. of AN3321S.

Test Circuit 10 (G_1)



Test Circuit 11 (AN3321K: $G_{25\text{-}2}$, $f_{25\text{-}1}$, $f_{25\text{-}2}$, AN3321S: $G_{27\text{-}2}$, $f_{27\text{-}1}$, $f_{27\text{-}2}$)



	G_{25-2}	f_{25-1}	f_{25-2}
㉖Electric Potential	2.5V	0V	5.0V

( ) show the Pin No. of AN3321S

■ Pin

AN3321K

Pin No.	Pin Name	Pin No.	Pin Name
1	Line N.C. LIM. Output	16	DOC Pulse Output
2	2H/4, 6H Select	17	Envelop Det.
3	Line N.C. LIM Input	18	RF Input
4	Diff. Sig. Input	19	RF Output
5	Diff. Sig. Output	20	1H Delay RF Input
6	Limited Sig. Input	21	GND2
7	To Except Rec V_{cc1}	22	DEM. (1H DL)Output
8	Video Input	23	Video(1H DL)Input
9	DEM. Output	24	To Except Rec V_{cc2}
10	GND1	25	Video Output
11	LIM.	26	Picture Control
12	LIM.	27	De-emphasis
13	DEM. Gain Control	28	Peaking
14	Double LIM. HPF Input	29	Extension
15	Double LIM. LPF Input	30	Relative Delecting Pulse Output

AN3321S

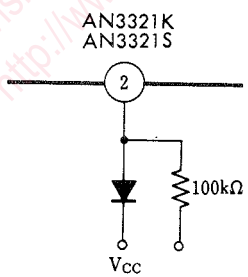
Pin No.	Pin Name	Pin No.	Pin Name
1	Line N.C. LIM. Output	17	DOC Pulse Output
2	2H/4, 6H Select	18	Envelop Det.
3	Line N.C. LIM. Input	19	RF Input
4	Diff. Sig. Input	20	RF Output
5	Diff. Sig. Output	21	1H Delay RF Input
6	Limited Sig. Input	22	GND2
7	To Except Rec V_{cc1}	23	NC
8	Video Input	24	DEM. (1H DL)Output
9	DEM. Output	25	Video(1H DL)Input
10	NC	26	To Except Rec V_{cc2}
11	GND1	27	Video Output
12	LIM.	28	Picture Control
13	LIM.	29	De-emphasis
14	DEM. Gain Control	30	Peaking
15	Double LIM. HPF Input	31	Extension
16	Double LIM. LPF Input	32	Relative Detecting Pulse Output

Note 1: Power supply to be supplied to Pins ⑬ and ⑳ (Pins ⑭ and ㉘ for AN3321S) should be used the same as that supplied to Pin ⑦ of this integrated circuit.

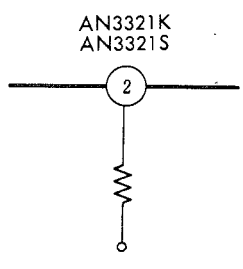
Note 2: If any influence is exerted when this IC is used with power supply furnished for recording, some measures such as cutting off power, etc. should be taken for use.

Note 3: When using this IC with power supply off for recording, make Pin ② Low level during recording, connet the diodes to Pin ② in the opposite direction (see Fig. 1), or connect the external resistor of 47Ω～470kΩ to Pin ② (see Fig. 2 for V_{cc}=5V).

(Fig. 1)



(Fig. 2)



Note 4 : Since deterioration of destroy of characteristics due to flow of overcurrent caused by the inverting current, careful attention should be taken to handling.

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