

# BULD50KC, BULD50SL NPN SILICON TRANSISTOR WITH INTEGRATED DIODE

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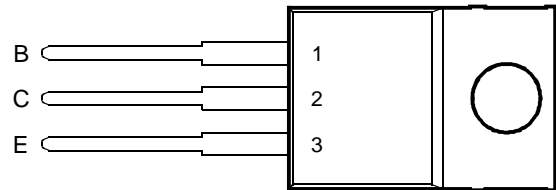
FEBRUARY 1994 - REVISED SEPTEMBER 1997

- **Designed Specifically for High Frequency Electronic Ballasts**
- **Integrated Fast  $t_{rr}$  Anti-Parallel Diode, Enhancing Reliability**
- **Diode  $t_{rr}$  Typically 1  $\mu$ s**
- **New Low-Height SL Power Package, TO220 Pin-Compatible**
- **Tightly Controlled Transistor Storage Times**
- **Voltage Matched Integrated Transistor and Diode**
- **Characteristics Optimised for Cool Running**
- **Diode-Transistor Charge Coupling Minimised to Enhance Frequency Stability**

## description

The new BULDxx range of transistors have been designed specifically for use in High Frequency Electronic Ballasts (HFEB's). This range of switching transistors has tightly controlled storage times and an integrated fast  $t_{rr}$  anti-parallel diode. The revolutionary design ensures that the diode has both fast forward and reverse recovery times, achieving the same performance as a discrete anti-parallel diode plus transistor. The integrated diode has minimal charge coupling with the transistor, increasing frequency stability, especially in lower power circuits where the circulating currents are low. By design, this new device offers a voltage matched integrated transistor and anti-parallel diode.

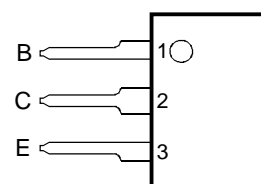
**TO-220 PACKAGE  
(TOP VIEW)**



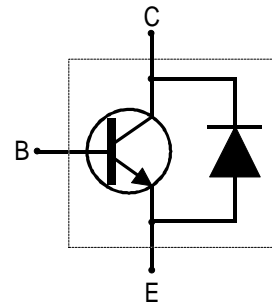
Pin 2 is in electrical contact with the mounting base.

MDTRACA

**SL PACKAGE  
(TOP VIEW)**



## device symbol



## absolute maximum ratings at 25°C † (unless otherwise noted)

RATING		SYMBOL	VALUE	UNIT
Collector-emitter voltage ( $V_{BE} = 0$ )		$V_{CES}$	600	V
Collector-base voltage ( $I_E = 0$ )		$V_{CBO}$	600	V
Collector-emitter voltage ( $I_B = 0$ )		$V_{CEO}$	400	V
Emitter-base voltage		$V_{EBO}$	9	V
Continuous collector current	BULD50KC BULD50SL (see Note 1)	$I_C$	3.5	A
Peak collector current (see Note 2)		$I_{CM}$	6	A
Continuous base current	BULD50KC BULD50SL (see Note 1)	$I_B$	1.5	A
Peak base current (see Note 2)		$I_{BM}$	2.5	A

NOTES: 1. This value applies for  $t_p = 1$  s.

2. This value applies for  $t_p = 10$  ms, duty cycle  $\leq 2\%$ .

†  $\leq 25^\circ\text{C}$  case temperature for BULD50KC, and  $\leq 25^\circ\text{C}$  ambient temperature for BULD50SL

## PRODUCT INFORMATION

Information is current as of publication date. Products conform to specifications in accordance with the terms of Power Innovations standard warranty. Production processing does not necessarily include testing of all parameters.



# BULD50KC, BULD50SL

## NPN SILICON TRANSISTOR WITH INTEGRATED DIODE

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### absolute maximum ratings at 25°C † (unless otherwise noted) (continued)

RATING	SYMBOL	VALUE	UNIT
Continuous device dissipation	$P_{tot}$	50 see Figure 11	W
Maximum average continuous diode forward current	$I_{E(av)}$	0.5	A
Operating junction temperature range	$T_j$	-65 to +150	°C
Storage temperature range	$T_{stg}$	-65 to +150	°C

### electrical characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CE(sus)}$ Collector-emitter sustaining voltage	$I_C = 100\text{ mA}$ $L = 25\text{ mH}$	400			V
$I_{CES}$ Collector-emitter cut-off current	$V_{CE} = 600\text{ V}$ $V_{BE} = 0$			10	μA
$I_{EBO}$ Emitter cut-off current	$V_{EB} = 9\text{ V}$ $I_C = 0$			1	mA
$V_{BE(sat)}$ Base-emitter saturation voltage	$I_B = 150\text{ mA}$ $I_C = 750\text{ mA}$ (see Notes 3 and 4)		0.9	1.1	V
$V_{CE(sat)}$ Collector-emitter saturation voltage	$I_B = 150\text{ mA}$ $I_B = 300\text{ mA}$ $I_C = 750\text{ mA}$ $I_C = 1.5\text{ A}$ (see Notes 3 and 4)		0.2 0.4	0.5 1	V
$h_{FE}$ Forward current transfer ratio	$V_{CE} = 10\text{ V}$ $V_{CE} = 1\text{ V}$ $V_{CE} = 5\text{ V}$ $I_C = 10\text{ mA}$ $I_C = 750\text{ mA}$ $I_C = 1.5\text{ A}$ (see Notes 3 and 4)	10 10 10	17 15 15	20 20 20	
$V_{EC}$ Anti-parallel diode forward voltage	$I_E = 1\text{ A}$ (see Notes 3 and 4)		1.25	1.5	V
$t_{rr}$ Anti-parallel diode reverse recovery time	(see Note 5)		1		μs

NOTES: 3. These parameters must be measured using pulse techniques,  $t_p = 300\text{ μs}$ , duty cycle  $\leq 2\%$ .

4. These parameters must be measured using voltage-sensing contacts, separate from the current carrying contacts, and located within 3.2 mm from the device body.

5. Tested in a typical High Frequency Electronic Ballast.

### thermal characteristics

PARAMETER	MIN	TYP	MAX	UNIT
$R_{\theta JA}$ Junction to free air thermal resistance			62.5 115	°C/W
$R_{\theta JC}$ Junction to case thermal resistance			2.5	°C/W

### inductive-load switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{sv}$ Storage time	$I_C = 750\text{ mA}$ $L = 1\text{ mH}$ $I_{B(on)} = 150\text{ mA}$ $I_{B(off)} = 150\text{ mA}$ $V_{CC} = 40\text{ V}$ $V_{CLAMP} = 300\text{ V}$		3.35	4.5	μs

### resistive-load switching characteristics at 25°C case temperature

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{fi}$ Current fall time	$I_C = 750\text{ mA}$ $V_{CC} = 300\text{ V}$ $I_{B(on)} = 150\text{ mA}$ $I_{B(off)} = 150\text{ mA}$		150	250	ns

## PRODUCT INFORMATION

TYPICAL CHARACTERISTICS

FORWARD CURRENT TRANSFER RATIO  
vs  
COLLECTOR CURRENT

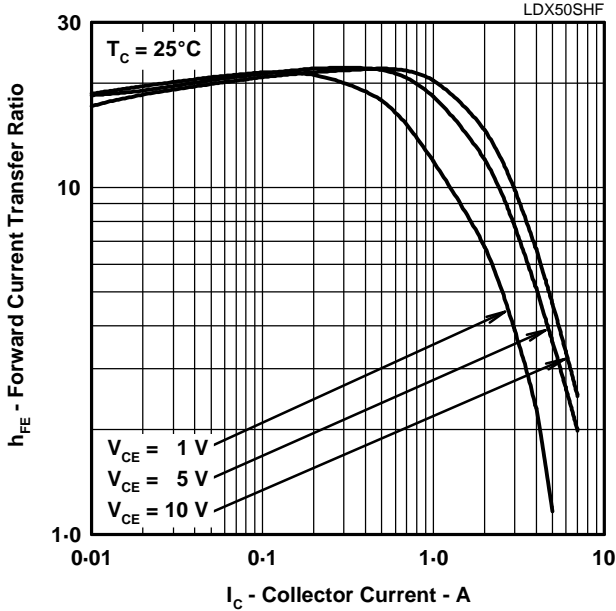


Figure 1.

ANTI-PARALLEL DIODE  
INSTANTANEOUS FORWARD CURRENT  
vs  
INSTANTANEOUS FORWARD VOLTAGE

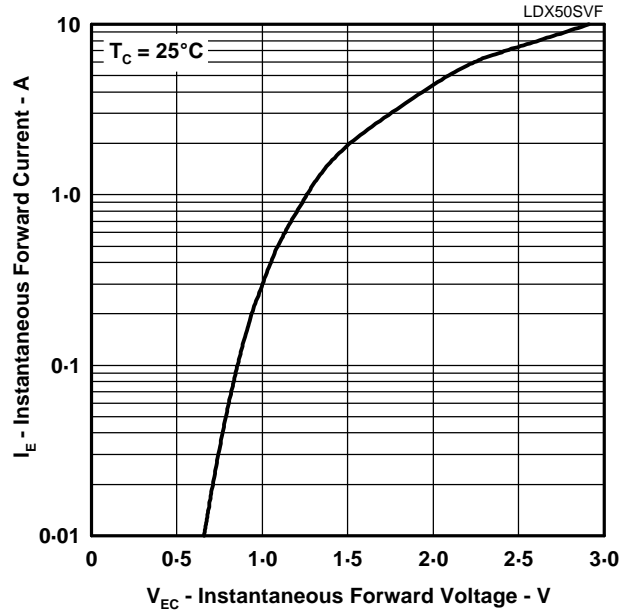


Figure 2.

BASE-EMITTER SATURATION VOLTAGE  
vs  
CASE TEMPERATURE

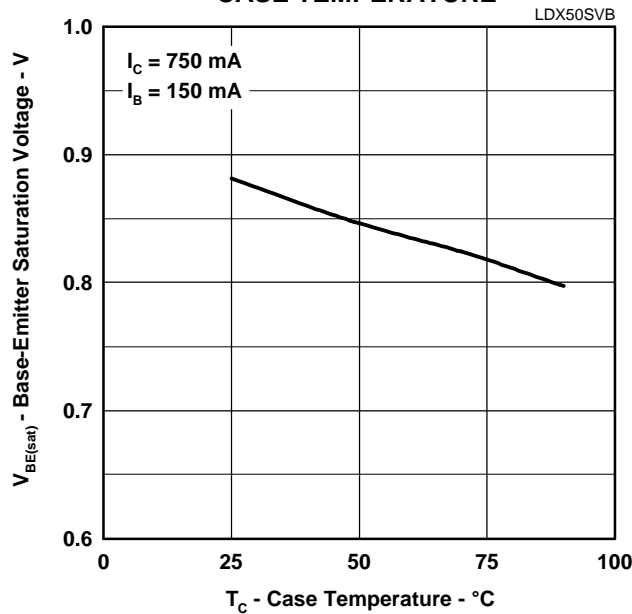
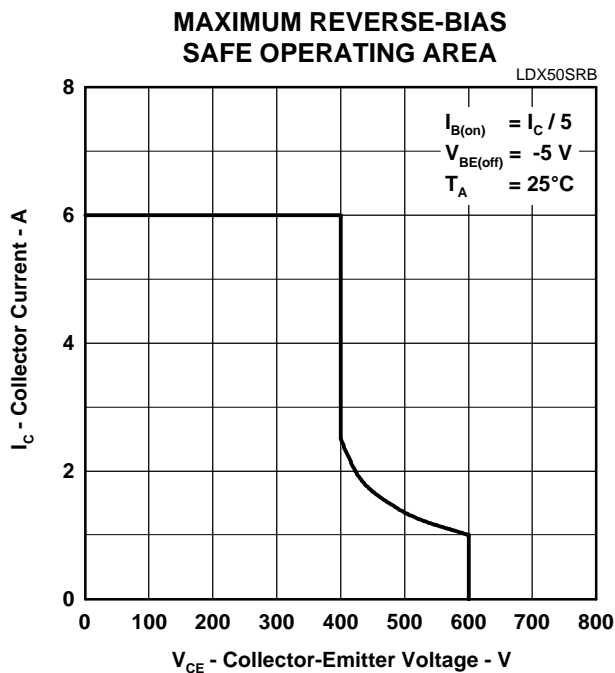
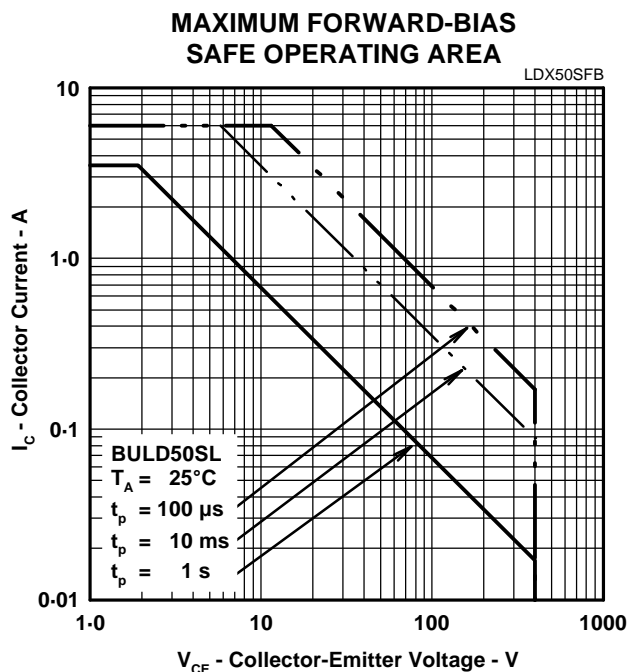
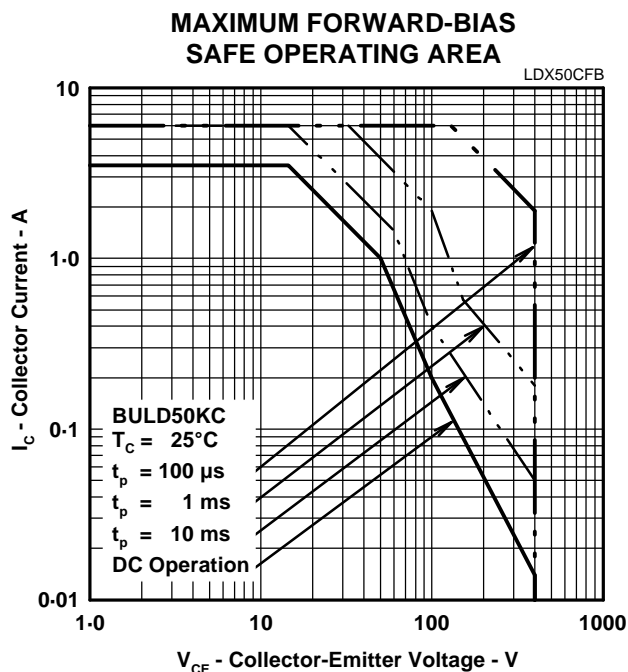


Figure 3.

# BULD50KC, BULD50SL NPN SILICON TRANSISTOR WITH INTEGRATED DIODE

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## MAXIMUM SAFE OPERATING REGIONS



THERMAL INFORMATION

THERMAL RESPONSE JUNCTION TO AMBIENT  
VS  
POWER PULSE DURATION

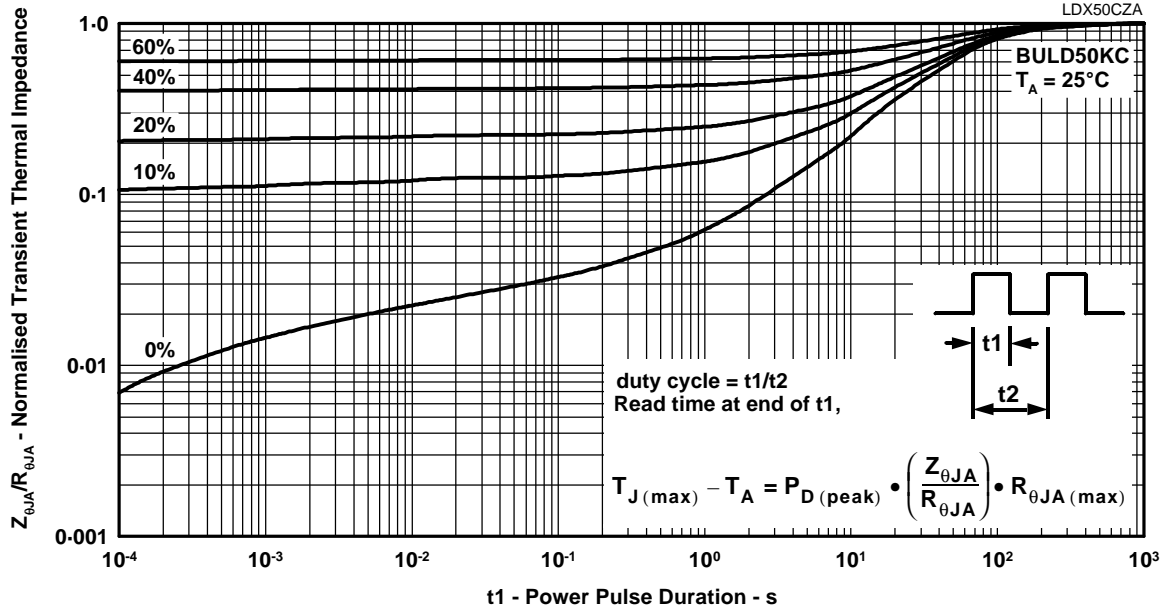


Figure 7.

THERMAL RESPONSE JUNCTION TO AMBIENT  
VS  
POWER PULSE DURATION

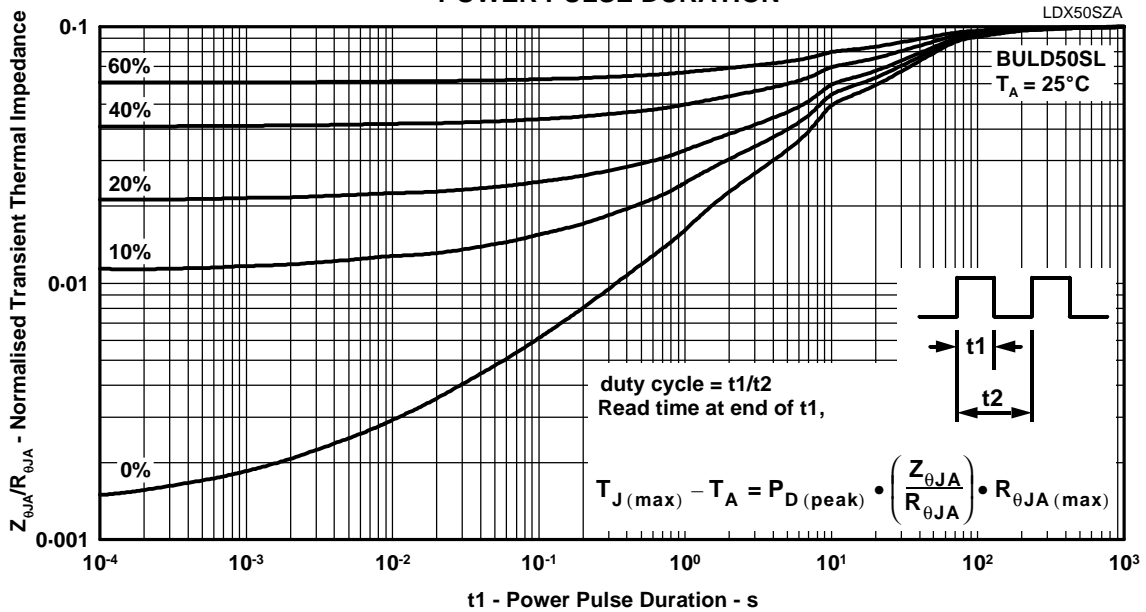


Figure 8.

# BULD50KC, BULD50SL NPN SILICON TRANSISTOR WITH INTEGRATED DIODE

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## THERMAL INFORMATION

### THERMAL RESPONSE JUNCTION TO CASE VS POWER PULSE DURATION

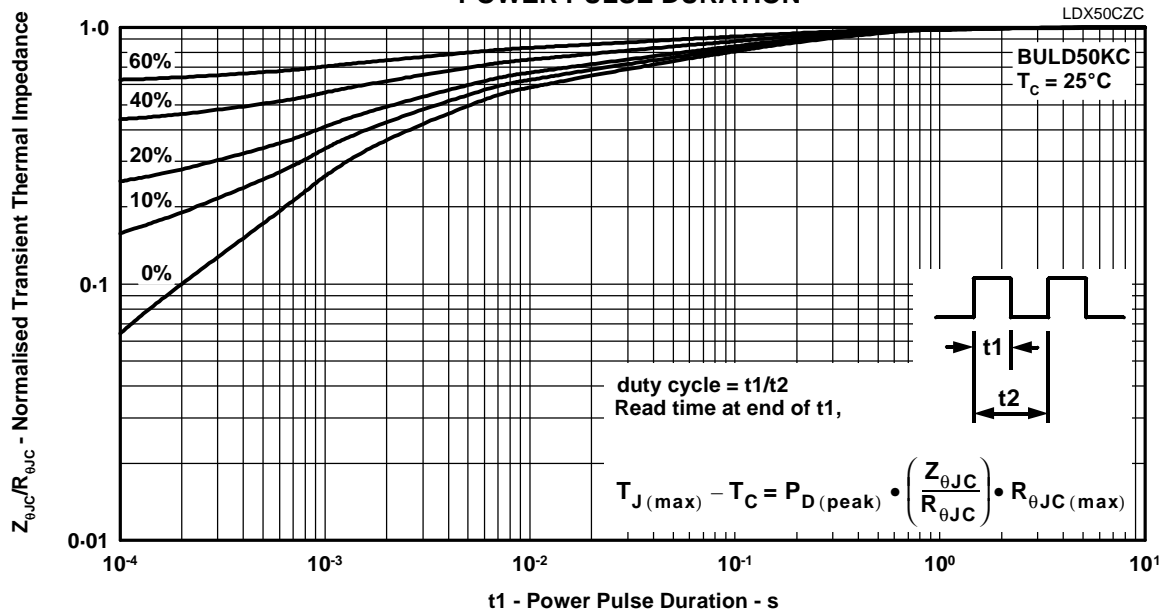


Figure 9.

### MAXIMUM POWER DISSIPATION JUNCTION TO AMBIENT VS POWER PULSE DURATION

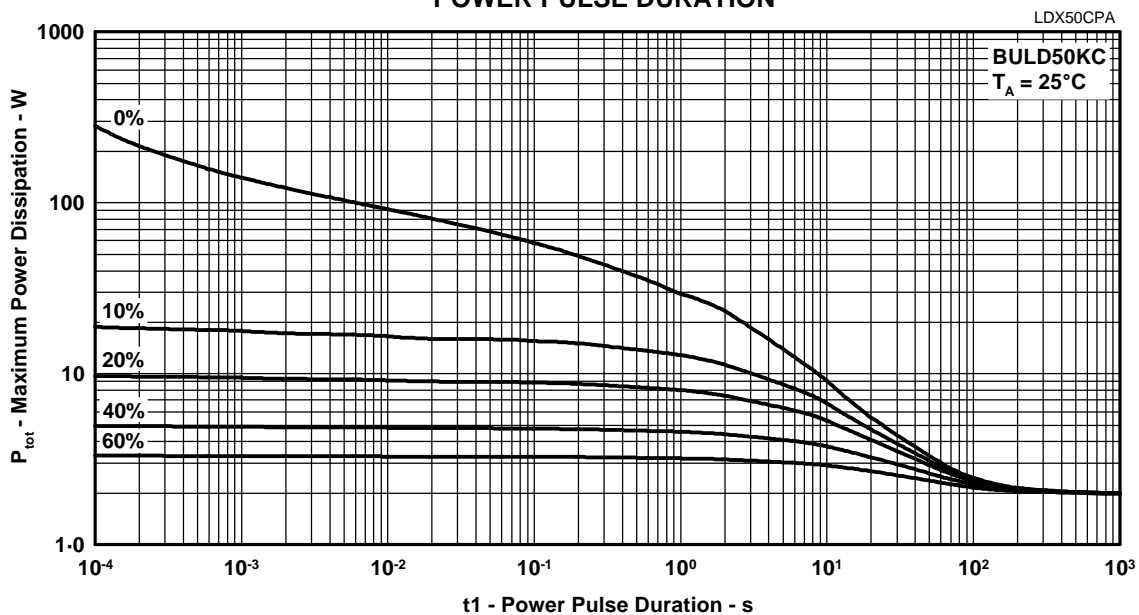


Figure 10.

THERMAL INFORMATION

MAXIMUM POWER DISSIPATION JUNCTION TO AMBIENT  
VS  
POWER PULSE DURATION

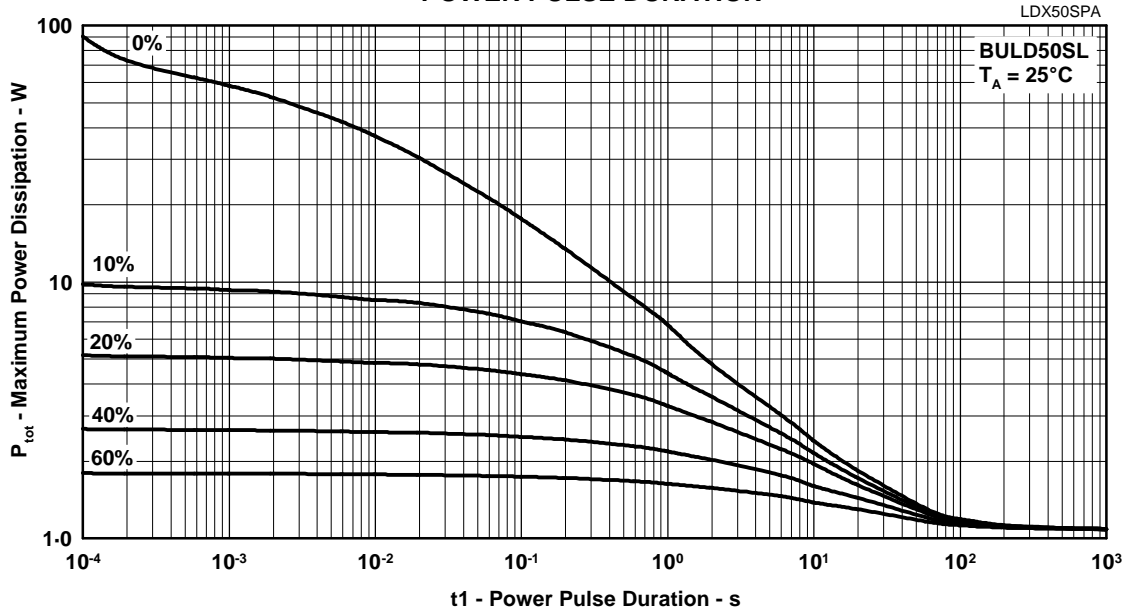


Figure 11.

MAXIMUM POWER DISSIPATION JUNCTION TO CASE  
VS  
POWER PULSE DURATION

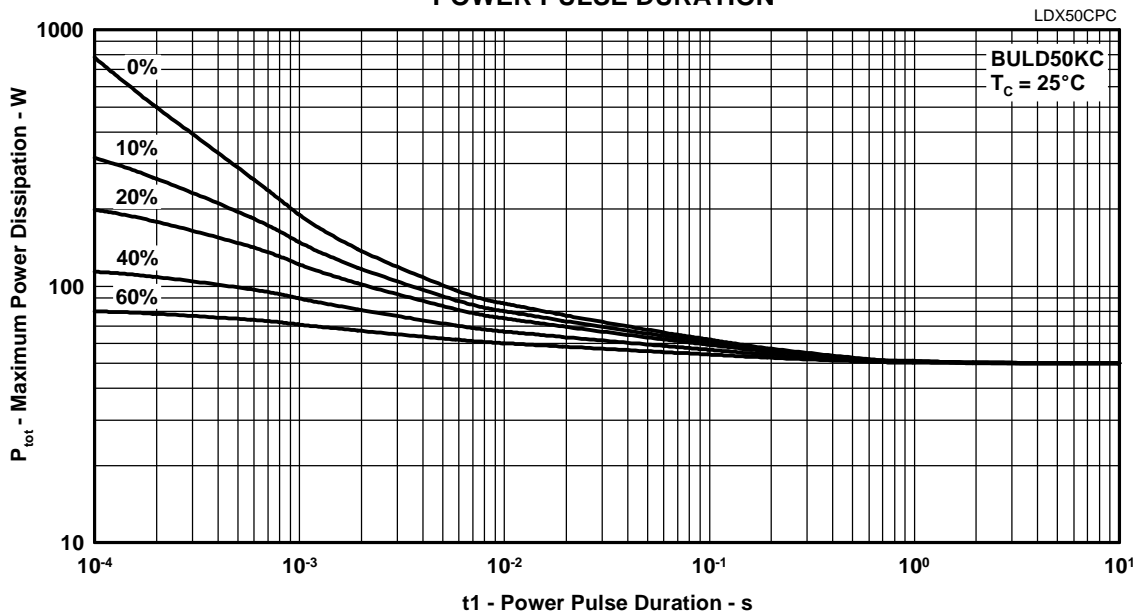


Figure 12.

# BULD50KC, BULD50SL NPN SILICON TRANSISTOR WITH INTEGRATED DIODE

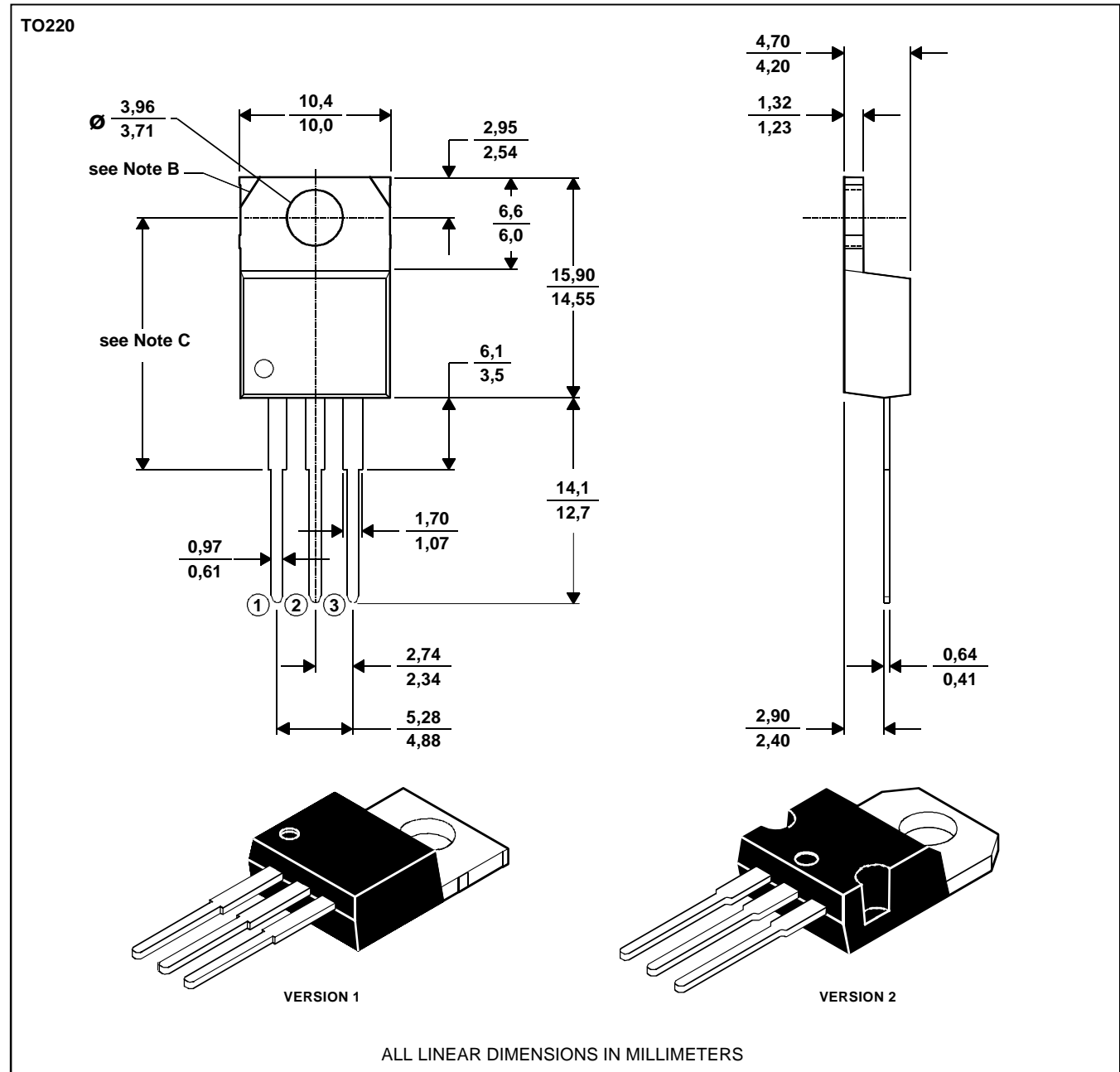
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## MECHANICAL DATA

### TO-220

#### 3-pin plastic flange-mount package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



- NOTES: A. The centre pin is in electrical contact with the mounting tab.  
 B. Mounting tab corner profile according to package version.  
 C. Typical fixing hole centre stand off height according to package version.  
 Version 1, 18.0 mm. Version 2, 17.6 mm.

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## PRODUCT INFORMATION

# BULD50KC, BULD50SL NPN SILICON TRANSISTOR WITH INTEGRATED DIODE

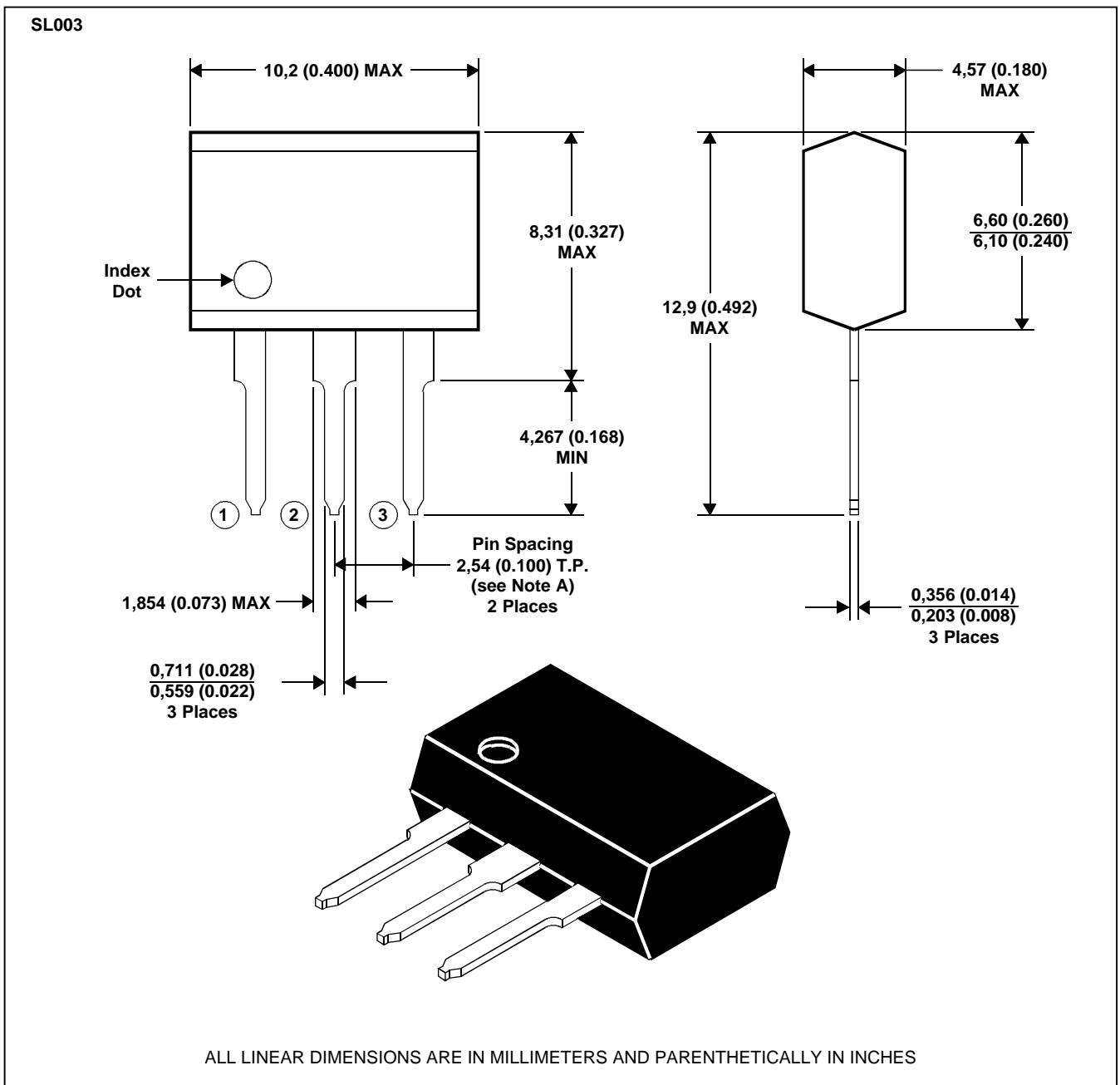
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## MECHANICAL DATA

### SL003

#### 3-pin plastic single-in-line package

This single-in-line package consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation, and circuit performance characteristics will remain stable when operated in high humidity conditions. Leads require no additional cleaning or processing when used in soldered assembly.



NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.  
B. Body molding flash of up to 0,15 (0.006) may occur in the package lead plane.

MDXXAD

# **BULD50KC, BULD50SL**

## **NPN SILICON TRANSISTOR WITH INTEGRATED DIODE**

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