

CD74AC251, CD74ACT251

August 1998

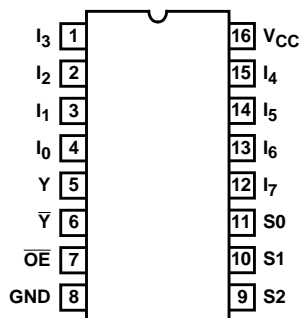
8-Input Multiplexer, Three-State

Features

- Buffered Inputs
- Typical Propagation Delay
 - 6ns at $V_{CC} = 5V$, $T_A = 25^{\circ}C$, $C_L = 50pF$
- Exceeds 2kV ESD Protection MIL-STD-883, Method 3015
- SCR-Latchup-Resistant CMOS Process and Circuit Design
- Speed of Bipolar FAST™/AS/S with Significantly Reduced Power Consumption
- Balanced Propagation Delays
- AC Types Feature 1.5V to 5.5V Operation and Balanced Noise Immunity at 30% of the Supply
- $\pm 24mA$ Output Drive Current
 - Fanout to 15 FAST™ ICs
 - Drives 50 Ω Transmission Lines

Pinout

CD74AC251, CD74ACT251
(PDIP, SOIC)
TOP VIEW



Description

The CD74AC251 and CD74ACT251 8-input multiplexers that utilize the Harris Advanced CMOS Logic technology. This multiplexer features both true (Y) and complement (\bar{Y}) outputs as well as an Output Enable (\bar{OE}) input. The \bar{OE} must be at a LOW logic level to enable this device. When the \bar{OE} input is HIGH, both outputs are in the high-impedance state. When enabled, address information on the data select inputs determines which data input is routed to the Y and \bar{Y} outputs.

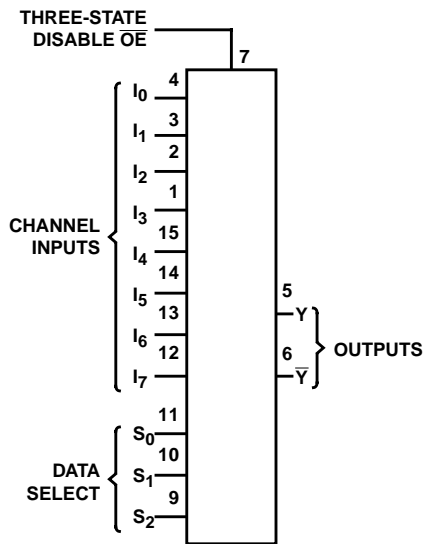
Ordering Information

PART NUMBER	TEMP. RANGE ($^{\circ}C$)	PACKAGE	PKG. NO.
CD74AC251E	0 to 70 $^{\circ}C$, -40 to 85, -55 to 125	16 Ld PDIP	E16.3
CD74ACT251E	0 to 70 $^{\circ}C$, -40 to 85, -55 to 125	16 Ld PDIP	E16.3
CD74AC251M	0 to 70 $^{\circ}C$, -40 to 85, -55 to 125	16 Ld SOIC	M16.15
CD74ACT251M	0 to 70 $^{\circ}C$, -40 to 85, -55 to 125	16 Ld SOIC	M16.15

NOTES:

1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer and die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

Functional Diagram



TRUTH TABLE

INPUTS			OUTPUTS		
SELECT			OUTPUT ENABLE \overline{OE}	Y	\overline{Y}
S2	S1	S0			
X	X	X	H	Z	Z
L	L	L	L	I ₀	$\overline{I_0}$
L	L	H	L	I ₁	$\overline{I_1}$
L	H	L	L	I ₂	$\overline{I_2}$
L	H	H	L	I ₃	$\overline{I_3}$
H	L	L	L	I ₄	$\overline{I_4}$
H	L	H	L	I ₅	$\overline{I_5}$
H	H	L	L	I ₆	$\overline{I_6}$
H	H	H	L	I ₇	$\overline{I_7}$

H = High logic level, L = Low logic level, Z = High impedance (off),
 X = Irrelevant, I₀, I₁...I₇ = The level of the respective input

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Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 6V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 50mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 50mA$
DC V_{CC} or Ground Current, I_{CC} or I_{GND} (Note 3)	$\pm 100mA$

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)
PDIP Package	—
SOIC Package	—
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C

Operating Conditions

Temperature Range, T_A	-55°C to 125°C
Supply Voltage Range, V_{CC} (Note 4)	
AC Types	1.5V to 5.5V
ACT Types	4.5V to 5.5V
DC Input or Output Voltage, V_I , V_O	0V to V_{CC}
Input Rise and Fall Slew Rate, dt/dv	
AC Types, 1.5V to 3V	50ns (Max)
AC Types, 3.6V to 5.5V	20ns (Max)
ACT Types, 4.5V to 5.5V	10ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

3. For up to 4 outputs per device, add $\pm 25mA$ for each additional output.
4. Unless otherwise specified, all voltages are referenced to ground.
5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS	
		V_I (V)	I_O (mA)		MIN	MAX	MIN	MAX	MIN	MAX		
AC TYPES												
High Level Input Voltage	V_{IH}	-	-	1.5	1.2	-	1.2	-	1.2	-	V	
				3	2.1	-	2.1	-	2.1	-	V	
				5.5	3.85	-	3.85	-	3.85	-	V	
Low Level Input Voltage	V_{IL}	-	-	1.5	-	0.3	-	0.3	-	0.3	V	
				3	-	0.9	-	0.9	-	0.9	V	
				5.5	-	1.65	-	1.65	-	1.65	V	
High Level Output Voltage	V_{OH}	V_{IH} or V_{IL}	-0.05	-0.05	1.5	1.4	-	1.4	-	1.4	-	V
			-0.05	-0.05	3	2.9	-	2.9	-	2.9	-	V
			-0.05	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-4	-4	3	2.58	-	2.48	-	2.4	-	V
			-24	-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	-75	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	-50	5.5	-	-	-	-	3.85	-	V

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DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C		-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	1.5	-	0.1	-	0.1	-	0.1	V
			0.05	3	-	0.1	-	0.1	-	0.1	V
			0.05	4.5	-	0.1	-	0.1	-	0.1	V
			12	3	-	0.36	-	0.44	-	0.5	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	1.65	V	
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Three-State Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	-	5.5	-	±0.5	-	±5	-	±10	μA
Quiescent Supply Current MSI	I _{CC}	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μA
ACT TYPES											
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage	V _{OH}	V _{IH} or V _{IL}	-0.05	4.5	4.4	-	4.4	-	4.4	-	V
			-24	4.5	3.94	-	3.8	-	3.7	-	V
			-75 (Note 6, 7)	5.5	-	-	3.85	-	-	-	V
			-50 (Note 6, 7)	5.5	-	-	-	-	3.85	-	V
Low Level Output Voltage	V _{OL}	V _{IH} or V _{IL}	0.05	4.5	-	0.1	-	0.1	-	0.1	V
			24	4.5	-	0.36	-	0.44	-	0.5	V
			75 (Note 6, 7)	5.5	-	-	-	1.65	-	-	V
			50 (Note 6, 7)	5.5	-	-	-	-	-	1.65	V
Input Leakage Current	I _I	V _{CC} or GND	-	5.5	-	±0.1	-	±1	-	±1	μA
Three-State or Leakage Current	I _{OZ}	V _{IH} or V _{IL} V _O = V _{CC} or GND	-	5.5	-	±0.5	-	±5	-	±10	μA
Quiescent Supply Current MSI	I _{CC}	V _{CC} or GND	0	5.5	-	8	-	80	-	160	μA
Additional Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI _{CC}	V _{CC} -2.1	-	4.5 to 5.5	-	2.4	-	2.8	-	3	mA

NOTES:

- Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.
- Test verifies a minimum 50Ω transmission-line-drive capability at 85°C, 75Ω at 125°C.

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ACT Input Load Table

INPUT	UNIT LOAD
S0, S1, S3	1
OE	1
I ₀ - I ₇	1

NOTE: Unit load is ΔI_{CC} limit specified in DC Electrical Specifications Table, e.g., 2.4mA max at 25°C.

Switching Specifications Input $t_r, t_f = 3ns, C_L = 50pF$ (Worst Case)

PARAMETER	SYMBOL	V _{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
AC TYPES									
Propagation Delay, Data to Y Output	t _{PLH} , t _{PHL}	1.5	-	-	153	-	-	169	ns
		3.3 (Note 9)	4.9	-	17.2	4.7	-	18.9	ns
		5 (Note 10)	3.5	-	12.3	3.4	-	13.5	ns
Propagation Delay, Data to \bar{Y} Output	t _{PLH} , t _{PHL}	1.5	-	-	169	-	-	186	ns
		3.3	5.4	-	19	5.2	-	20.9	ns
		5	3.8	-	13.5	3.7	-	14.9	ns
Propagation Delay, Select to Y Output	t _{PLH} , t _{PHL}	1.5	-	-	207	-	-	228	ns
		3.3	6.6	-	23.2	6.4	-	25.5	ns
		5	4.7	-	16.5	4.6	-	18.2	ns
Propagation Delay, Select to \bar{Y} Output	t _{PLH} , t _{PHL}	1.5	-	-	223	-	-	245	ns
		3.3	7.1	-	24.9	6.9	-	27.4	ns
		5	5.1	-	17.8	4.9	-	19.6	ns
Propagation Delay, Output Enable and Output Disable to Output	t _{PZH} , t _{PZL} , t _{PHZ} , t _{PLZ}	1.5	-	-	155	-	-	169	ns
		3.3	5.2	-	18.7	5.1	-	20.3	ns
		5	3.5	-	12.3	3.4	-	13.5	ns
Three-State Output Capacitance	C _O	-	-	-	15	-	-	15	pF
Input Capacitance	C _I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C _{PD} (Note 11)	-	-	120	-	-	120	-	pF
ACT TYPES									
Propagation Delay, Data to Y Output	t _{PLH} , t _{PHL}	5 (Note 10)	3.5	-	12.3	3.4	-	13.5	ns
Propagation Delay, Data to \bar{Y} Output	t _{PLH} , t _{PHL}	5	3.8	-	13.5	3.7	-	14.9	ns
Propagation Delay, Select to Y Output	t _{PLH} , t _{PHL}	5	4.7	-	16.5	4.6	-	18.2	ns
Propagation Delay, Select to \bar{Y} Output	t _{PLH} , t _{PHL}	5	5.1	-	17.8	4.9	-	19.6	ns
Propagation Delay, Output Enable and Output Disable to Output	t _{PZH} , t _{PZL} , t _{PHZ} , t _{PLZ}	5	3.5	-	12.3	3.4	-	13.5	ns

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Switching Specifications Input $t_r, t_f = 3\text{ns}$, $C_L = 50\text{pF}$ (Worst Case) (Continued)

PARAMETER	SYMBOL	V_{CC} (V)	-40°C TO 85°C			-55°C TO 125°C			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Three-State Output Capacitance	C_O								
Input Capacitance	C_I	-	-	-	10	-	-	10	pF
Power Dissipation Capacitance	C_{PD} (Note 11)	-	-	45	-	-	45	-	pF

NOTES:

8. Limits tested 100%.
9. 3.3V Min is at 3.6V, Max is at 3V.
10. 5V Min is at 5.5V, Max is at 4.5V.
11. C_{PD} is used to determine the dynamic power consumption per device.
 $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

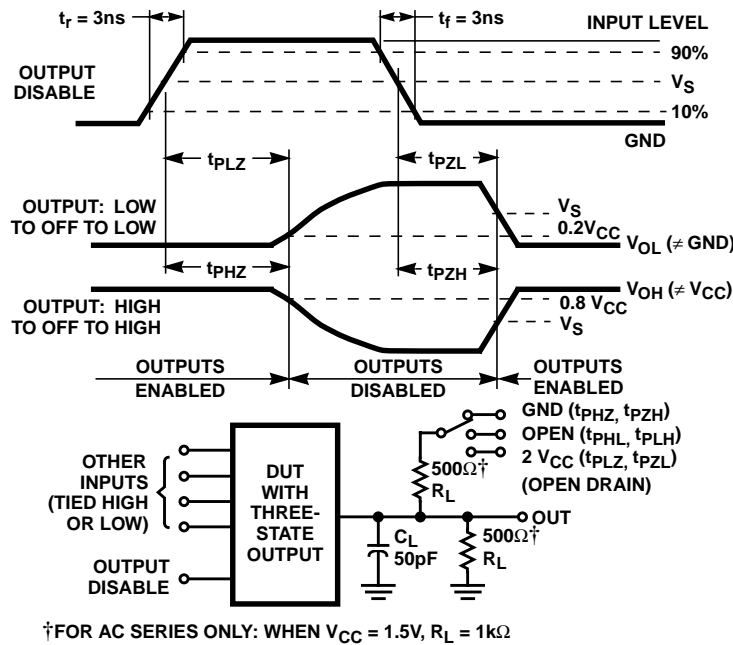


FIGURE 1. THREE-STATE PROPAGATION DELAY WAVEFORMS AND TEST CIRCUIT

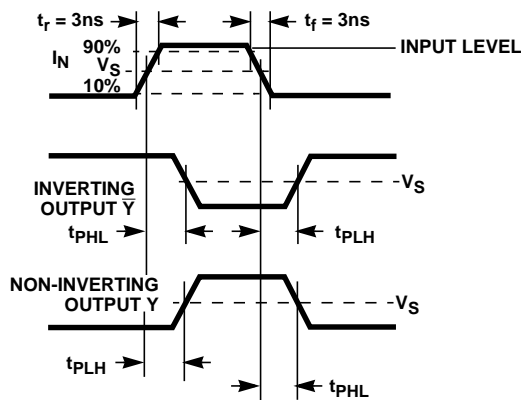
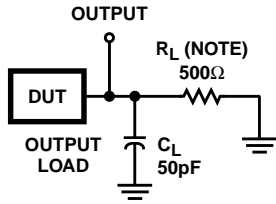


FIGURE 2. PROPAGATION DELAY TIMES

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NOTE: For AC Series Only: When $V_{CC} = 1.5V$, $R_L = 1k\Omega$.

	CD74AC	CD74ACT
Input Level	V_{CC}	3V
Input Switching Voltage, V_S	$0.5 V_{CC}$	1.5V
Output Switching Voltage, V_S	$0.5 V_{CC}$	$0.5 V_{CC}$

FIGURE 3. PROPAGATION DELAY TIMES

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