

SONY

CX20018/CXA1144S

Dual 16 bit 44kHz Multiplexed A/D Converter

Evaluation Board Available — CX20018PCB

Description

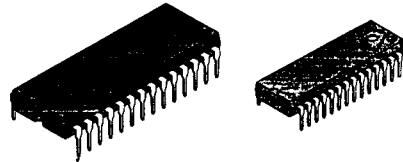
CX20018/CXA1144S are monolithic bipolar ICs designed for PCM (Pulse Code Modulation) audio. This IC consists of 16 bit counters, shift registers, clock buffer, clocked synchronous comparator, stabilized current source and TTL compatible interface circuits, etc.

Features

- Good monotonicity
- Low noise
- TTL compatible input/output
- Stereo or monaural modes can be selected by external control

28 pin DIP (Plastic)

28 pin SDIP (Plastic)



Structure

Bipolar silicon monolithic IC

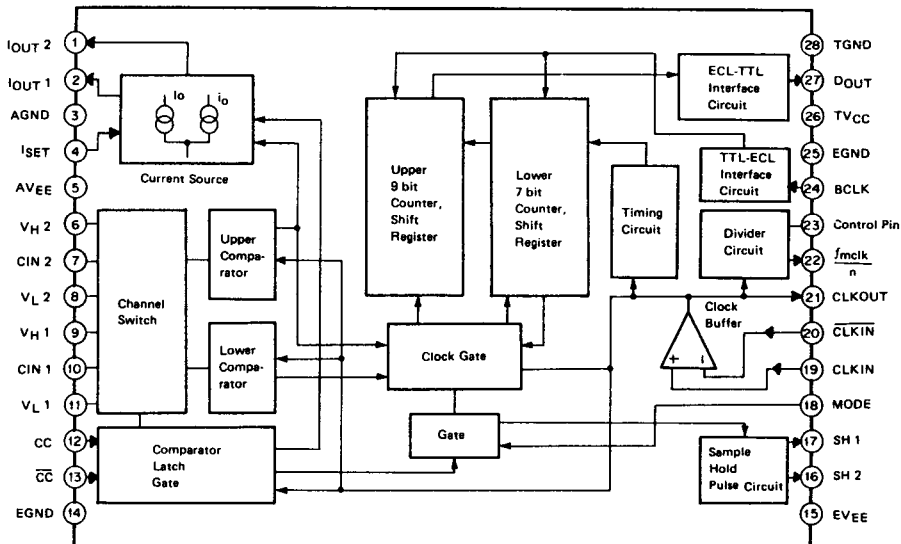
Absolute Maximum Ratings

• Supply voltage	V_{CC} to V_{EE}	12	V
• Operating temperature	T_{opr}	-20 to +75	°C
• Storage temperature	T_{stg}	-50 to +150	°C
• Allowable power dissipation	P_D	1.7	W (CX20018)
	P_D	1.2	W (CXA1144S)

Recommended Operating Conditions

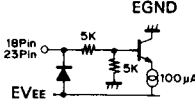
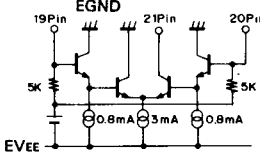
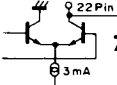
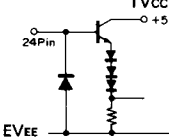
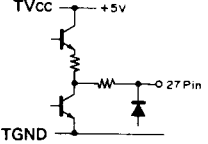
• Supply voltage	V_{CC}	4.75 to 5.25	V
	V_{EE}	-5.25 to -4.75	V

Block Diagram



Pin Description and Equivalent Circuit

No.	Symbol	Equivalent circuit	Description
1	Iout2		Integration current output of channel 2
2	Iout1		Integration current output of channel 1
3	AGND		Analog ground
4	ISET		Setting the value of integration current ($I_{SET} = 32I_o$, $I_{SET} = I_o/4$) $I_{SET} \leq 750\mu A$
5	AVee		Analog supply
6	VH2		Upper comparator input of channel 2
8	VL2		Lower comparator input of channel 2
9	VH1		Upper comparator input of channel 1
11	VL1		Lower comparator input of channel 1
7	CIN2		Upper and lower common input of channel 2
10	CIN1		Upper and lower common input of channel 1
12	CC		Non-inverting input of conversion command $600mV \leq CC \leq 4.0V$
13	\overline{CC}		Inverting input of conversion command
14	EGND		Digital ground (ECL)
15	EVee		Digital supply
16	SH2		Sample/hold pulse output of channel 2
17	SH1		Sample/hold pulse output of channel 1

No.	Symbol	Equivalent circuit	Description
18	MODE		Switching of stereo, monaural or sample/hold pulse.
23	CONTROL PIN		Determining division ratio of divided output. Can select division ratio at OFF, 1/2, 1/4, 1/8 of master clock frequency
19	CLK IN		Non-inverting input of clock buffer
20	CLK IN		Inverting input of clock buffer
21	CLK OUT		Output of clock buffer
22	$\frac{fMCLK}{N}$		Divided output (Open corrector)
24	BCLK		Clock input that shifts the internal converted data to external.
25	EGND		Digital ground
26	TVCC		Digital supply
27	DOUT		Conversion data output (Output at TTL level)
28	TGND		TTL ground

Electrical Characteristics

(Ta=25°C, VEE=-5V, VCC=5V)

Item	Symbol	Pin No. and Test Condition	Min.	Typ.	Max.	Unit	Note
Supply voltage range *1	VEE		-4.75	-5.00	-5.25	V	1
Supply voltage range *1	VCC		4.75	5.00	5.25	V	1
Circuit current	IEE		70.0	102.0	130.0	mA	1
Circuit current	ICC		4.0	10.0	15.0	mA	1
Current output pin leak	IOLEAK	1, 2 (Pins 1, 2 Voltage=0V when current output is off)			1.0	μA	2
IOUT output current	Iout	1, 2 (Pins 1, 2 Voltage=0V, Iset=410 μA)		1.64		mA	2
Current ratio *2	Io/io	1, 2 (Iset=410 μA)	127.0	128.0	129.0		2
Maximum ISET current	ISET Max.	4 $127.0 \leq \frac{I_o}{i_o} \leq 129.0$			750	μA	2
Sample hold pulse high level output voltage	VSH1H VSH2H	16, 17	-0.05	0	0.1	V	
Sample hold pulse low level output voltage	VSH1L VSH2L	16, 17	-4.40	-4.25	-3.50	V	
Clock input bias voltage	VCLKIN VCLKIN	19, 20	-1.90	-1.72	-1.50	V	
Clock output low level output current	ICLKOUTL	21		3.0	4.0	mA	
CC, CC input bias voltage	VCCIN VCCIN	12, 13	-2.20	-1.92	-1.60	V	
Data output high level output voltage	VDOUTH	27 I _{OH} =0.1 mA	3.2			V	
Data output low level output voltage	VDOUTL	27 I _{OL} =-0.4 mA			0.4	V	
Bit clock high level input voltage	VBCLKH	24	2.0			V	
Bit clock low level input voltage	VBCLKL	24			0.5	V	
Bit clock high level input current	IBCLKH	24		4		μA	
Bit clock low level input current	IBCLKL	24	0.2	1		μA	
Distortion *3 factor	THD	During 0 dB (full scale) playback for both channel		0.005	0.006	%	3
		During -20 dB playback for both channel			0.05	%	3

Item	Symbol	Pin No. and Test Condition		Min.	Typ.	Max.	Unit
Maximum operating clock frequency	fMCLK	Self-excitation or separate excitation	CX20018			100 (CX20018)	MHz
			CXA1144S			95 (CXA1144S)	
Dividing ratio control voltage	VCTL (∞)	23		2.0		5.0	V
	VCTL (2)	23		0.2		0.8	V
	VCTL (4)	23		-0.8		-0.2	V
	VCTL (8)	23		-5.0		-2.0	V
Mode control voltage	VMODE (1)	18 Stereo, S/H ON		2.0		5.0	V
	VMODE (2)	18 Stereo, S/H OFF		0.2		0.8	V
	VMODE (3)	18 Monaural, S/H OFF		-0.8		-0.2	V
	VMODE (4)	18 Monaural, S/H ON		-5.0		-2.0	V

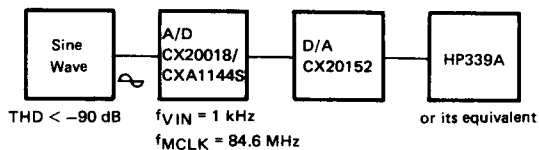
- Note)** 1 Pins 1, 2, 3, 6, 7, 8, 9, 10, 11, 14, 21, 25 and 28 are for grounding, pins 18, 22, 23, are connected Vcc. Pin 4 draws 410 μA of current by external current source.
 2 Reference to the current ratio test circuit.
 3 Conversion Frequency 44.1 kHz
 Distortion Meter HP339A (all Filters are turned on) or its equivalent that has an 80 kHz, LPF, 30 kHz LPF and 400 Hz HPF.

*1 Recommended operating voltage

*2 In the current ratio test circuit (See Fig. 1)

$$\left| 15 \times 8 \text{ (k}\Omega\text{)} \times i_o \text{ (}\mu\text{A)} - \frac{15}{16} \text{ (k}\Omega\text{)} \times i_o \text{ (}\mu\text{A)} \right| < 12.0 \text{ mV}$$

*3 Measurement Method (See Note 3)



Current Ratio Test Circuit

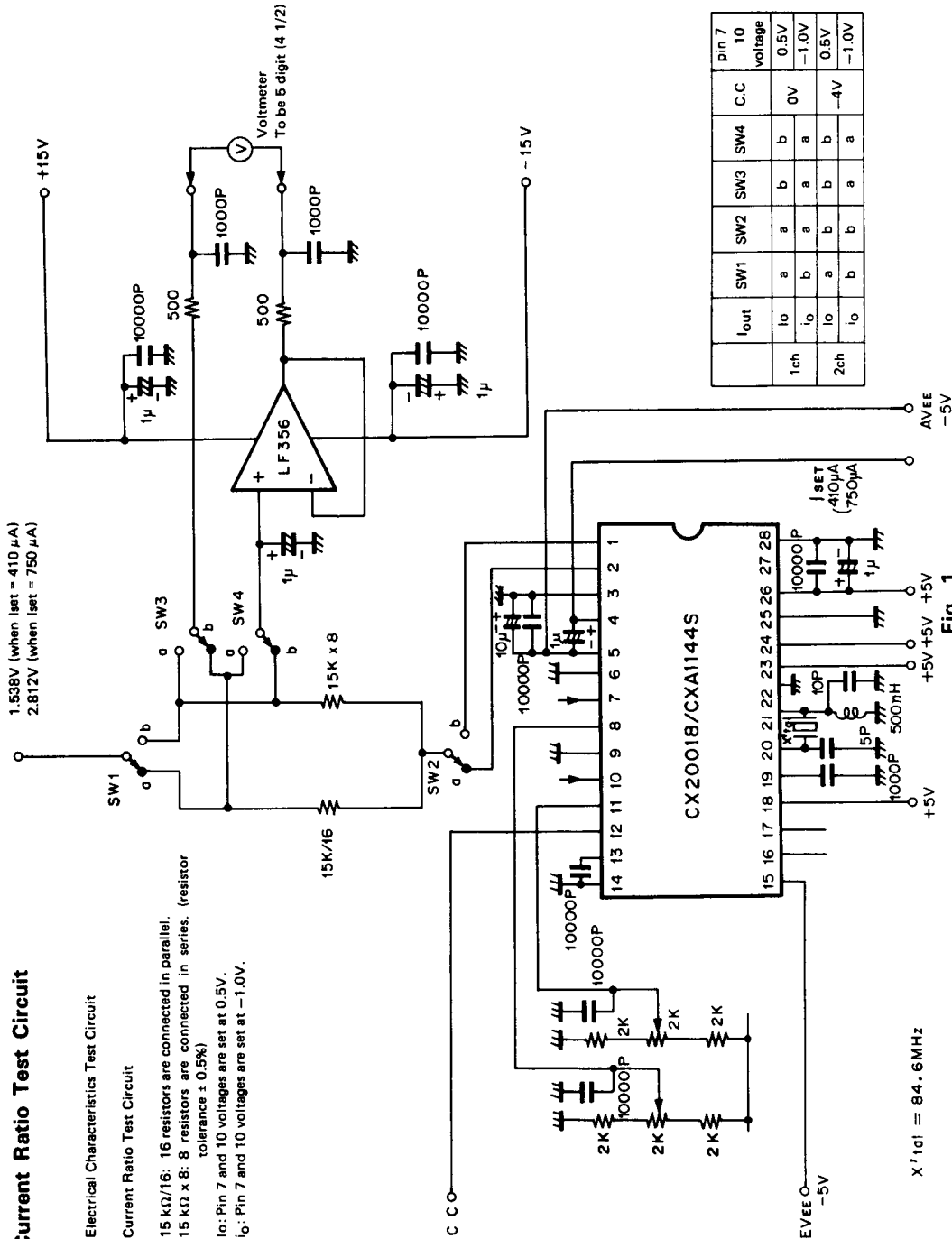
Electrical Characteristics Test Circuit

Current Ratio Test Circuit

15 kΩ/16: 16 resistors are connected in parallel.
 15 kΩ x 8: 8 resistors are connected in series. (resistor tolerance ± 0.5%)

I_o: Pin 7 and 10 voltages are set at 0.5V.

I_o: Pin 7 and 10 voltages are set at -1.0V.



X¹f_{ol} = 84.6MHz

Fig. 1

Description of CX20018 Conversion Process

Conversion process

The timing circuit controls a conversion cycle and send "Data Transfer Pulse" to the 16 bit shift register for transmitting the last converted data. It is reset by both the edge of CC (Conversion Command), and the master clock pulse is fed to the timing circuit.

"Data Transfer Pulse" and "Mask Pulse" become "H" level as soon as the timing circuit starts to count clocks. "Data Transfer Pulse" becomes "L" when the timing circuit counts 11 clocks, and then the last data is transferred. Simultaneously, "Current Switch Pulse" becomes "H", and integral current starts to flow. "Counter Preset Pulse" becomes "H" when the timing circuit counts 16 clocks. And then, upper and lower level counters are reset. Counter Preset Pulse holds "H" level during the period of 8 clocks.

When the timing circuit counts 31 clocks, Mask Pulse becomes "L" and A/D conversion starts.

The coarse current "I_o" discharges the sampled charge of integrator until the output voltage of integrator crosses the reference voltage (VrefH). During this period the upper level counter counts the number of clock. After crossing the VrefH the fine current discharges the remaining charge of integrator. The lower level counter counts the number of clock until the output voltage of integrator crosses the lower level references voltage (VrefL). (See Figs. 2, 3, 4)

Data output

Data are 16 bit serial signals and 2's complement. The serial data are synchronous with a rising edge of Bit clock (BCLK), and only MSB data is synchronized with a edge of "Conversion Command (CC)" (See Fig. 3)

Monaural operation mode

In monaural mode the external integrator is tracking the input signal during CC is "H" state. At the moment when CC goes "L" state, the CX20018/CXA1144S starts conversion. The data is transferred to the output from MSB sequentially.

After 16 bit data are transferred, "Data Out" comes to the "H" level and keeps "H" level until next conversion. (See Fig. 4)

Timing Chart

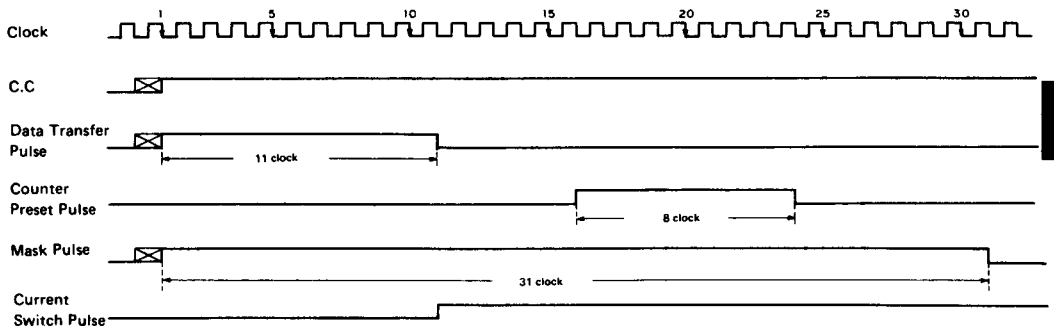


Fig. 2

Stereo Mode

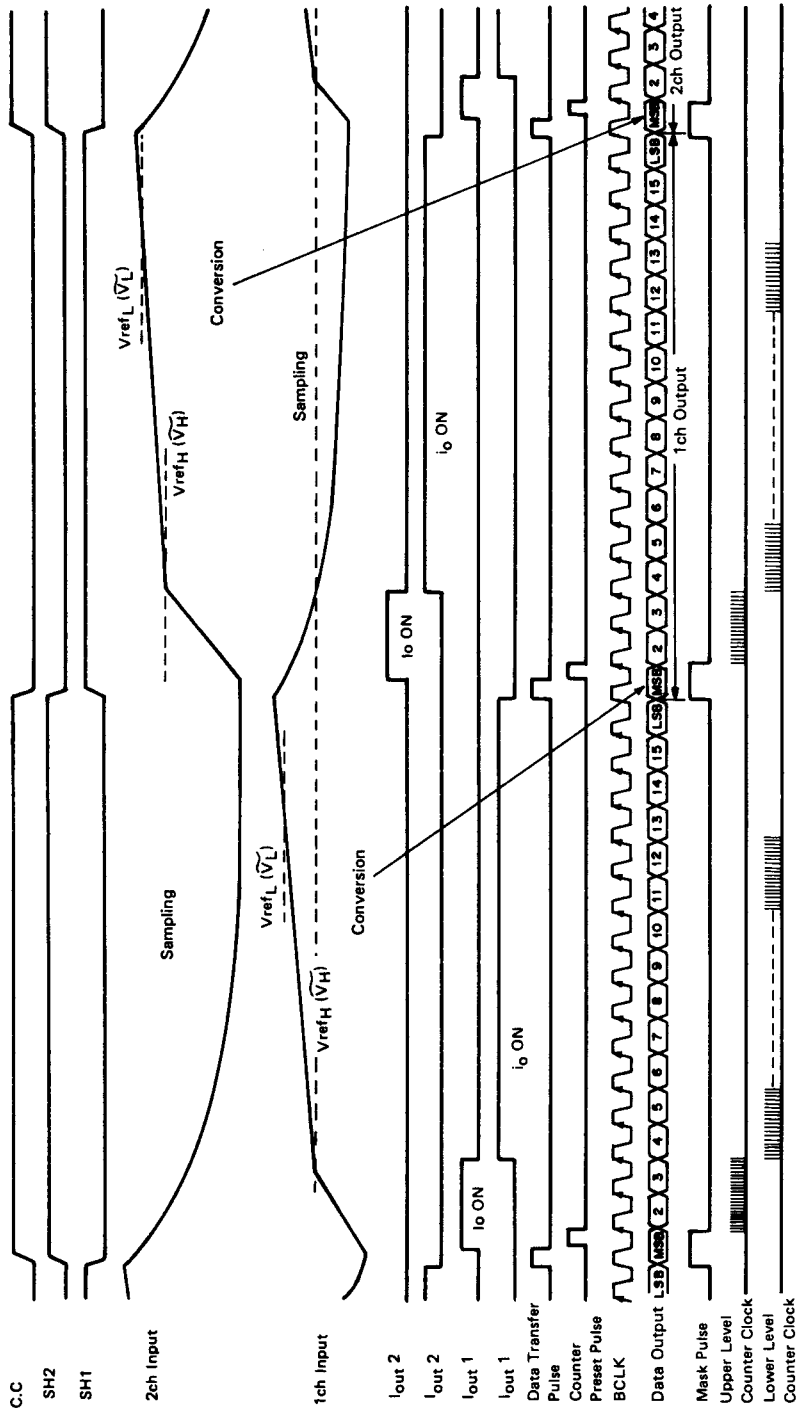


Fig. 3

Monaural Mode

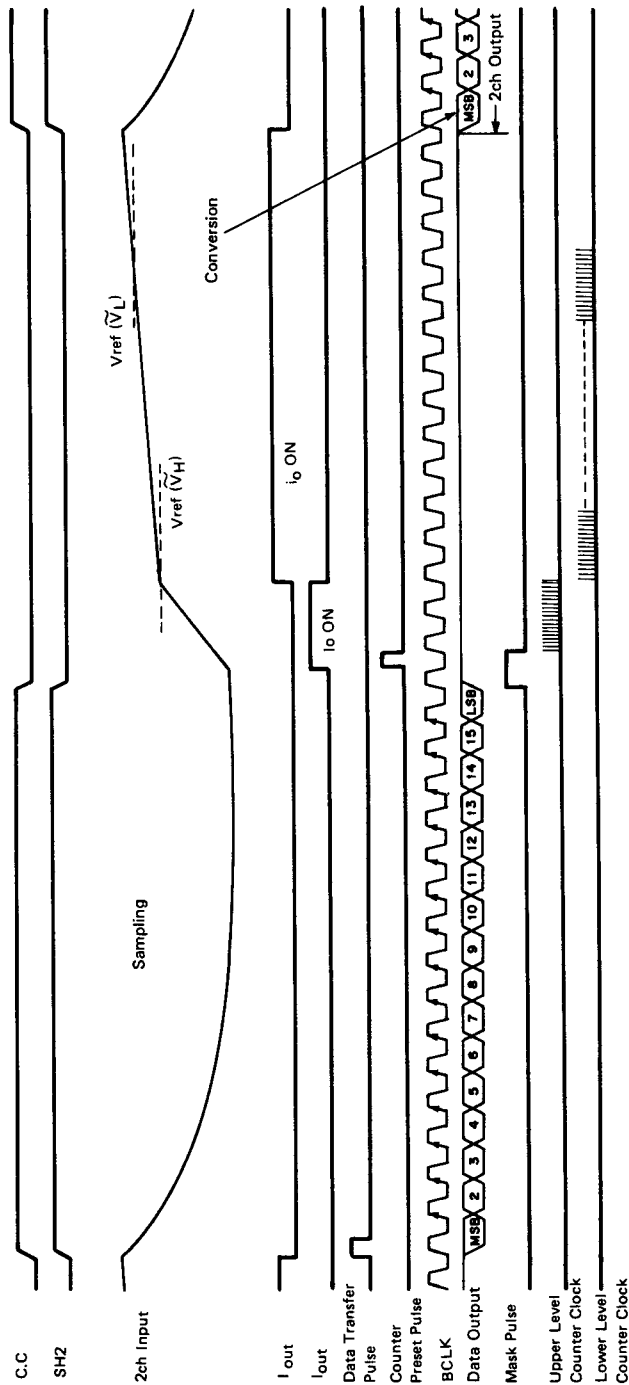


Fig. 4

Interface Circuit, Divider Circuit, Sample/Hold Circuit

(1) Intergration current output

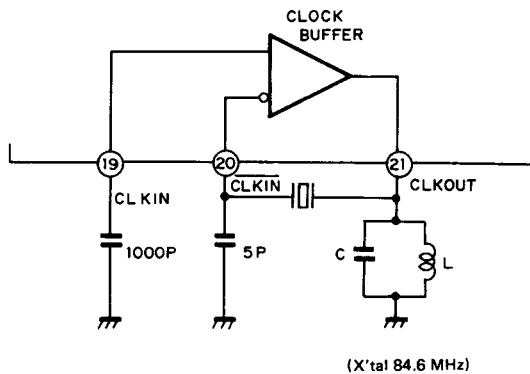
Recommended value; $I_{set} = 410 \mu A$

$$\left(\begin{array}{l} I_o = 4 I_{set} = 1.64 \text{ mA} \\ I_o = \frac{1}{32} I_{set} = 12.8 \mu A \end{array} \right)$$

with $C_{SH} = 1000pF$
 $f_{MCLK} = 84.6 \text{ MHz}$
 $V_{in} = 10 \text{ Vp-p}$

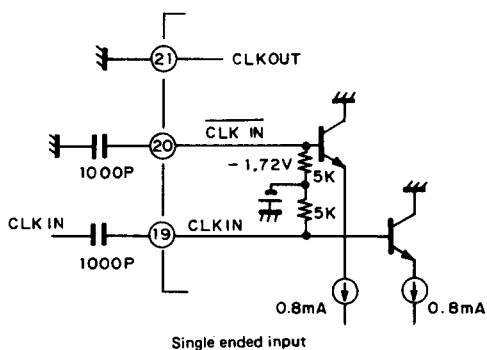
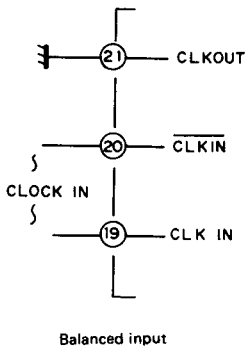
(2) Clock Buffer

(a) Internal clock (Excited circuit with crystal)



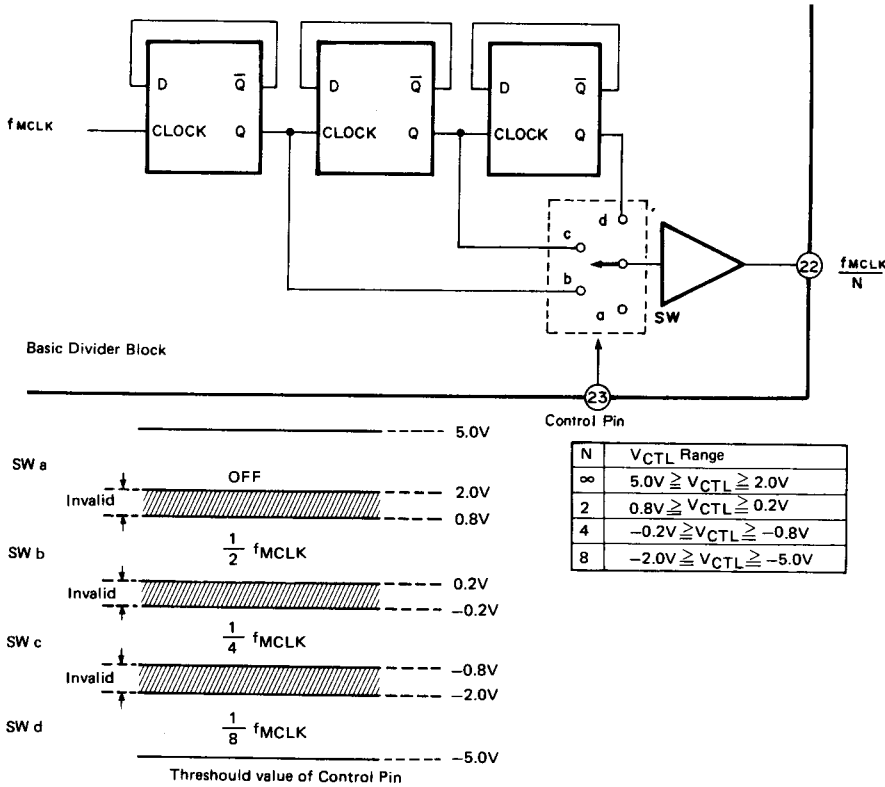
$(C, L) = (10p, 500nH)$
 or
 $(15p, 270nH)$

(b) External clock



(3) fMCLK/N Output

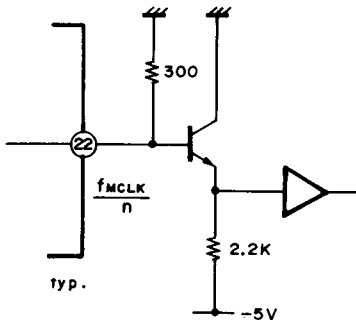
The output of fMCLK/N is prepared for synchronous operation with digital circuit. Divided value "N" is determined by external control, and N is 2, 4, 8 or ∞.



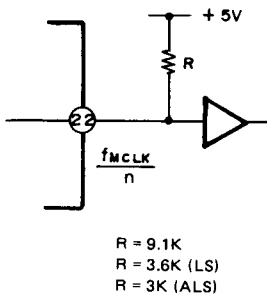
(4) Recommended Interface Circuit

[In all of these cases, R15(3KΩ) mounted on the PCB should be removed. Instead, a resistor (300, 3.6K and 1.2K, respectively) should be attached externally.]

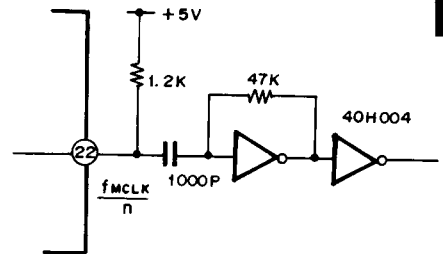
(a) ECL 10k (N=2)



(b) TTLs (N=4 or 8)



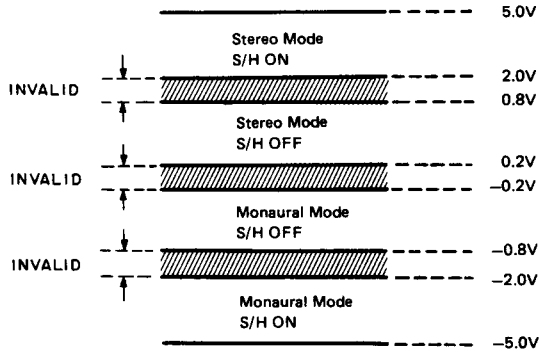
(c) High Speed CMOS (N=8)



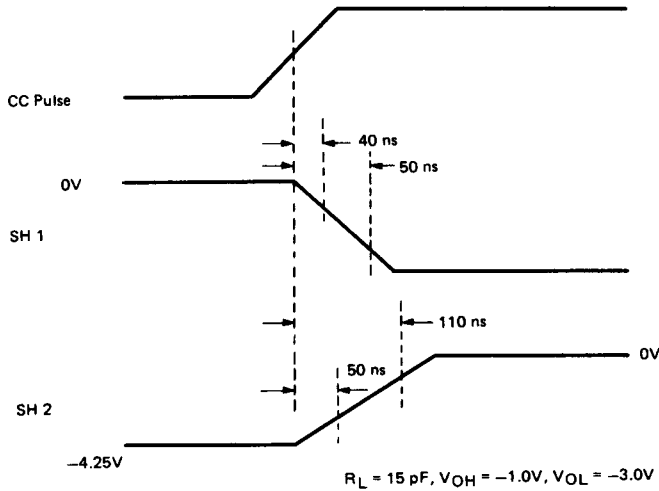
(5) Stereo mode, Monaural mode

Stereo or Monaural modes can be selected by mode pin. And "ON" or "OFF" state of Sample/Hold Pulse is selected similarly.

This is illustrated in the following way.

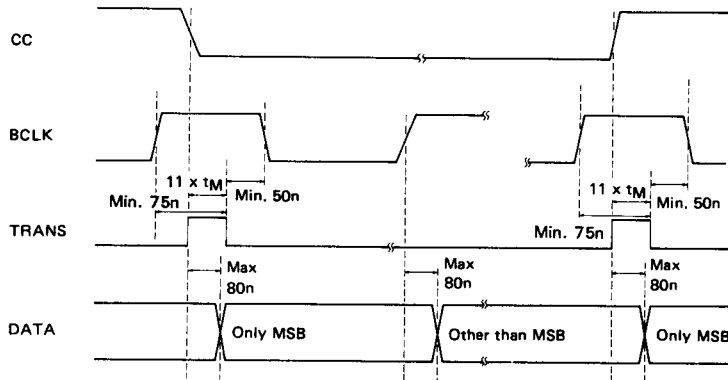


S/H Pulse



Propagation Delay Times from CC input to SH1, SH2 output

(6) Data Out

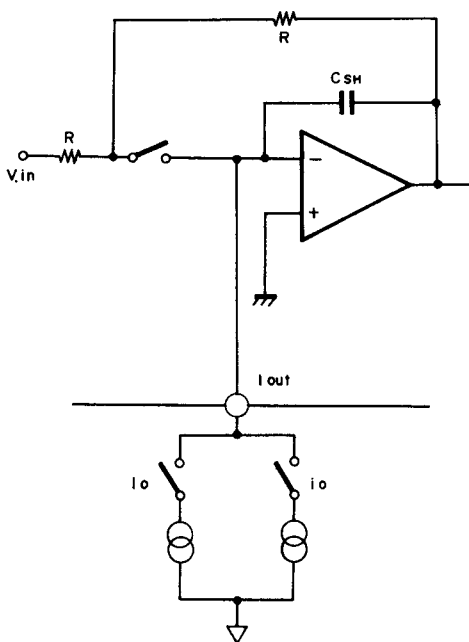


Propagation Delay Time from CC or BCLK Data Out
The maximum frequency of BCLK = 4 MHz

(Only MSB is delayed against the CC pulse.)
(Others are delayed against the bit clock.)
 t_M : One cycle of master clock

(7) Relationship of $V_{in\ max}$, CSH, I_{set} , I_o and i_o

- (1) V_{in} is defined as the input voltage of integrator.
- (2) I_o , i_o are defined as the coarse and fine integration current respectively.
- (3) In case of a full scale input voltage.



$$V_{in\ max} = \frac{I_o \tau_o}{CSH} (2^9 - 1) + \frac{i_o \tau_o}{CSH} (2^7 - 1)$$

$$\text{Using } I_o = 4I_{set}, i_o = \frac{1}{32} I_{set}$$

$$V_{in\ max} = \frac{1}{32} \cdot \frac{I_{set} \tau_o}{CSH} (2^{16} - 1)$$

$$\text{Assuming } V_{in\ max} = 10\ V_{p-p}, \tau_o = \frac{1}{f} = \frac{1}{84.6\ MHz}$$

$$CSH = 1500\ PF$$

$$\therefore I_{set} = 620\ \mu A$$

$$\therefore 1\ LSB = \frac{i_o \tau_o}{CSH} = 152\ \mu V$$

Note) In case of non-inverting operation, $V_{in\ max}$ is limited to 5 V_{p-p}.

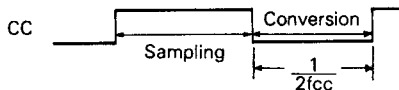
(8) Select guide of f_{MCLK} , f_{BCLK} and f_{cc} .

(1) In case of CX20018

(a) Stereo mode

f_{MCLK} , f_{BCLK} and f_{cc} are the frequency of MCLK, BCLK and CC, respectively. The following relation should be followed:

$$\begin{aligned} f_{MCLK} &\leq 100\text{MHz} \\ f_{BCLK} &\leq 4\text{MHz} \\ f_{cc} &\leq \frac{1}{32} f_{BCLK} \\ \frac{1}{2f_{cc}} &\geq \frac{795}{f_{MCLK}} \quad (*) \end{aligned}$$



(*) The minimum number of clock for a conversion is calculated as follows.

$$\underbrace{(2^9 - 2)}_{\text{Upper level Counter}} + 2 \times \underbrace{(2^7 - 1)}_{\text{Lower level counter}} + \underbrace{(2^5 - 1)}_{\text{Timing circuit}} = 795 \text{ clocks}$$

Namely,

$$32f_{cc} \leq f_{BCLK} \leq 4\text{MHz} \quad \text{...①}$$

$$1590f_{cc} \leq f_{MCLK} \leq 100\text{MHz} \quad \text{...②}$$

For f_{BCLK} , $32f_{cc}$ is recommendable for simple system.

(Example 1)

If f_{cc} is fixed at 44.06 kHz,

$$1.41 \text{ MHz} \leq f_{BCLK} \leq 4 \text{ MHz}$$

($f_{BCLK} = 32f_{cc}$ is recommended.)

$$71 \text{ MHz} \leq f_{MCLK} \leq 100 \text{ MHz}$$

(Example 2)

If f_{MCLK} is 100 MHz,

$$f_{cc} \leq 62 \text{ kHz}$$

$$32f_{cc} \leq f_{BCLK} \leq 4 \text{ MHz}$$

($f_{BCLK} = 32f_{cc}$ is recommended.)

(Example 3)

If f_{BCLK} is 4 MHz,

$$f_{cc} \leq 62 \text{ kHz}$$

$$1590f_{cc} \leq f_{MCLK} \leq 100 \text{ MHz}$$

(b) Monaural mode

Using slower f_{MCLK} or realizing faster conversion time is possible by changing the duty of CC.

Assuming the duty of CC is X%, the following relation should be followed:

$$f_{MCLK} \leq 100 \text{ MHz}$$

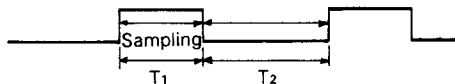
$$f_{BCLK} \leq 4 \text{ MHz}$$

$$T_1 \geq \frac{16}{f_{BCLK}}$$

$$T_2 \geq \frac{795}{f_{MCLK}} \quad (*)$$

$$T_1 + T_2 = \frac{1}{f_{cc}}$$

$$T_1 : T_2 = X : 100 - X$$



These lead to

$$\frac{1600}{X} f_{cc} \leq f_{BCLK} \leq 4 \text{ MHz} \quad \text{...③}$$

$$\frac{79500}{100 - X} f_{cc} \leq f_{MCLK} \leq 100 \text{ MHz} \quad \text{...④}$$

For f_{BCLK} , $\frac{1600}{X}$ (i.e. $\frac{16}{T_1}$) is recommendable for simple system.

(Example 1)

If fcc is 44.06 kHz,

$$\frac{70.5 \text{ MHz}}{X} \leq f_{\text{BCLK}} \leq 4 \text{ MHz}$$

($f_{\text{BCLK}} = \frac{70.5 \text{ MHz}}{X}$ is recommended)

$$\frac{3500 \text{ MHz}}{100 - X} \leq f_{\text{MCLK}} \leq 100 \text{ MHz}$$

In a simple case where $X = 25$ and $f_{\text{BCLK}} = \frac{70.5 \text{ MHz}}{X}$,
 $f_{\text{BCLK}} = 2.82 \text{ MHz}$,

$47 \text{ MHz} \leq f_{\text{MCLK}} \leq 100 \text{ MHz} \rightarrow f_{\text{MCLK}}$ can be 47 MHz.

(Example 2)

If $f_{\text{MCLK}} = 100 \text{ MHz}$,

$$f_{\text{CC}} \leq \text{Min} \left(\frac{100 - X}{795} \text{ MHz}, \frac{X}{400} \text{ MHz} \right)$$

$$\frac{1600}{X} f_{\text{CC}} \leq f_{\text{BCLK}} \leq 4 \text{ MHz}$$

($f_{\text{BCLK}} = \frac{1600}{X} f_{\text{CC}}$ is recommended)

$T_1 \geq \frac{16}{f_{\text{BCLK}}}$, $T_2 \geq 8 \mu\text{sec}$ \rightarrow Conversion time can be $8 \mu\text{sec}$.

(Example 3)

If $f_{\text{BCLK}} = 4 \text{ MHz}$,

$$f_{\text{CC}} \leq \text{Min} \left(\frac{100 - X}{795} \text{ MHz}, \frac{X}{400} \text{ MHz} \right)$$

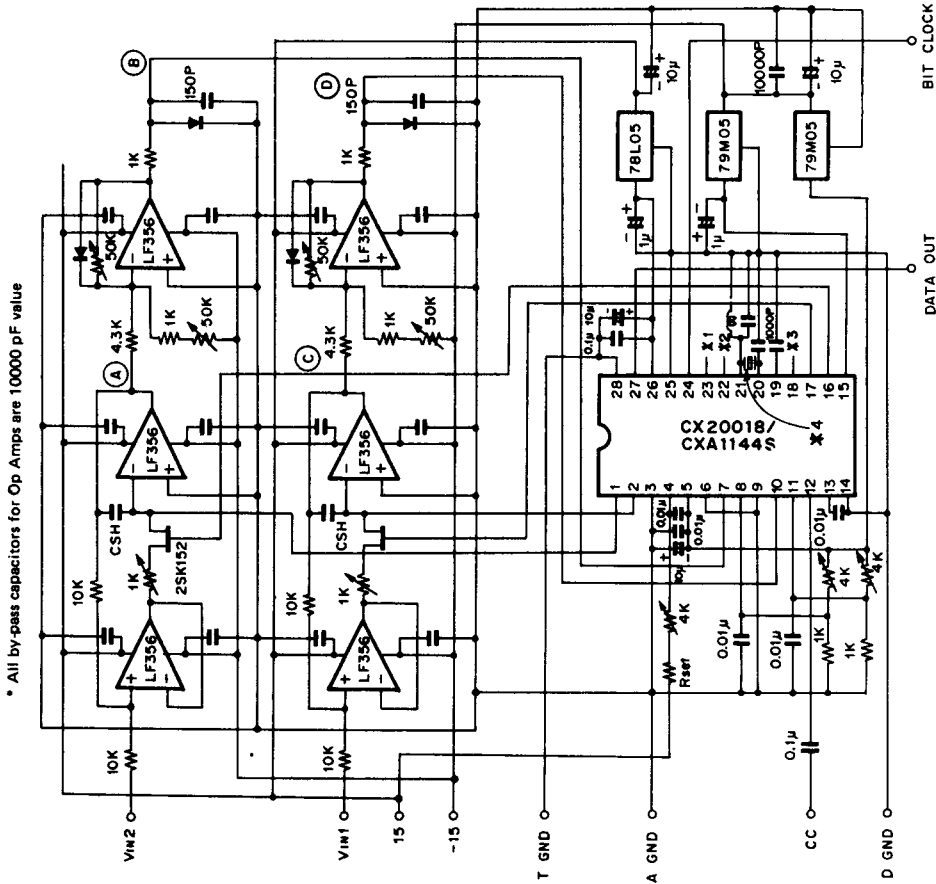
$$\frac{79500}{100 - X} f_{\text{CC}} \leq f_{\text{MCLK}} \leq 100 \text{ MHz}$$

$T_1 \geq 4 \mu\text{sec}$, $T_2 \geq \frac{795}{f_{\text{MCLK}}} (\geq 8 \mu\text{sec}) \rightarrow$ Short conversion time can be obtained.

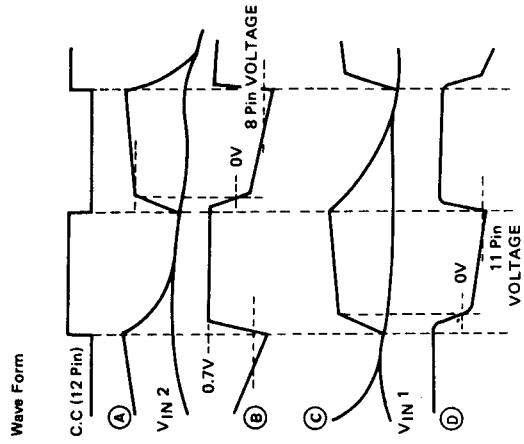
(2) In case of CXA1144S

The same as CX20018 except $f_{\text{MCLK}} \leq 95 \text{ MHz}$.

Typical Application
16 Bit A/D Converter Peripheral
Circuit (Stereo Mode)



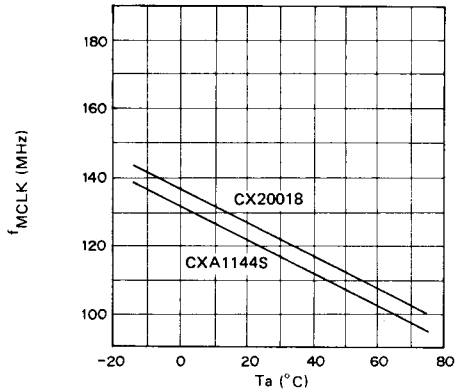
* All by-pass capacitors for Op Amps are 10000 pF value



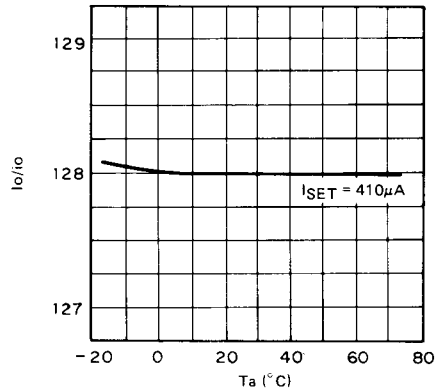
- * 1, 2, 3: See to Page 13 and 14.
- * Rset, CSH: See to Page 16.
(Rset = 42 kΩ when Iset = 410 µA, Rset = 22 kΩ when Iset = 750 µA.)
- * 4: HC43/U (American KSS), etc.

Fig. 5 16 bit A/D Converter Peripheral Circuit (Stereo Mode)

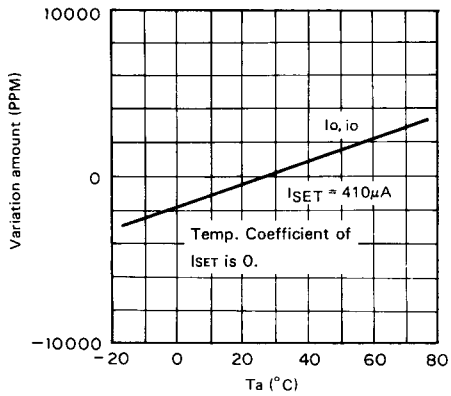
fmCLK temperature characteristics



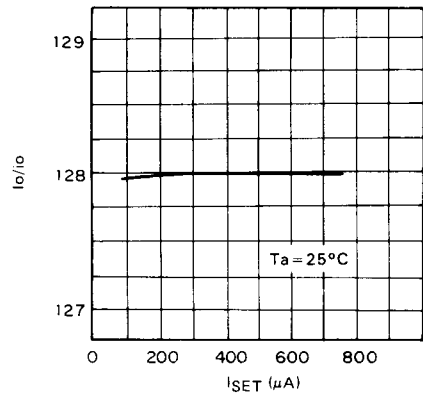
Current ratio temperature characteristics



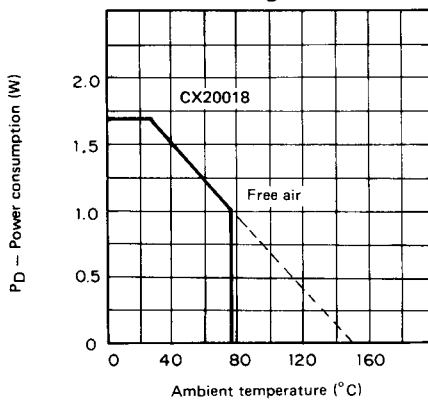
Output current temperature characteristics



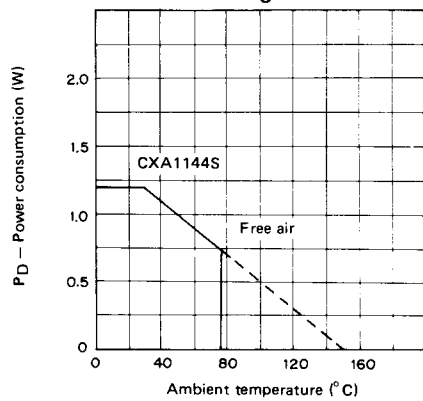
Current ratio vs. ISET



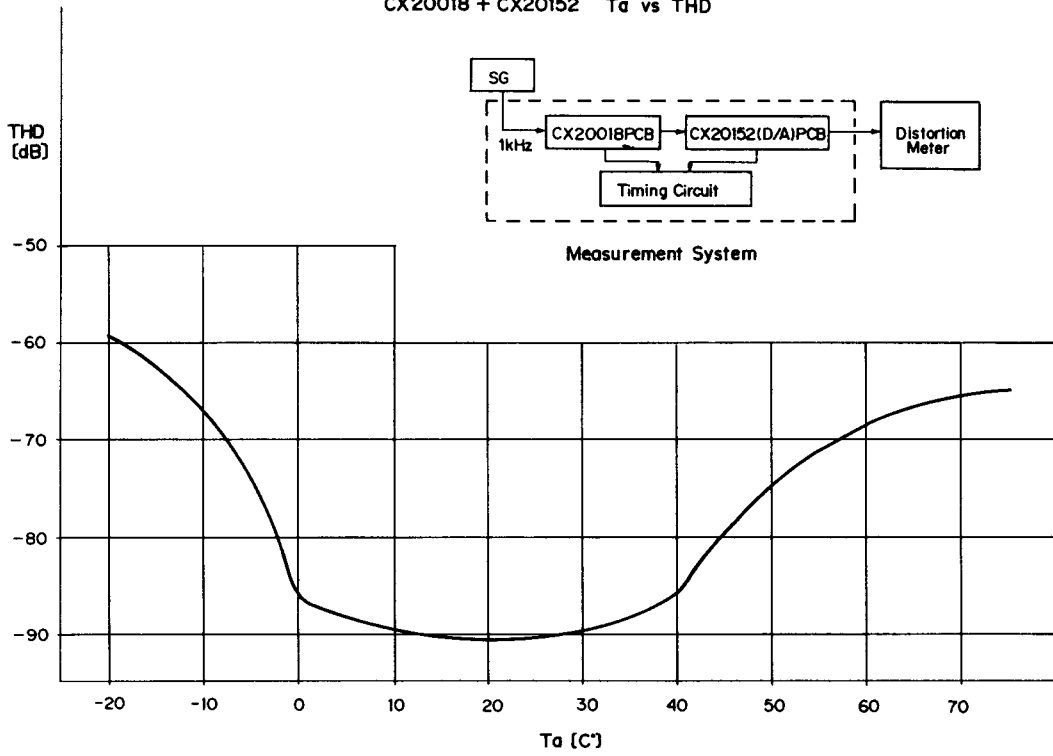
Derating curve



Derating curve



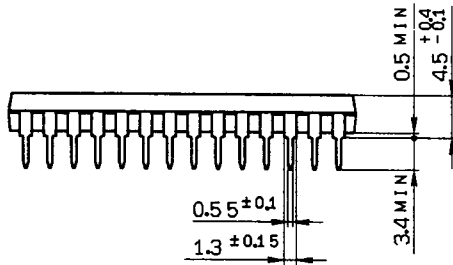
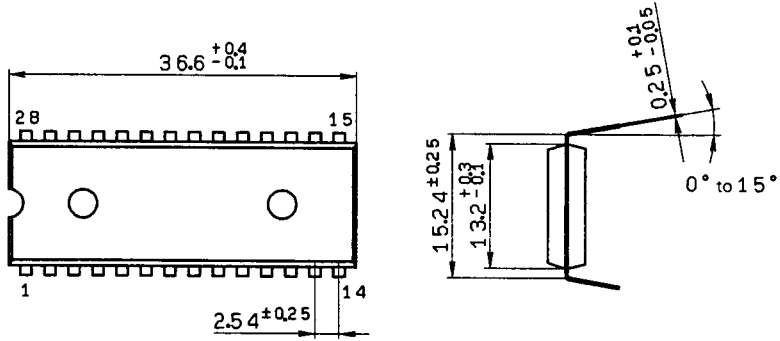
CX20018 + CX20152 T_a vs THD



Package Outline

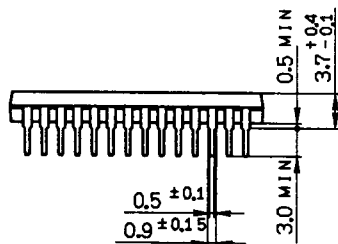
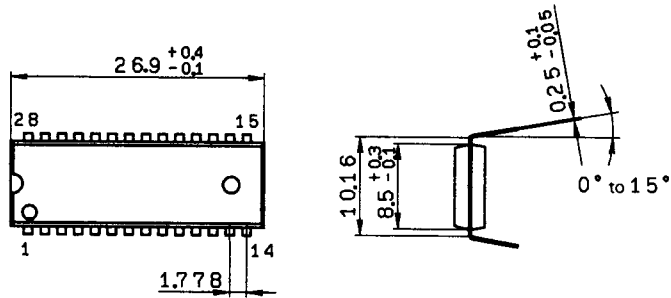
Unit: mm

CX20018 28 pin DIP (Plastic) 600 mil 4.0g



DIP-28P-02

CXA1144S 28 pin SDIP (Plastic) 400 mil 1.7g



SDIP-28P-01

T-90-20

Sony Package Product Name

Type	Package name		Package	Features				
	Symbol	Description		Material*	Lead pitch	Lead shape	Lead pull out direction	
Inserted	Standard	DIP	DUAL IN LINE PACKAGE		P C	2.54mm (100MIL)	Through Hole Lead	2-direction
		SIP	SINGLE IN LINE PACKAGE		P	2.54mm (100MIL)	Through Hole Lead	1-direction
		ZIP	ZIG ZAG IN LINE PACKAGE		P	2.54mm (100MIL) Zig Zag inline	Through Hole Lead	1-direction
		PGA	PIN GRID ARRAY		C	2.54mm (100MIL)	Through Hole Lead	4-direction
		PIGGY BACK	PIGGY BACK		C	2.54mm (100MIL)	Through Hole Lead	2-direction
Shrink	SDIP	SHRINK DUAL IN LINE PACKAGE		P	1.778mm (70MIL)	Through Hole Lead	2-direction	
Surface mounted	Standard flat package	QFP	QUAD FLAT PACKAGE		P	1.0mm 0.8mm	Gull-Wing	4-direction
		SOP	SMALL-OUTLINE PACKAGE		P	1.27mm (50MIL)	Gull-Wing	2-direction
	Shrink flat package	VQFP	VERY SMALL QUAD FLAT PACKAGE		P	0.5mm	Gull-Wing	4-direction
		VSOP	VERY SMALL OUTLINE PACKAGE		P	0.65mm	Gull Wing	2-direction
	Standard chip carrier	PLCC	PLASTIC LEADED CHIP CARRIER		P	1.27mm (50MIL)	J-bend	4-direction
		LCC	LEAD LESS CHIP CARRIER		C	1.27mm (50MIL)	Lead less	Package side
	Shrink chip carrier	SPLCC (PLCC)	SHRINK PLASTIC LEADED CHIP CARRIER		P	1.27mm Max. (50MIL Max.)	J-bend	4-direction
	Standard 2-direction chip carrier	SOJ	SMALL OUTLINE J-LEAD PACKAGE		P	1.27mm (50MIL)	J-bend	2-direction



*P.....Plastic, C.....Ceramic

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