

Features

- Pin- and function-compatible with CY7C1020CV33
- Temperature Ranges
 - Commercial: 0 °C to 70 °C
 - Industrial: -40 °C to 85 °C
 - Automotive: -40 °C to 125 °C
- High speed
 - $t_{AA} = 10$ ns
- CMOS for optimum speed/power
- Low active power
 - 325 mW (max)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin TSOP II package

Functional Description

The CY7C1020CV33 is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

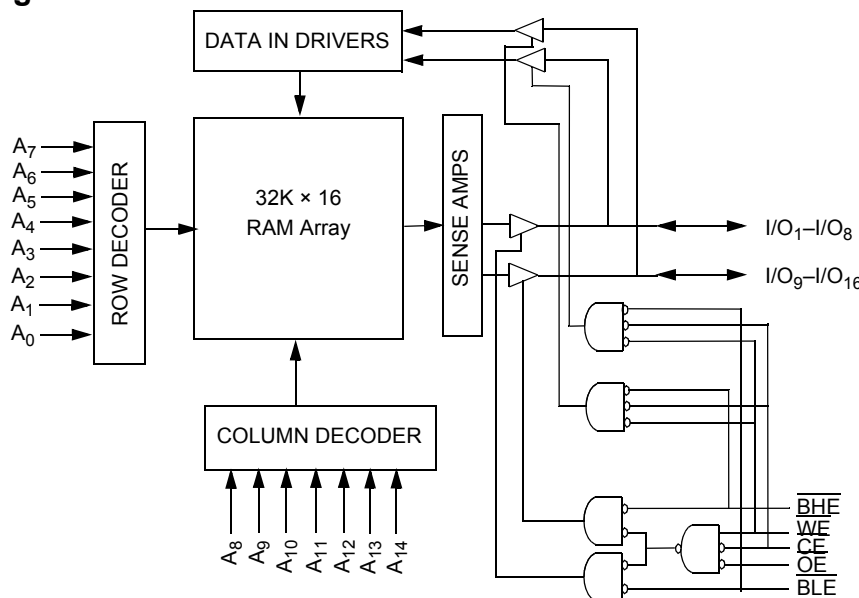
Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (WE) inputs LOW. If Byte Low Enable (BLE) is LOW, then data from I/O pins (I/O₁ through I/O₈), is written into the location specified on the address pins (A₀ through A₁₄). If Byte High Enable (BHE) is LOW, then data from I/O pins (I/O₉ through I/O₁₆) is written into the location specified on the address pins (A₀ through A₁₄).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on I/O₁ to I/O₈. If Byte High Enable (BHE) is LOW, then data from memory will appear on I/O₉ to I/O₁₆. See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O₁ through I/O₁₆) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the BHE and \overline{BLE} are disabled (BHE, \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and WE LOW).

The CY7C1020CV33 is available in standard 44-pin TSOP Type II package.

Logic Block Diagram



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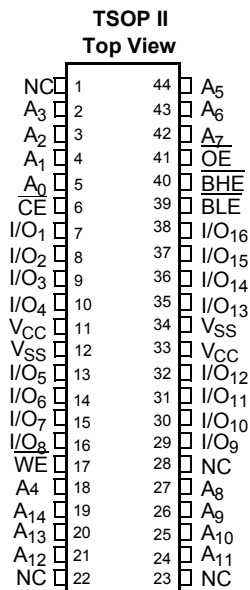
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Selection Guide

Description		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Commercial/Industrial	90	85	80	mA
	Automotive	–	–	85	mA
Maximum CMOS Standby Current	Commercial/Industrial	5	5	5	mA
	Automotive	–	–	10	mA

Pin Configuration

Figure 1. 44-pin TSOP Type II pinout (Top View) ^[1]



Note

1. NC pins are not connected on the die.

Pin Definitions

Pin Name	Pin Number	I/O Type	Description
A ₀ –A ₁₄	5, 4, 3, 2, 18, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19	Input	Address Inputs used to select one of the address locations.
I/O ₁ –I/O ₁₆	7–10, 13–16, 29–32, 35–38	Input/Output	Bidirectional Data I/O lines. Used as input or output lines depending on operation.
NC	1, 22, 23, 28	No Connect	No Connects. Not connected to the die.
$\overline{\text{WE}}$	17	Input/Control	Write Enable Input, active LOW. When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
$\overline{\text{CE}}$	6	Input/Control	Chip Enable Input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{\text{BHE}}, \overline{\text{BLE}}$	40, 39	Input/Control	Byte Write Select Inputs, active LOW. $\overline{\text{BHE}}$ controls I/O ₁₆ –I/O ₉ , $\overline{\text{BLE}}$ controls I/O ₈ –I/O ₁ .
$\overline{\text{OE}}$	41	Input/Control	Output Enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V _{SS}	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V _{CC}	11, 33	Power Supply	Power Supply inputs to the device.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage on V_{CC} to relative GND [2] -0.5 V to +4.6 V
 DC voltage applied to outputs in high Z State [2] -0.5 V to $V_{CC} + 0.5$ V
 DC input voltage [2] -0.5 V to $V_{CC} + 0.5$ V

Current into outputs (LOW) 20 mA
 Static discharge voltage (per MIL-STD-883, method 3015) > 2001 V
 Latch-up current > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0 °C to +70 °C	3.3 V ± 10%
Industrial	-40 °C to +85 °C	3.3 V ± 10%
Automotive	-40 °C to +125 °C	3.3 V ± 10%

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		-15		Unit	
			Min	Max	Min	Max	Min	Max		
V_{OH}	Output HIGH voltage	$V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$	2.4	-	2.4	-	2.4	-	V	
V_{OL}	Output LOW voltage	$V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$	-	0.4	-	0.4	-	0.4	V	
V_{IH}	Input HIGH voltage		2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	2.0	$V_{CC} + 0.3$	V	
V_{IL}	Input LOW voltage [2]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V	
I_{IX}	Input leakage current	$GND \leq V_I \leq V_{CC}$	Commercial / Industrial	-1	+1	-1	+1	-1	+1	μA
			Automotive	-	-	-	-	-20	+20	μA
I_{OZ}	Output leakage current	$GND \leq V_I \leq V_{CC}$, Output Disabled	Commercial / Industrial	-1	+1	-1	+1	-1	+1	μA
			Automotive	-	-	-	-	-20	+20	μA
I_{CC}	V_{CC} operating supply current	$V_{CC} = \text{Max}, I_{OUT} = 0 \text{ mA}, f = f_{MAX} = 1/t_{RC}$	Commercial / Industrial	-	90	-	85	-	80	mA
			Automotive	-	-	-	-	-	85	mA
I_{SB1}	Automatic CE power-down current – TTL Inputs	Max V_{CC} , CE $\geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$	Commercial / Industrial	-	15	-	15	-	15	mA
			Automotive	-	-	-	-	-	20	mA
I_{SB2}	Automatic CE power-down current – CMOS inputs	Max V_{CC} , CE $\geq V_{CC} - 0.3 \text{ V}$, $V_{IN} \geq V_{CC} - 0.3 \text{ V}$, or $V_{IN} \leq 0.3 \text{ V}$, $f = 0$	Commercial / Industrial	-	5	-	5	-	5	mA
			Automotive	-	-	-	-	-	10	mA

Note

2. $V_{IL}(\text{min}) = -2.0 \text{ V}$ and $V_{IH}(\text{max}) = V_{CC} + 0.5 \text{ V}$ for pulse durations of less than 20 ns.

Capacitance

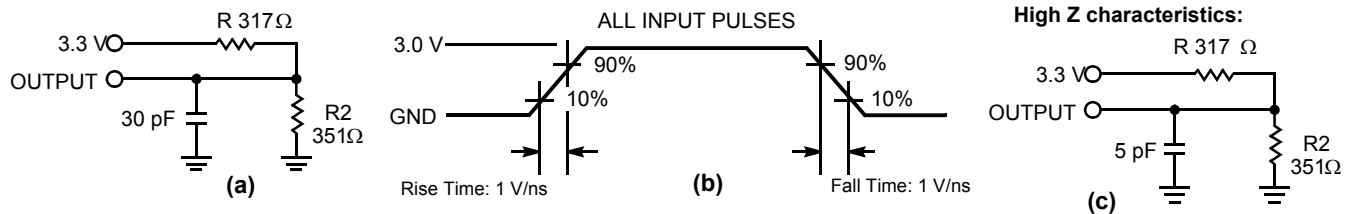
Parameter ^[3]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.3 V	8	pF
C _{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter ^[3]	Description	Test Conditions	44-pin TSOP-II	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	76.92	°C/W
Θ _{JC}	Thermal resistance (junction to case)		15.86	°C/W

AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms ^[4]



Notes

- 3. Tested initially and after any design or process changes that may affect these parameters.
- 4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.

Switching Characteristics

Over the Operating Range

Parameter ^[5]	Description	-10		-12		-15		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle								
t_{RC}	Read cycle time	10	–	12	–	15	–	ns
t_{AA}	Address to data valid	–	10	–	12	–	15	ns
t_{OHA}	Data hold from address change	3	–	3	–	3	–	ns
t_{ACE}	\overline{CE} LOW to data valid	–	10	–	12	–	15	ns
t_{DOE}	\overline{OE} LOW to data valid	–	5	–	6	–	7	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[6]	0	–	0	–	0	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[6, 7]	–	5	–	6	–	7	ns
t_{LZCE}	\overline{CE} LOW to low Z ^[6]	3	–	3	–	3	–	ns
t_{HZCE}	\overline{CE} HIGH to high Z ^[6, 7]	–	5	–	6	–	7	ns
$t_{PU}^{[8]}$	\overline{CE} LOW to power-up	0	–	0	–	0	–	ns
$t_{PD}^{[8]}$	\overline{CE} HIGH to power-down	–	10	–	12	–	15	ns
t_{DBE}	Byte enable to data valid	–	5	–	6	–	7	ns
t_{LZBE}	Byte enable to low Z	0	–	0	–	0	–	ns
t_{HZBE}	Byte disable to high Z	–	5	–	6	–	7	ns
Write Cycle^[9]								
t_{WC}	Write cycle time	10	–	12	–	15	–	ns
t_{SCE}	\overline{CE} LOW to write end	8	–	9	–	10	–	ns
t_{AW}	Address set-up to write end	7	–	8	–	10	–	ns
t_{HA}	Address hold from write end	0	–	0	–	0	–	ns
t_{SA}	Address set-up to write start	0	–	0	–	0	–	ns
t_{PWE}	\overline{WE} pulse width	7	–	8	–	10	–	ns
t_{SD}	Data set-up to write end	5	–	6	–	8	–	ns
t_{HD}	Data hold from write end	0	–	0	–	0	–	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[6]	3	–	3	–	3	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[6, 7]	–	5	–	6	–	7	ns
t_{BW}	Byte enable to end of write	7	–	8	–	9	–	ns

Notes

- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
- t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE}/\overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

Switching Waveforms

Figure 3. Read Cycle No. 1 [10, 11]

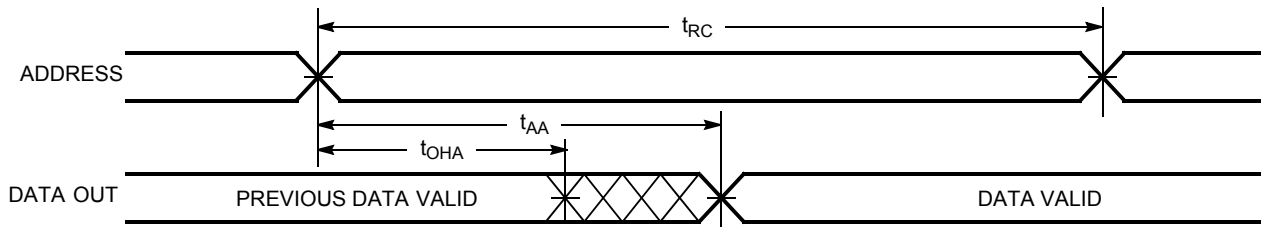
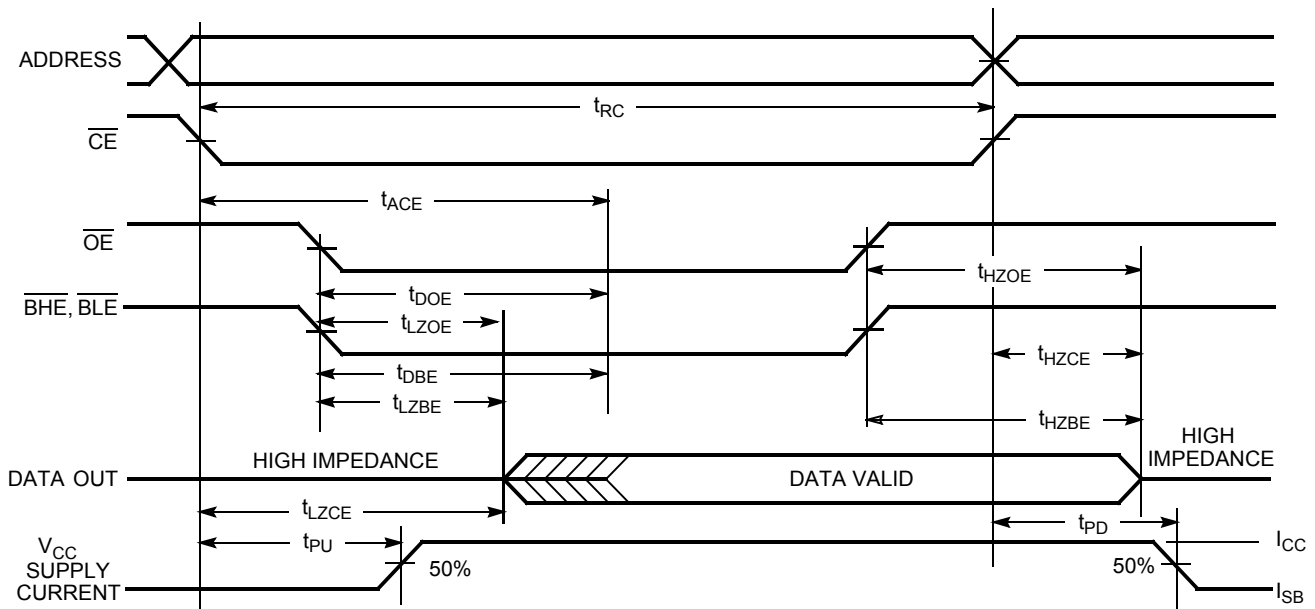


Figure 4. Read Cycle No. 2 (\overline{OE} Controlled) [11, 12]



Notes

- 10. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLA} = V_{IL} .
- 11. \overline{WE} is HIGH for Read cycle.
- 12. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled) [13, 14]

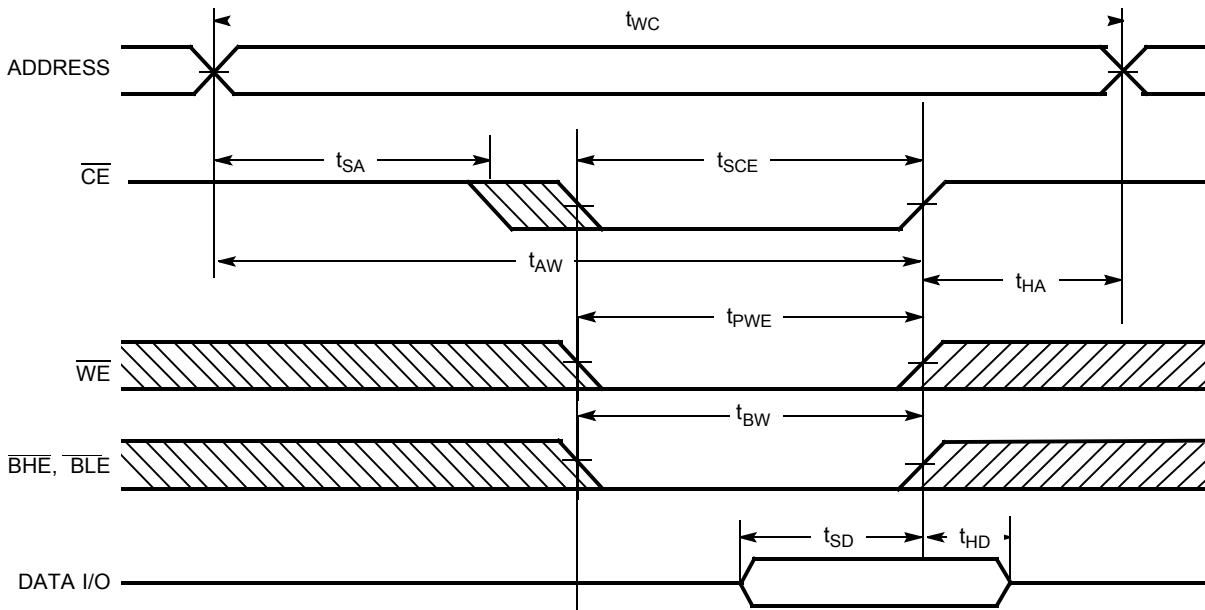
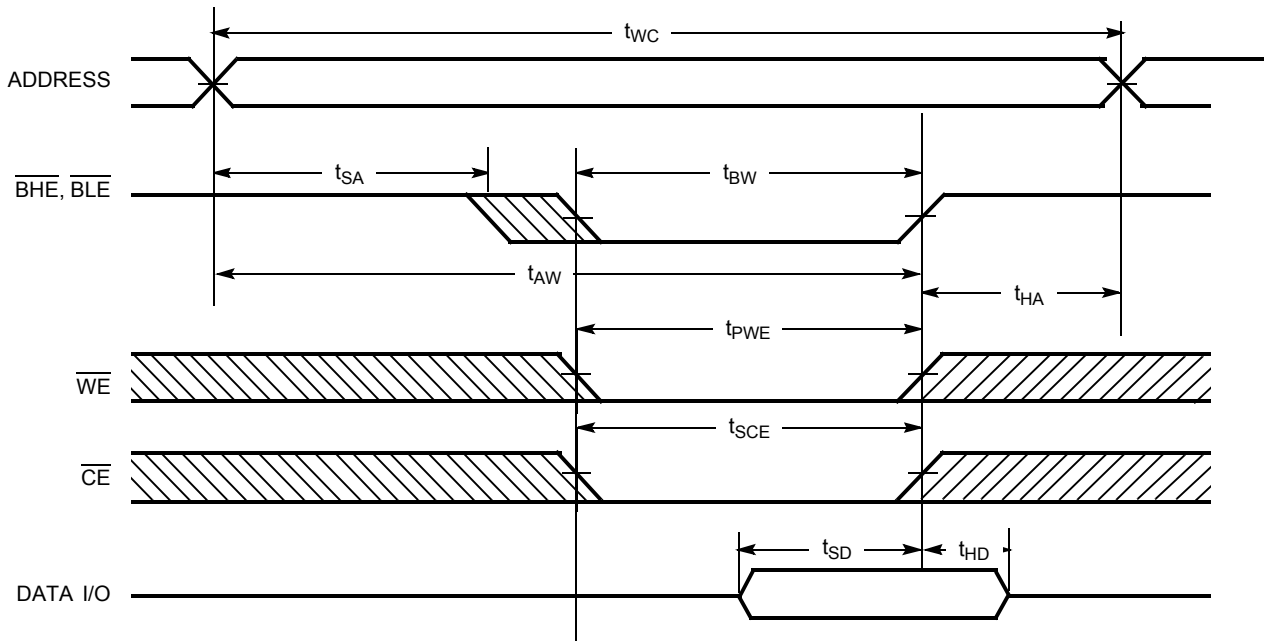


Figure 6. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

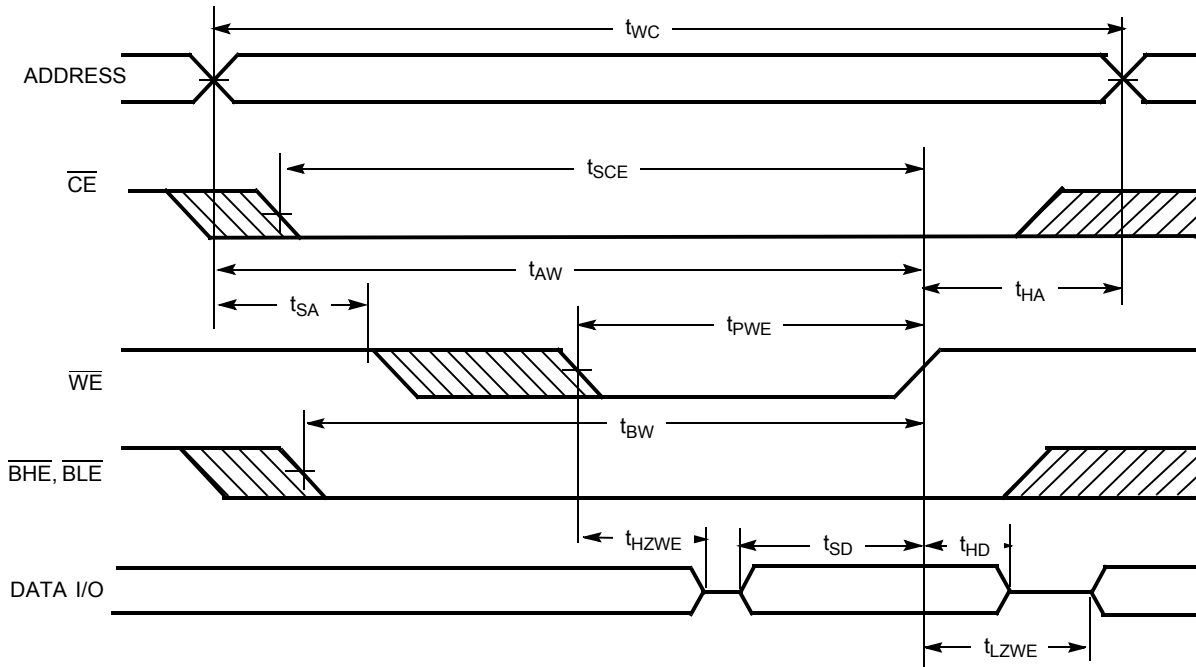


Notes

- 13. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{\text{IH}}$.
- 14. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 7. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)



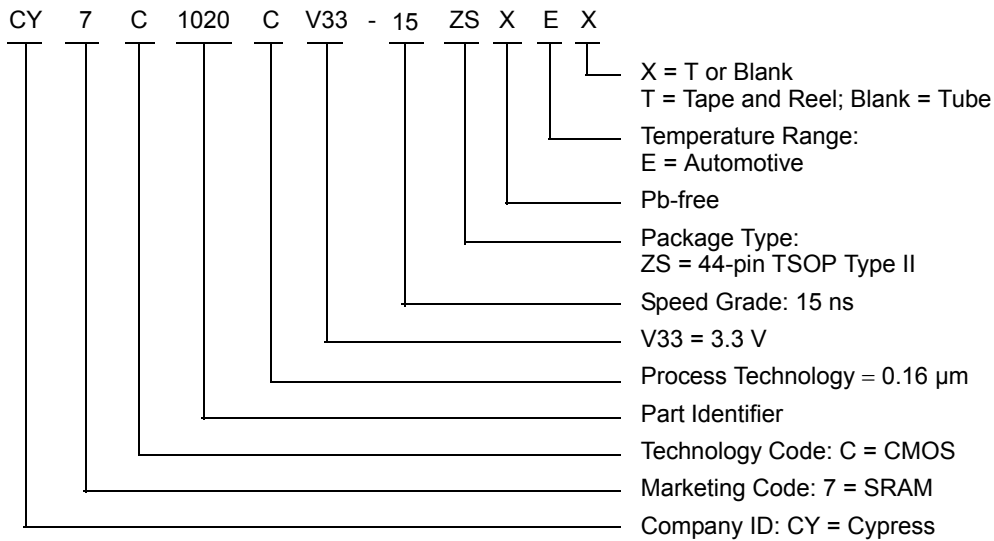
Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{BLE}	\overline{BHE}	I/O ₁ –I/O ₈	I/O ₉ –I/O ₁₆	Mode	Power
H	X	X	X	X	High Z	High Z	Power-down	Standby (I _{SB})
L	L	H	L	L	Data out	Data out	Read – All bits	Active (I _{CC})
			L	H	Data out	High Z	Read – Lower bits only	Active (I _{CC})
			H	L	High Z	Data out	Read – Upper bits only	Active (I _{CC})
L	X	L	L	L	Data in	Data in	Write – All bits	Active (I _{CC})
			L	H	Data in	High Z	Write – Lower bits only	Active (I _{CC})
			H	L	High Z	Data in	Write – Upper bits only	Active (I _{CC})
L	H	H	X	X	High Z	High Z	Selected, outputs disabled	Active (I _{CC})
L	X	X	H	H	High Z	High Z	Selected, outputs disabled	Active (I _{CC})

Ordering Information

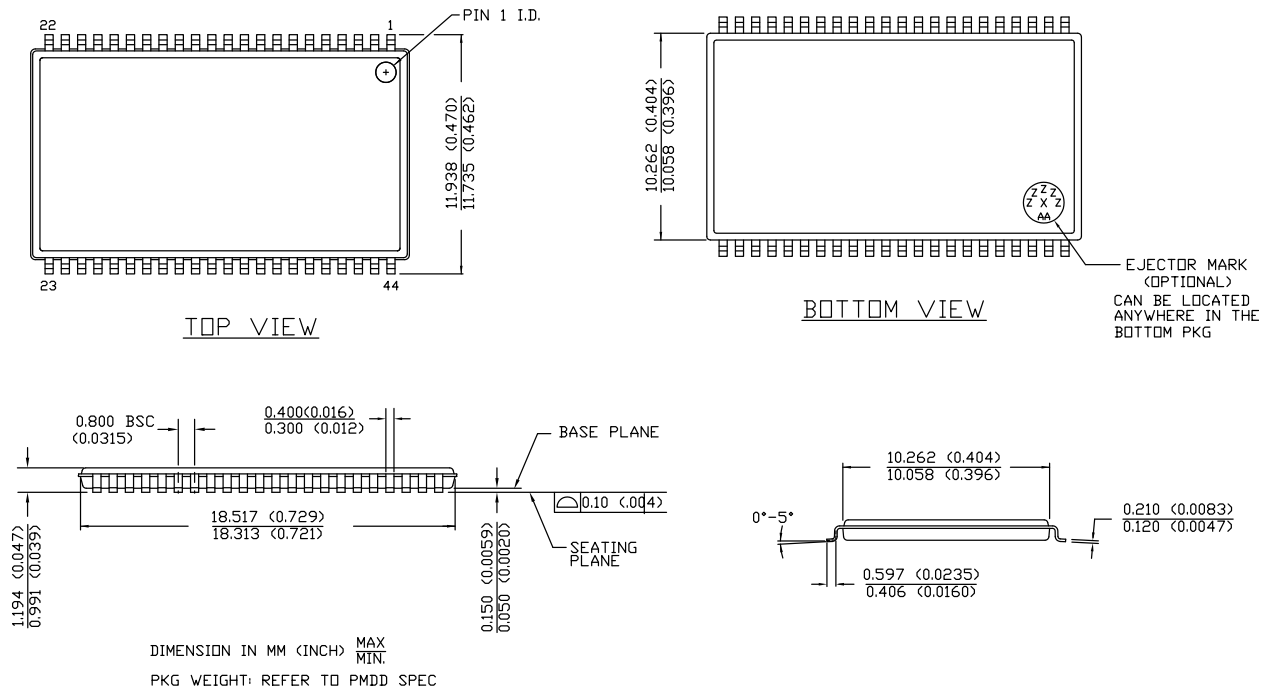
Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
15	CY7C1020CV33-15ZSX E	51-85087	44-pin TSOP Type II (Pb-free)	Automotive
	CY7C1020CV33-15ZSX ET	51-85087	44-pin TSOP Type II (Pb-free)	Automotive

Ordering Code Definitions



Package Diagrams

Figure 8. 44-pin TSOP Z44-II Package Outline, 51-85087



51-85087 *E

Acronyms

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
$\overline{\text{CE}}$	Chip Enable
I/O	Input/Output
$\overline{\text{OE}}$	Output Enable
SRAM	Static Random Access Memory
TSOP	Thin Small-Outline Package
TTL	Transistor-Transistor Logic
$\overline{\text{WE}}$	Write Enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μA	microampere
mA	milliampere
mW	milliwatt
ns	nanosecond
%	percent
pF	picofarad
V	volt
W	watt

Document History Page

Document Title: CY7C1020CV33, 512 K (32 K × 16) Static RAM Document Number: 38-05133				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	109428	12/16/01	HGK	New data sheet.
*A	115045	05/30/02	HGK	I _{CC} and I _{SB1} data modified
*B	117615	08/14/02	DFP	Pin 1= NC Pin 18 = A4; remove SOJ package option; remove 8ns option.
*C	262949	See ECN	RKF	Added Automotive Specs to Data sheet
*D	334398	See ECN	SYT	Added Lead-Free Product Information
*E	493543	See ECN	NXR	Added note #1 on page #1 Changed the description of I _{Ix} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I _{OS} parameter from DC Electrical Characteristics table Updated Ordering Information Table
*F	2897691	03/23/2010	RAME	Updated Ordering Information Updated Package Diagrams .
*G	3057593	10/13/2010	PRAS	Updated Ordering Information and added Ordering Code Definitions .
*H	3100106	12/02/2010	PRAS	Added Acronyms and Units of Measure . Minor edits and updated in new template.
*I	4146968	10/04/2013	VINI	Updated Package Diagrams : spec 51-85087 – Changed revision from *C to *E. Updated in new template. Completing Sunset Review.

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