

Quad Complementary CMOS Analog Switch

Features

- ± 22 -V Supply Voltage Rating
- TTL and CMOS Compatible Logic
- Low On-Resistance— $r_{DS(on)}$: 45 Ω
- Low Leakage— $I_{D(on)}$: 20 pA
- Single Supply Operation Possible
- Extended Temperature Range
- Fast Switching— t_{ON} : 85 ns

Benefits

- Low Charge Injection—Q: 1 pC
- Wide Analog Signal Range
- Simple Logic Interface
- Higher Accuracy
- Minimum Transients
- Reduced Power Consumption
- Low Cost

Applications

- Industrial Instrumentation
- Test Equipment
- Communications Systems
- Computer Peripherals
- Portable Instruments
- Sample-and-Hold Circuits

Description

The versatile DG213 analog switch has two NC and two NO switches. It can be used in various configurations, including four single-pole single-throw (SPST), two single-pole double-throw (SPDT), one "T" switch, one DPDT, etc. This device is fabricated in a Siliconix' proprietary high-voltage silicon gate CMOS process, resulting in lower on-resistance, lower leakage, higher speed, and lower power consumption.

This analog switch was designed for a wide variety of general purpose applications in telecommunications, instrumentation, process control, computer peripherals, etc.

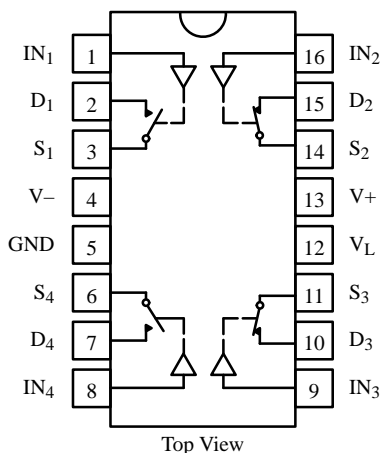
An improved charge injection compensation design minimizes switching transients. These switches can handle up to ± 22 V, and have an improved continuous current rating of 30 mA. An epitaxial layer prevents latchup.

All switches feature true bi-directional performance in the on condition, and will block signals to the supply levels in the off condition.

For additional information, please refer to Application Note AN208.

Functional Block Diagram and Pin Configuration

DG213



Truth Table

Logic	SW ₁ , SW ₄	SW ₂ , SW ₃
0	OFF	ON
1	ON	OFF

Logic "0" ≤ 0.8 V
Logic "1" ≥ 2.4 V

Ordering Information

Temp Range	Package	Part Number
-40 to 85°C	16-Pin Plastic DIP	DG213DJ
	16-Pin Narrow SOIC	DG213DY
	16-Pin TSSOP	DG213DQ

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #70662. Applications information may also be obtained via FaxBack, request document #70606.

Absolute Maximum Ratings

Voltages Referenced to V-

V+	44 V
GND	25 V
Digital Inputs ^a V _S , V _D	(V-) -2 V to (V+) +2 V or 30 mA, whichever occurs first
Current, Any Terminal	30 mA
Peak Current, S or D (Pulsed at 1 ms, 10% duty cycle max)	100 mA
Storage Temperature	-65 to 125°C

Power Dissipation (Package)^b

16-Pin Plastic DIP ^c	470 mW
16-Pin Narrow SOIC ^d	640 mW
16-Pin TSSOP ^d	500 mW

Notes:

- Signals on S_X, D_X, or IN_X exceeding V+ or V- will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
- All leads welded or soldered to PC Board.
- Derate 6.5 mW/°C above 75°C
- Derate 7.6 mW/°C above 75°C

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V- = -15 V V _L = 5 V, V _{IN} = 2.4 V, 0.8 V ^e	Temp ^a	D Suffix -40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	V-		V+	V
Drain-Source On-Resistance	r _{DS(on)}	V _D = ±10 V, I _S = 1 mA	Room		45	60	Ω
r _{DS(on)} Match	Δr _{DS(on)}		Full			85	
Source Off Leakage Current	I _{S(off)}	V _S = ±14 V, V _D = ∓14 V	Room	-0.5	±0.01	0.5	nA
Drain Off Leakage Current	I _{D(off)}	V _D = ±14 V, V _S = ∓14 V	Full	-5		5	
Drain On Leakage Current	I _{D(on)}	V _S = V _D = 14 V	Room	-0.5	±0.02	0.5	
			Full	-10		10	
Digital Control							
Input Voltage High	V _{INH}		Full	2.4			V
Input Voltage Low	V _{INL}		Full			0.8	
Input Current	I _{INH} or I _{INL}	V _{INH} or V _{INL}	Full	-1		1	μA
Input Capacitance	C _{IN}		Room		5		pF
Dynamic Characteristics							
Turn-On Time	t _{ON}	V _S = 2 V See Figure 2	Room		85	130	ns
Turn-Off Time	t _{OFF}		Room		55	100	
Break-Before-Make Time Delay	t _D	V _S = 10 V, See Figure 3	Room	20	25		
Charge Injection	Q	C _L = 1000 pF, V _g = 0 V, R _g = 0 Ω	Room		1		pC
Source-Off Capacitance	C _{S(off)}	V _S = 0 V, f = 1 MHz	Room		5		pF
Drain-Off Capacitance	C _{D(off)}		Room		5		
Channel On Capacitance	C _{D(on)}	V _D = V _S = 0 V, f = 1 MHz	Room		16		
Off Isolation	OIRR	C _L = 15 pF, R _L = 50 Ω V _S = 1 V _{RMS} , f = 100 kHz	Room		90		dB
Channel-to-Channel Crosstalk	X _{TALK}		Room		95		

Specifications

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 15\text{ V}$, $V_- = -15\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^e	Temp ^a	D Suffix -40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Power Supply							
Positive Supply Current	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			1 5	μA
Negative Supply Current	I-		Room Full	-1 -5			
Logic Supply Current	I _L	Room Full			1 5		
Power Supply Range for Continuous Operation	V _{OP}		Full	±3		±22	V

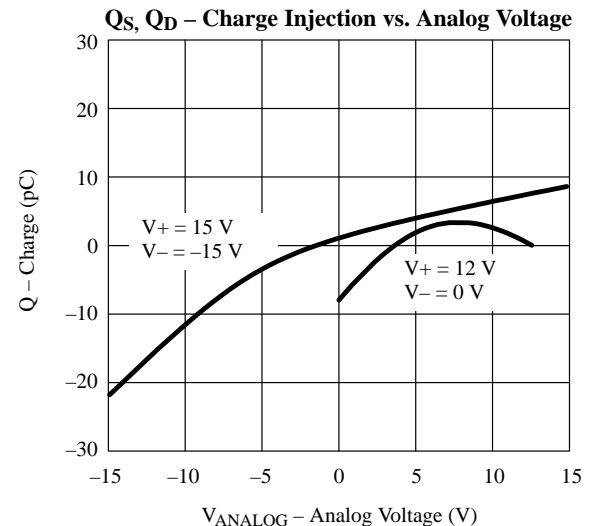
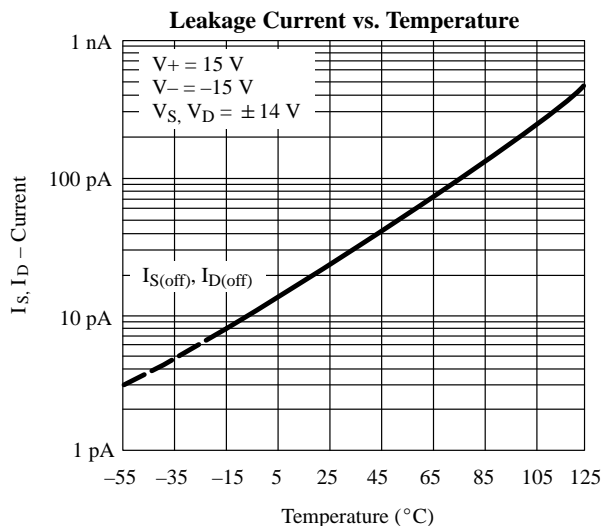
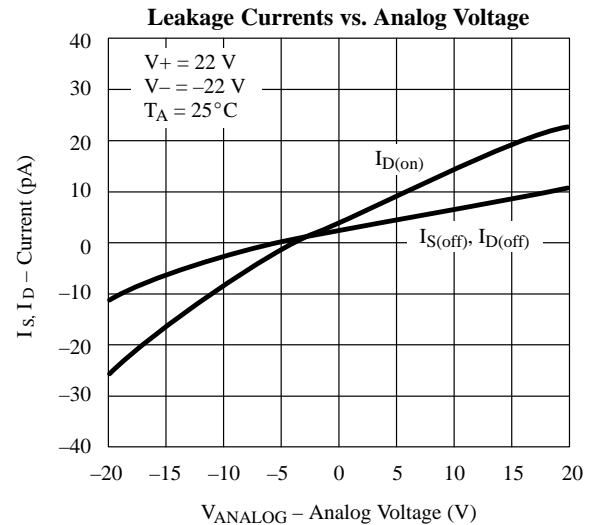
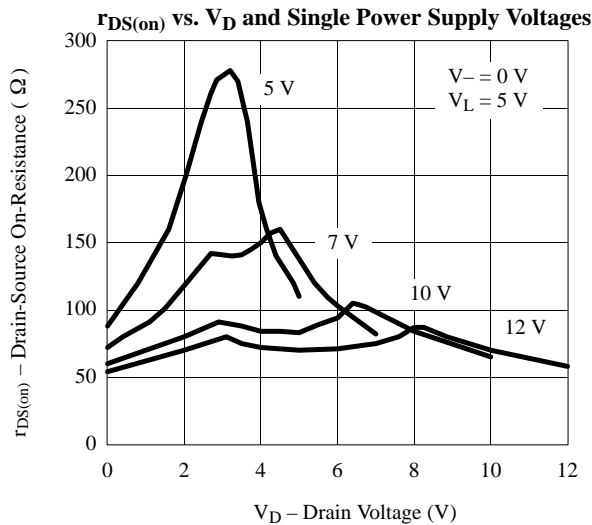
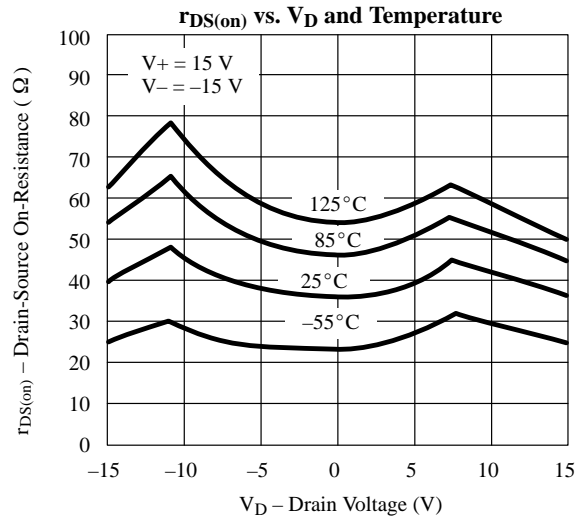
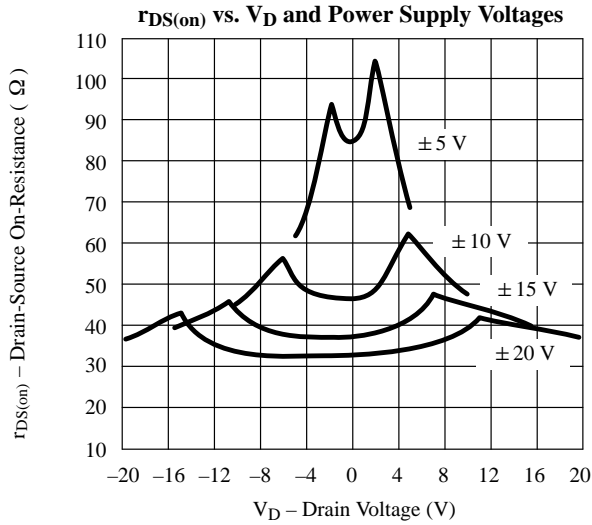
Specifications for Unipolar Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified $V_+ = 12\text{ V}$, $V_- = 0\text{ V}$ $V_L = 5\text{ V}$, $V_{IN} = 2.4\text{ V}$, 0.8 V^e	Temp ^a	D Suffix -40 to 85°C			Unit
				Min ^c	Typ ^b	Max ^c	
Analog Switch							
Analog Signal Range ^d	V _{ANALOG}		Full	V-		V+	V
Drain-Source On-Resistance	r _{DS(on)}	$V_D = 3\text{ V}$, 8 V , $I_S = 1\text{ mA}$	Room Full		90	110 140	Ω
Dynamic Characteristics							
Turn-On Time	t _{ON}	$V_S = 8\text{ V}$ See Figure 2	Room		125	200	ns
Turn-Off Time	t _{OFF}		Room		45	100	
Break-Before-Make Time Delay	t _D	DG213 Only, See Figure 3	Room	50	80		
Charge Injection	Q	$C_L = 1\text{ nF}$, $V_{gen} = 6\text{ V}$, $R_{gen} = 0\text{ Ω}$	Room		4		pC
Power Supply							
Positive Supply Current	I+	$V_{IN} = 0\text{ or }5\text{ V}$	Room Full			1 5	μA
Negative Supply Current	I-		Room Full	-1 -5			
Logic Supply Current	I _L	Room Full			1 5		
Power Supply Range for Continuous Operation	V _{OP}		Full	+3		+40	V

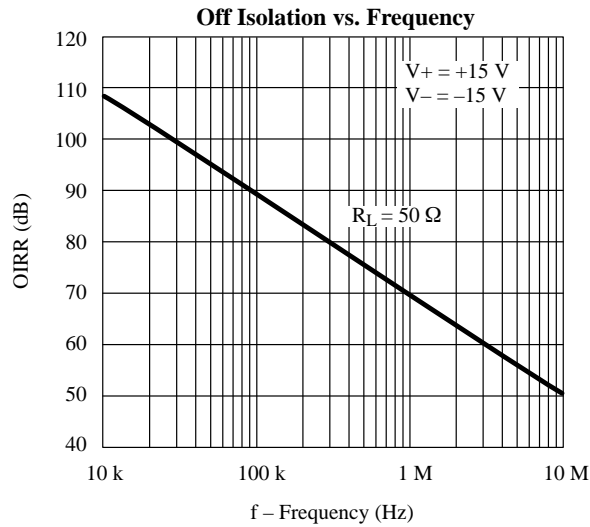
Notes:

- Room = 25°C, Full = as determined by the operating temperature suffix.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Guaranteed by design, not subject to production test.
- V_{IN} = input voltage to perform proper function.

Typical Characteristics



Typical Characteristics (Cont'd)



Schematic Diagram (Typical Channel)

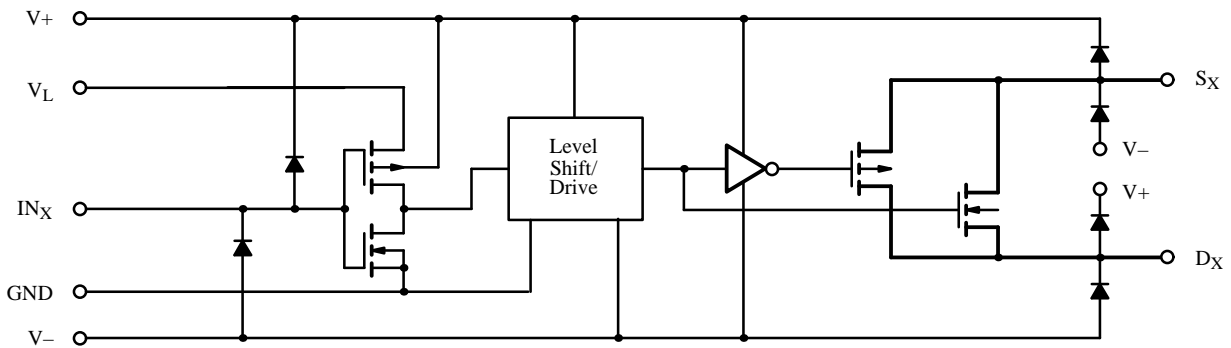


Figure 1.

Test Circuits

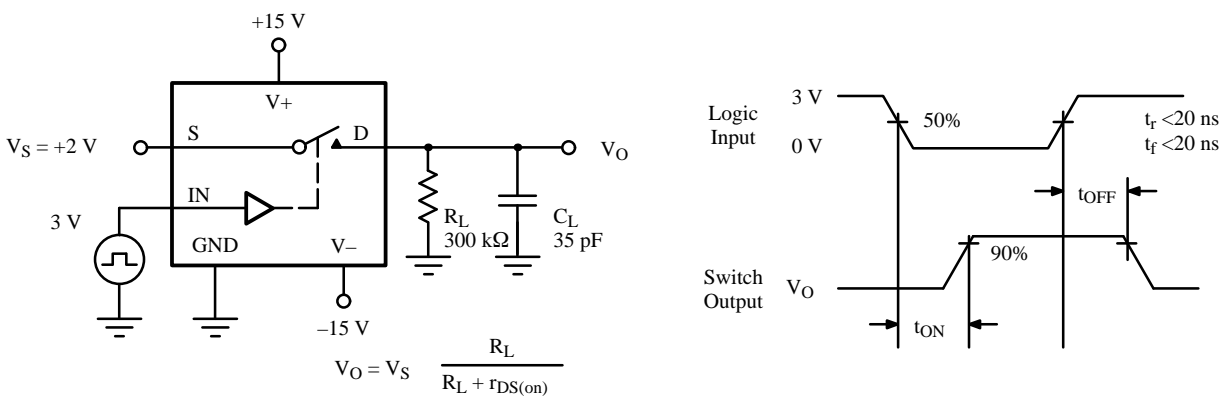


Figure 2. Switching Time

Test Circuits (Cont'd)

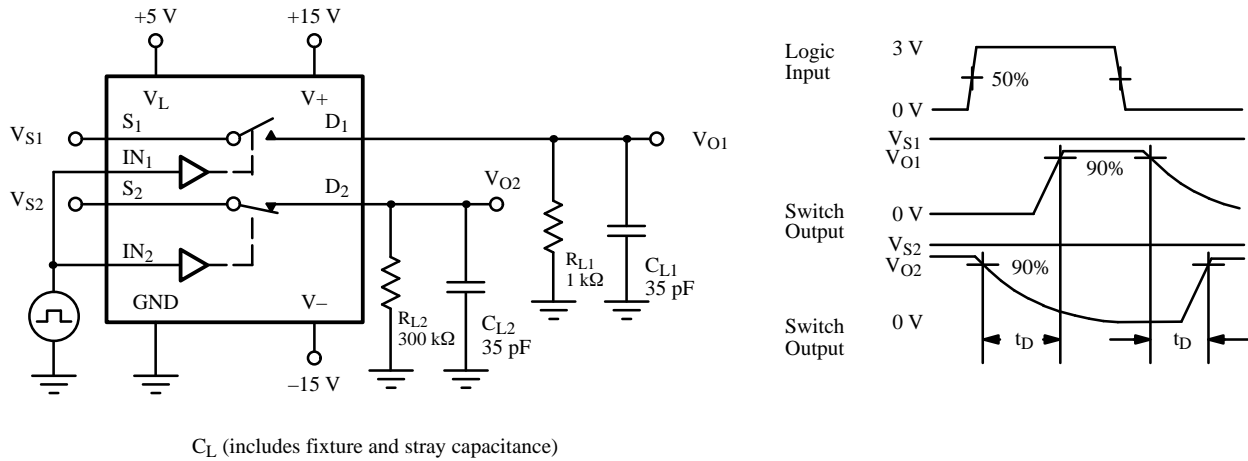


Figure 3. Break-Before-Make

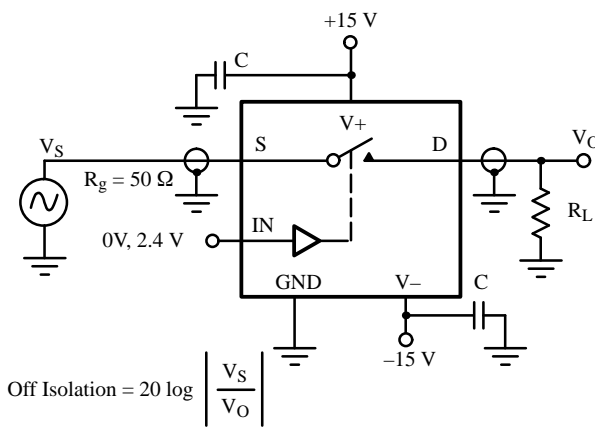


Figure 4. Off Isolation

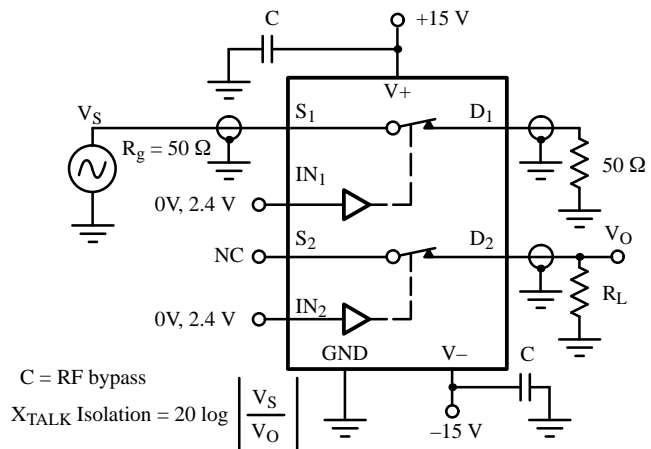
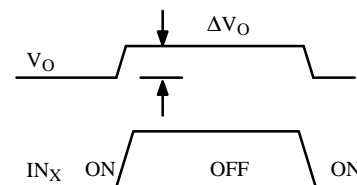
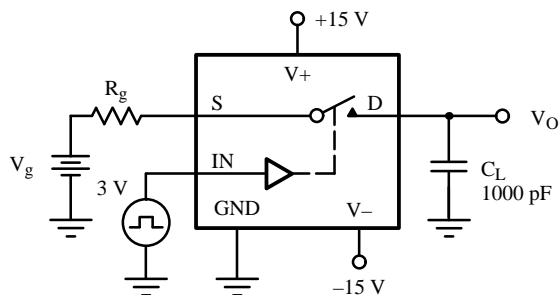


Figure 5. Channel-to-Channel Crosstalk



ΔV_O = measured voltage error due to charge injection
The charge injection in coulombs is $Q = C_L \times \Delta V_O$

Figure 6. Charge Injection

Applications

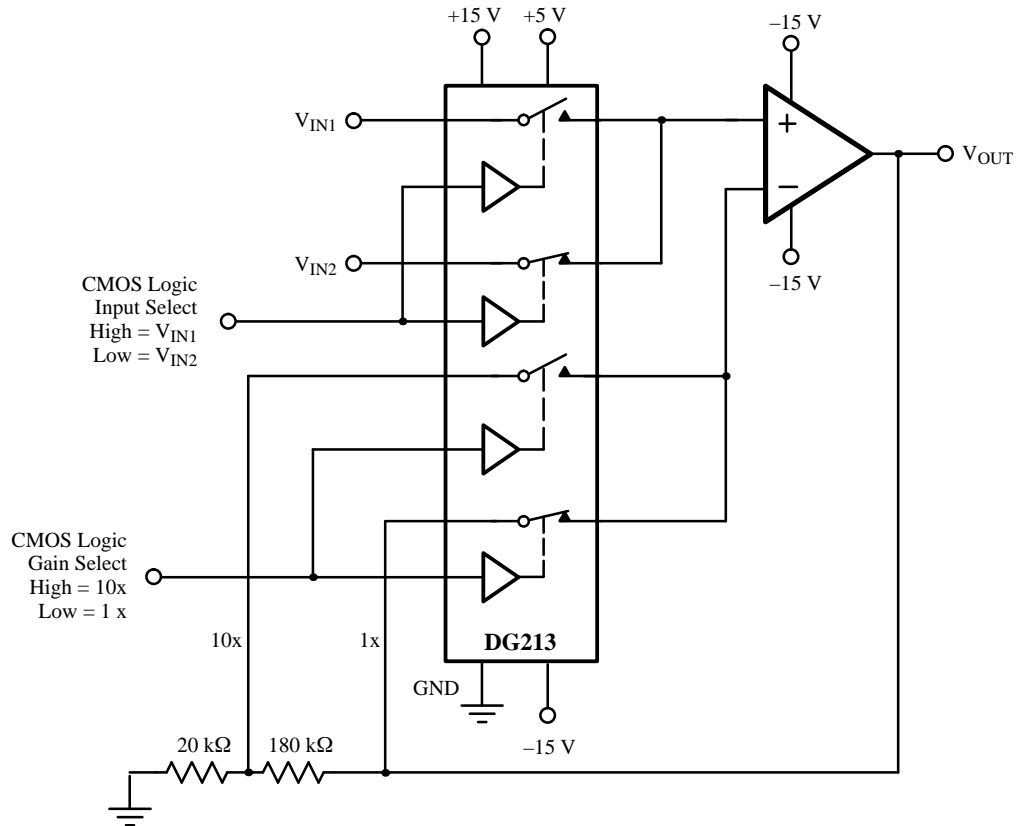


Figure 7. Low Power Non-Inverting Amplifier with Digitally Selectable Inputs and Gain

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