

DM74ALS174 • DM74ALS175 Hex/Quad D-Type Flip-Flops with Clear

General Description

These positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic. Both have an asynchronous clear input, and the quad (DM74ALS175) version features complementary outputs from each flip-flop.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or LOW level, the D input signal has no effect at the output.

Features

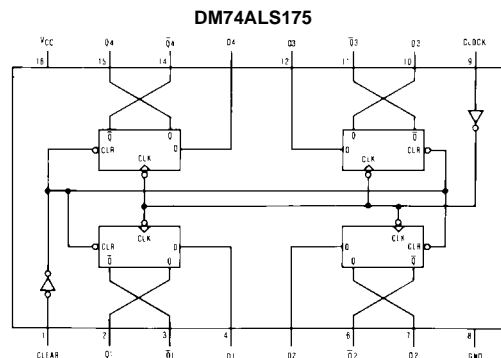
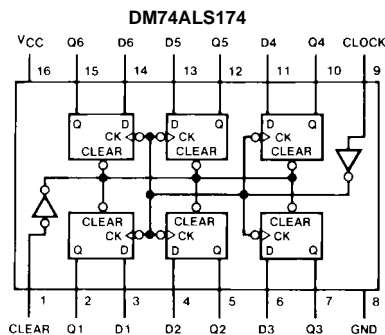
- Advanced oxide-isolated ion-implanted Schottky TTL process
- Pin and functional compatible with LS family counterpart
- Typical clock frequency maximum is 80 MHz
- Switching performance guaranteed over full temperature and V_{CC} supply range

Ordering Code:

| Ordering Code | Package Number | Package Description |
|---------------|----------------|---|
| DM74ALS174M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74ALS174SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| DM74ALS174N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |
| DM74ALS175M | M16A | 16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow |
| DM74ALS175SJ | M16D | 16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide |
| DM74ALS175N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

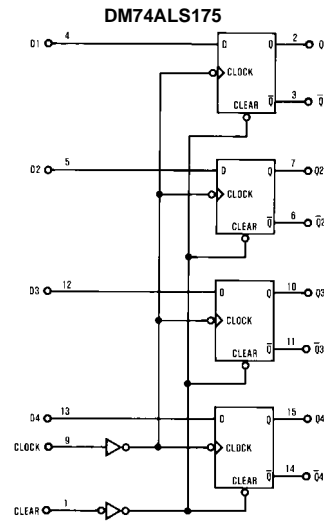
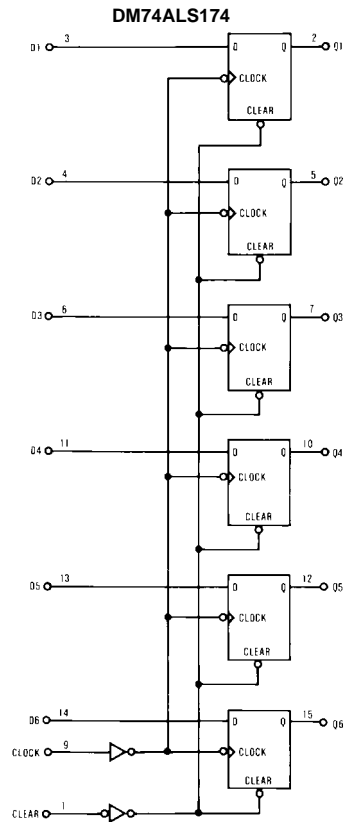


Function Table

| Inputs | | | Outputs | |
|--------|-------|---|---------|--------------------|
| Clear | Clock | D | Q | \bar{Q} (Note 1) |
| L | X | X | L | H |
| H | ↑ | H | H | L |
| H | ↑ | L | L | H |
| H | L | X | Q_0 | \bar{Q}_0 |

H = HIGH Level (steady state)
 L = LOW Level (steady state)
 X = Don't Care
 ↑ = Transition from LOW-to-HIGH Level
 Q_0 = the level of Q before the indicated steady-state input conditions were established
Note 1: applies to DM74ALS175 only

Logic Diagrams



Absolute Maximum Ratings(Note 2)

| | |
|--------------------------------------|-----------------|
| Supply Voltage | 7V |
| Input Voltage | 7V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | -65°C to +150°C |
| Typical θ_{JA} | |
| N Package | 77.9°C/W |
| M Package | 107.3°C/W |

Note 2: The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Recommended Operating Conditions

| Symbol | Parameter | Min | Nom | Max | Units |
|-------------|--------------------------------|-------------------------|---------------|------|-------|
| V_{CC} | Supply Voltage | 4.5 | 5 | 5.5 | V |
| V_{IH} | HIGH Level Input Voltage | 2 | | | V |
| V_{IL} | LOW Level Input Voltage | | | 0.8 | V |
| I_{OH} | HIGH Level Output Current | | | -0.4 | mA |
| I_{OL} | LOW Level Output Current | | | 8 | mA |
| t_W | Pulse Width | Clock HIGH or LOW | 10 | | ns |
| | | Clear LOW | 10 | | |
| t_{SETUP} | Setup Time (Note 3) | Data Input | 10 \uparrow | | ns |
| | | Clear Inactive State | 6 \uparrow | | |
| t_{HOLD} | Data Hold Time (Note 3) | 0 \uparrow | | | ns |
| f_{CLOCK} | Clock Frequency | 0 | | 50 | MHz |
| T_A | Free Air Operating Temperature | 0 | | 70 | °C |

Note 3: The symbol \uparrow indicates that the rising edge of the clock is used as reference.

Electrical Characteristics

over recommended operating free air temperature range. All typical values are measured at $V_{CC} = 5V$, $T_A = 25^\circ C$.

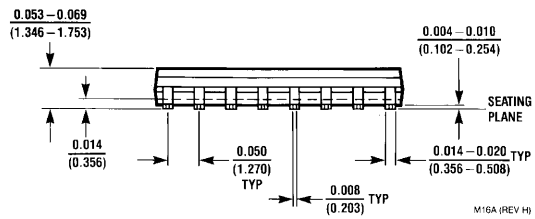
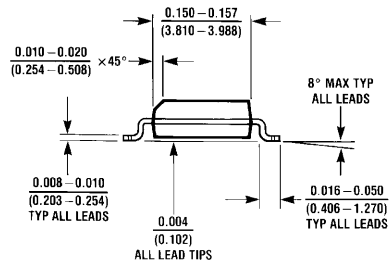
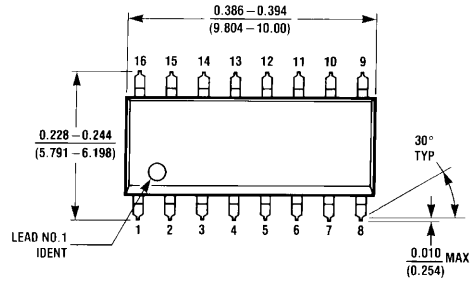
| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|----------|------------------------------------|---|--------------|----------------|------|---------|
| V_{IK} | Input Clamp Voltage | $V_{CC} = 4.5V$, $I_{IN} = -18\text{ mA}$ | | | -1.5 | V |
| V_{OH} | HIGH Level Output Voltage | $I_{OH} = -400\ \mu A$ $V_{CC} = 4.5V\text{ to }5.5V$ | $V_{CC} - 2$ | $V_{CC} - 1.6$ | | V |
| V_{OL} | LOW Level Output Voltage | $V_{CC} = 4.5V$, $I_{OL} = 8\text{ mA}$ | | 0.35 | 0.5 | V |
| I_I | Input Current at Max Input Voltage | $V_{CC} = 5.5V$, $V_{IN} = 7V$ | | | 0.1 | mA |
| I_{IH} | HIGH Level Input Current | $V_{CC} = 5.5V$, $V_{IH} = 2.7V$ | | | 20 | μA |
| I_{IL} | LOW Level Input Current | $V_{CC} = 5.5V$, $V_{IN} = 0.4V$ | | | -0.1 | mA |
| I_O | Output Drive Current | $V_{CC} = 5.5V$, $V_O = 2.25V$ | -30 | | -112 | mA |
| I_{CC} | Supply Current | $V_{CC} = 5.5V$ Clock = 4.5V Clear = GND D Input = GND | DM74ALS174 | 11 | 19 | mA |
| | | | DM74ALS175 | 8 | 14 | |

Switching Characteristics

over recommended operating free air temperature range

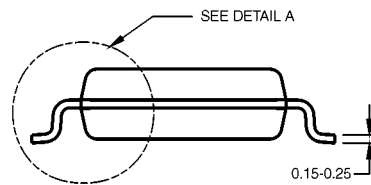
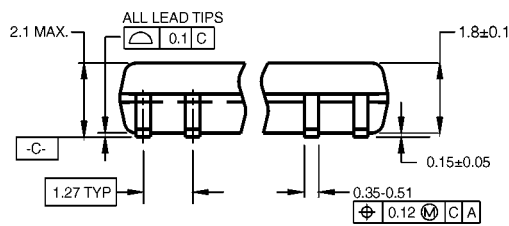
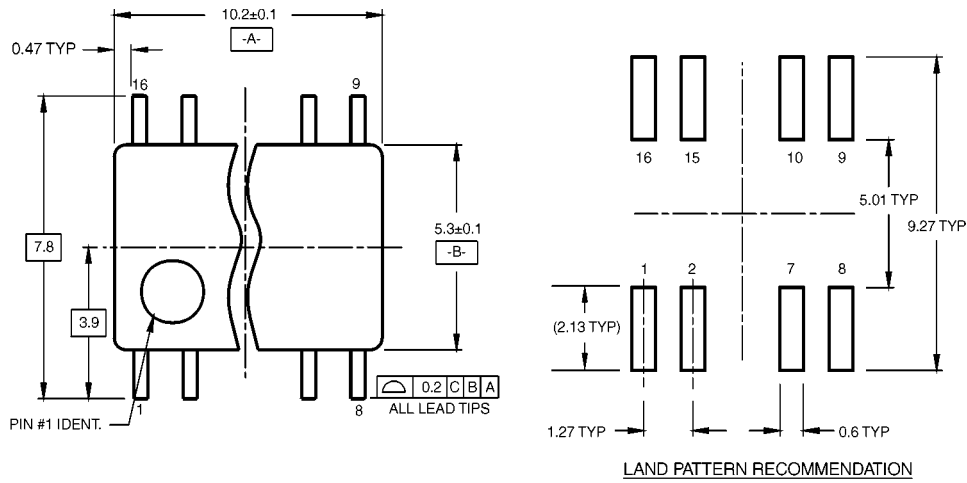
| Symbol | Parameter | Conditions | Min | Max | Units |
|-----------|---|---|--|-----|-------|
| f_{MAX} | Maximum Clock Frequency | $R_L = 500\ \Omega$ $C_L = 50\text{ pF}$ $V_{CC} = 4.5V\text{ to }5.5V$ | 50 | | MHz |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output From Clear (175 Only) | | 5 | 18 | ns |
| | t_{PHL} | | Propagation Delay Time HIGH-to-LOW Level Output From Clear | 8 | 23 |
| t_{PLH} | Propagation Delay Time LOW-to-HIGH Level Output From Clock | | 3 | 15 | ns |
| t_{PHL} | Propagation Delay Time HIGH-to-LOW Level Output From Clock | | 5 | 17 | ns |

Physical Dimensions inches (millimeters) unless otherwise noted



**16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
Package Number M16A**

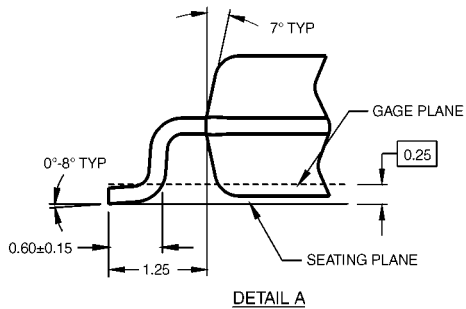
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

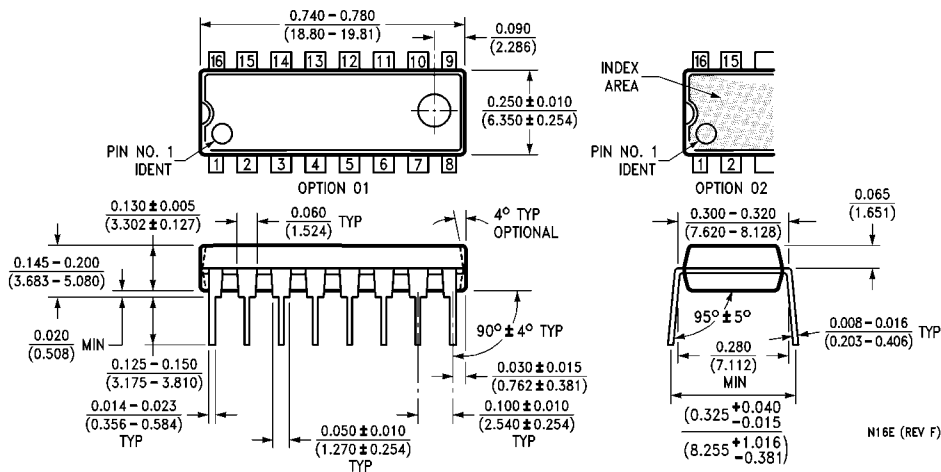
- NOTES:
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
 B. DIMENSIONS ARE IN MILLIMETERS.
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M16DRevB1



16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N16E

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