

DS90CR581 LVDS Transmitter 24-Bit Color Flat Panel Display (FPD) Link

General Description

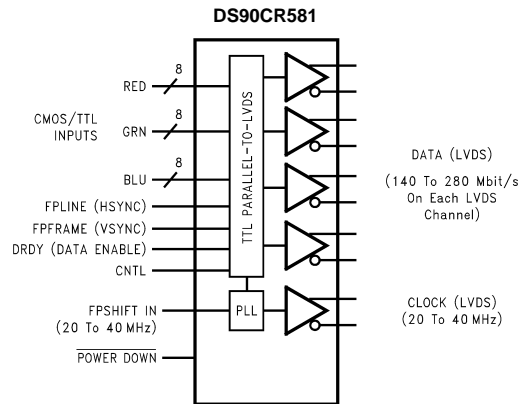
The DS90CR581 transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 40 MHz, 24 bits of RGB data and 4 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY, CNTL) are transmitted at a rate of 280 Mbps per LVDS data channel. Using a 40 MHz clock, the data throughput is 140 Megabytes per second. This transmitter is intended to interface to any of the FPD Link receivers.

The chipset is an ideal means to solve EMI and cable size problems associated with wide, high speed TTL interfaces.

Features

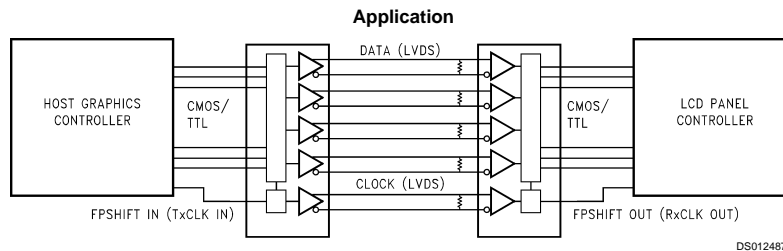
- Up to 140 Megabyte/sec Bandwidth
- Narrow bus reduces cable size and cost
- 290 mV swing LVDS devices for low EMI
- Low power CMOS design
- Power down mode
- PLL requires no external components
- Low profile 56-lead TSSOP package
- Rising edge data strobe
- Compatible with TIA/EIA-644 LVDS standard

Block Diagrams



DS012487-29

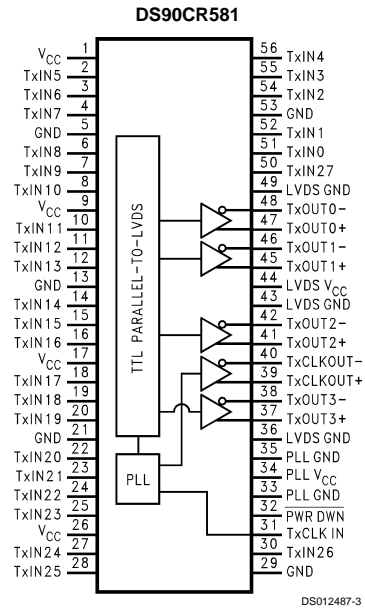
Order Number DS90CR581MTD
See NS Package Number MTD56



DS012487-2

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Connection Diagram



DS012487-3

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

| | |
|-------------------------------------------|-----------------------------|
| Supply Voltage (V_{CC}) | -0.3 to +6V |
| CMOS/TTL Input Voltage | -0.3 to ($V_{CC} + 0.3V$) |
| LVDS Driver Output Voltage | -0.3 to ($V_{CC} + 0.3V$) |
| LVDS Output Short Circuit Duration | continuous |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (Soldering, 4 sec.) | +260°C |
| Maximum Package Power Dissipation @ +25°C | |
| MTD56 (TSSOP) Package: | |

| | |
|-------------------|------------------------|
| DS90CR581 | 1.63W |
| Package Derating: | |
| DS90CR581 | 12.5 mW/°C above +25°C |

This device does not meet 2000V ESD rating. (Note 4)

Recommended Operating Conditions

| | Min | Nom | Max | Units |
|-----------------------------------|-----|-----|-----|-------------------|
| Supply Voltage (V_{CC}) | 4.5 | 5.0 | 5.5 | V |
| Operating Free | | | | |
| Air Temperature (T_A) | -10 | +25 | +70 | °C |
| Receiver Input Range | 0 | | 2.4 | V |
| Supply Noise Voltage (V_{CC}) | | | 100 | mV _{P-P} |

Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Conditions | Min | Typ | Max | Units | |
|--------------------------------------|--------------------------------------------------------|------------------------------------------------------------------------|----------------|-------|----------|-------|----|
| CMOS/TTL DC SPECIFICATIONS | | | | | | | |
| V_{IH} | High Level Input Voltage | | 2.0 | | V_{CC} | V | |
| V_{IL} | Low Level Input Voltage | | GND | | 0.8 | V | |
| V_{CL} | Input Clamp Voltage | $I_{CL} = -18$ mA | | -0.79 | -1.5 | V | |
| I_{IN} | Input Current | $V_{IN} = V_{CC}, GND, 2.5V$ or 0.4V | | ±5.1 | ±10 | µA | |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0V$ | | | -120 | mA | |
| LVDS DRIVER DC SPECIFICATIONS | | | | | | | |
| V_{OD} | Differential Output Voltage | $R_L = 100\Omega$ | 250 | 290 | 450 | mV | |
| ΔV_{OD} | Change in V_{OD} between Complimentary Output States | | | | 35 | mV | |
| V_{OS} | Offset Voltage (Note 5) | | 1.1 | 1.25 | 1.375 | V | |
| ΔV_{OS} | Change in V_{OS} between Complimentary Output States | | | | 35 | mV | |
| V_{OH} | High Level Output Voltage | | | 1.3 | 1.6 | V | |
| V_{OL} | Low Level Output Voltage | | 0.9 | 1.01 | | V | |
| I_{OS} | Output Short Circuit Current | $V_{OUT} = 0V, R_L = 100\Omega$ | | -2.9 | -5 | mA | |
| I_{OZ} | Output TRI-STATE® Current | Power Down = 0V, $V_{OUT} = 0V$ or V_{CC} | | ±1 | ±10 | µA | |
| TRANSMITTER SUPPLY CURRENT | | | | | | | |
| I_{CCTW} | Transmitter Supply Current, Worst Case | $R_L = 100\Omega, C_L = 5$ pF, Worst Case Pattern (Figure 1, Figure 2) | $f = 32.5$ MHz | | 34 | 51 | mA |
| | | | $f = 37.5$ MHz | | 36 | 53 | mA |
| I_{CCTG} | Transmitter Supply Current, 16 Grayscale | $R_L = 100\Omega, C_L = 5$ pF, Grayscale Pattern (Figure 2, Figure 3) | $f = 32.5$ MHz | | 27 | 47 | mA |
| | | | $f = 37.5$ MHz | | 28 | 48 | mA |
| I_{CCTZ} | Transmitter Supply Current, Power Down | Power Down = Low | | 1 | 25 | µA | |

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Note 2: Typical values are given for $V_{CC} = 5.0V$ and $T_A = +25^\circ C$.

Note 3: Current into device pins is defined as positive. Current out of device pins is defined as negative. Voltages are referenced to ground unless otherwise specified (except V_{OD} and ΔV_{OD}).

Note 4: ESD Rating: HBM (1.5 kΩ, 100 pF)

PLL $V_{CC} \geq 1000V$

All other pins $\geq 2000V$

EIAJ (0Ω, 200 pF) $\geq 150V$

Note 5: V_{OS} previously referred as V_{CM}

Transmitter Switching Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified

| Symbol | Parameter | Min | Typ | Max | Units | |
|--------|-----------------------------------------------------------------------|------------|------|-------|-------|----|
| LLHT | LVDS Low-to-High Transition Time (Figure 3) | | 0.75 | 1.5 | ns | |
| LHLT | LVDS High-to-Low Transition Time (Figure 3) | | 0.75 | 1.5 | ns | |
| TCIT | TxCLK IN Transition Time (Figure 4) | | | 8 | ns | |
| TCCS | TxOUT Channel-to-Channel Skew (Note 6) (Figure 5) | | | 350 | ps | |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 11) | f = 20 MHz | -200 | 150 | 350 | ps |
| TPPos1 | Transmitter Output Pulse Position for Bit 1 | | 6.3 | 7.2 | 7.5 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 | | 12.8 | 13.6 | 14.6 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 | | 20 | 20.8 | 21.5 | ns |
| TPPos4 | Transmitter Output Pulse Position for Bit 4 | | 27.2 | 28 | 28.5 | ns |
| TPPos5 | Transmitter Output Pulse Position for Bit 5 | | 34.5 | 35.2 | 35.6 | ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6 | | 42.2 | 42.6 | 42.9 | ns |
| TPPos0 | Transmitter Output Pulse Position for Bit 0 (Figure 11) | f = 40 MHz | -100 | 100 | 300 | ps |
| TPPos1 | Transmitter Output Pulse Position for Bit 1 | | 2.9 | 3.3 | 3.9 | ns |
| TPPos2 | Transmitter Output Pulse Position for Bit 2 | | 6.1 | 6.6 | 7.1 | ns |
| TPPos3 | Transmitter Output Pulse Position for Bit 3 | | 9.7 | 10.2 | 10.7 | ns |
| TPPos4 | Transmitter Output Pulse Position for Bit 4 | | 13 | 13.5 | 14.1 | ns |
| TPPos5 | Transmitter Output Pulse Position for Bit 5 | | 17 | 17.4 | 17.8 | ns |
| TPPos6 | Transmitter Output Pulse Position for Bit 6 | | 20.3 | 20.8 | 21.4 | ns |
| TCIP | TxCLK IN Period (Figure 6) | 25 | T | 50 | ns | |
| TCIH | TxCLK IN High Time (Figure 6) | 0.35T | 0.5T | 0.65T | ns | |
| TCIL | TxCLK IN Low Time (Figure 6) | 0.35T | 0.5T | 0.65T | ns | |
| TSTC | TxIN Setup to TxCLK IN (Figure 6) | f = 20 MHz | 14 | | ns | |
| | | f = 40 MHz | 8 | | ns | |
| THTC | TxIN Hold to TxCLK IN (Figure 6) | 2.5 | 2 | | ns | |
| TCCD | TxCLK IN to TxCLK OUT Delay @ 25°C, V _{CC} = 5.0V (Figure 7) | 5 | | 9.7 | ns | |
| TPLLS | Transmitter Phase Lock Loop Set (Figure 8) | | | 10 | ms | |
| TPDD | Transmitter Powerdown Delay (Figure 10) | | | 100 | ns | |

Note 6: This limit based on bench characterization.

AC Timing Diagrams

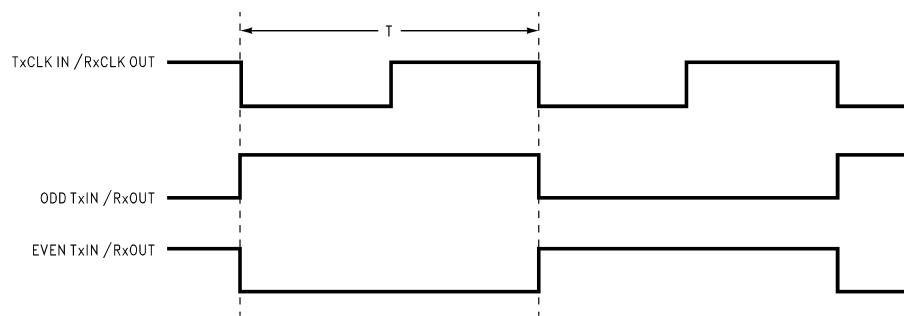
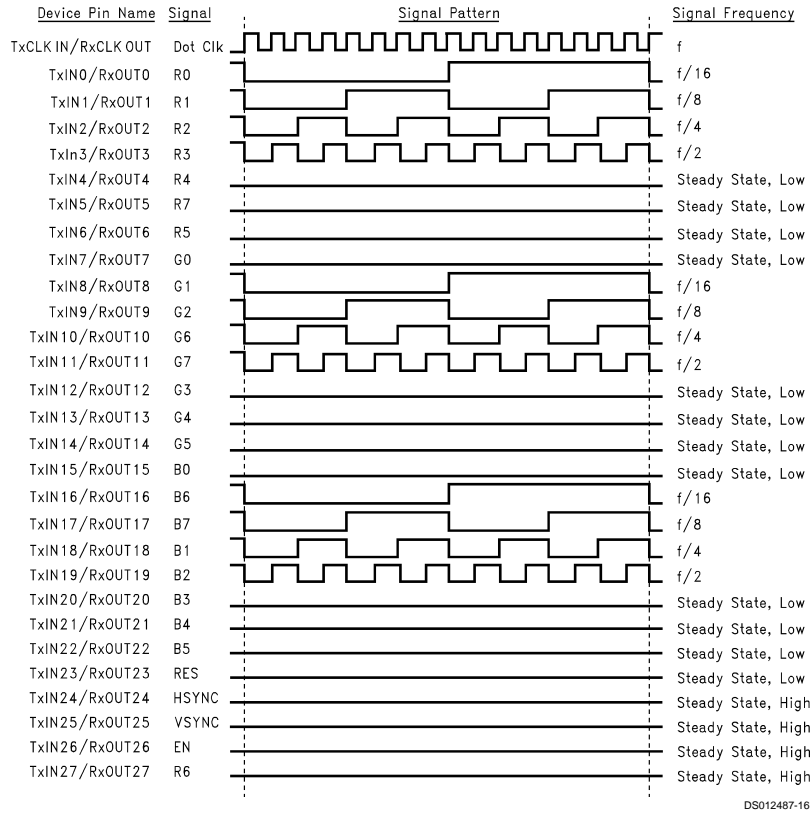


FIGURE 1. "Worst Case" Test Pattern

DS012487-15

AC Timing Diagrams (Continued)



Note 7: The worst case test pattern produces a maximum toggling of digital circuits, LVDS I/O and CMOS/TTL I/O.

Note 8: The 16 grayscale test pattern tests device power consumption for a "typical" LCD display pattern. The test pattern approximates signal switching needed to produce groups of 16 vertical stripes across the display.

Note 9: Figure 1 and Figure 2 show a rising edge data strobe (TxCLK IN/RxCLK OUT).

Note 10: Recommended pin to signal mapping. Customer may choose to define differently.

FIGURE 2. "16 Grayscale" Test Pattern (Notes 7, 8) (Note 9) (Note 10)

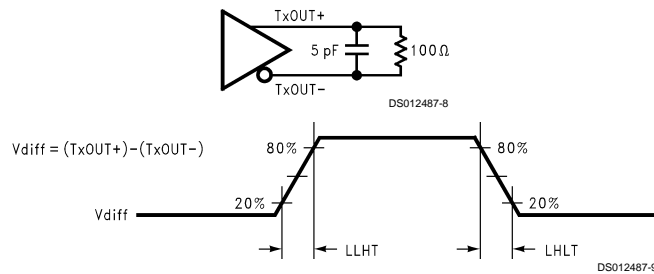


FIGURE 3. DS90CR581 (Transmitter) LVDS Output Load and Transition Timing

AC Timing Diagrams (Continued)

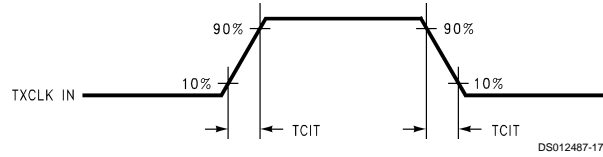
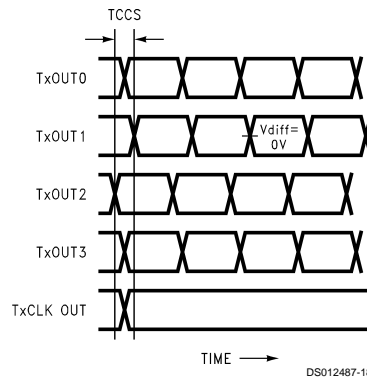


FIGURE 4. DS90CR581 (Transmitter) Input Clock Transition Time



Note 11: Measurements at $V_{diff} = 0V$

Note 12: TCCS measured between earliest and latest initial LVDS edges.

Note 13: TxCLK OUT Differential High→Low Edge for DS90CF581

TxCLK OUT Differential Low→High Edge for DS90CR581

FIGURE 5. DS90CR581 (Transmitter) Channel-to-Channel Skew

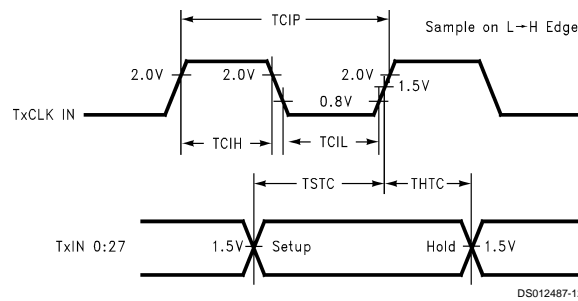


FIGURE 6. DS90CR581 (Transmitter) Setup/Hold and High/Low Times

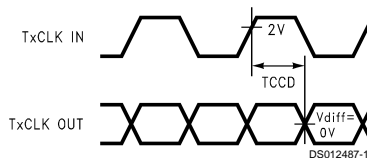


FIGURE 7. DS90CR581 (Transmitter) Clock In to Clock Out Delay

AC Timing Diagrams (Continued)

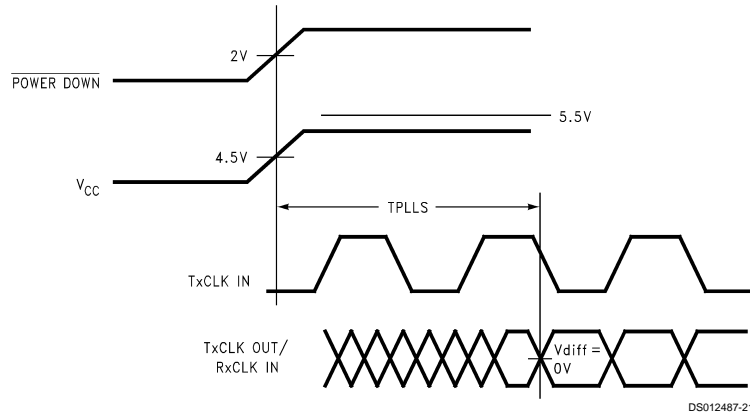


FIGURE 8. DS90CR581 (Transmitter) Phase Lock Loop Set Time

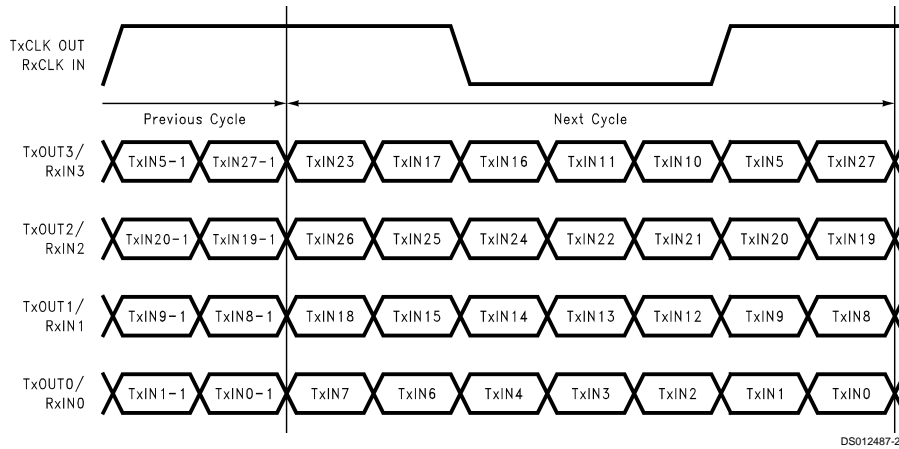


FIGURE 9. 28 Parallel TTL Data Inputs Mapped to LVDS Outputs (DS90CR581)

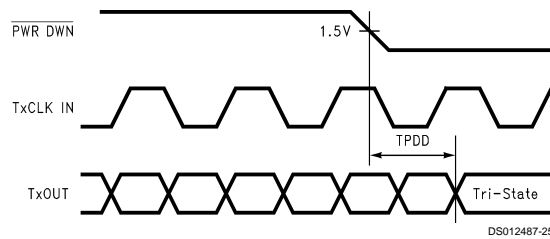
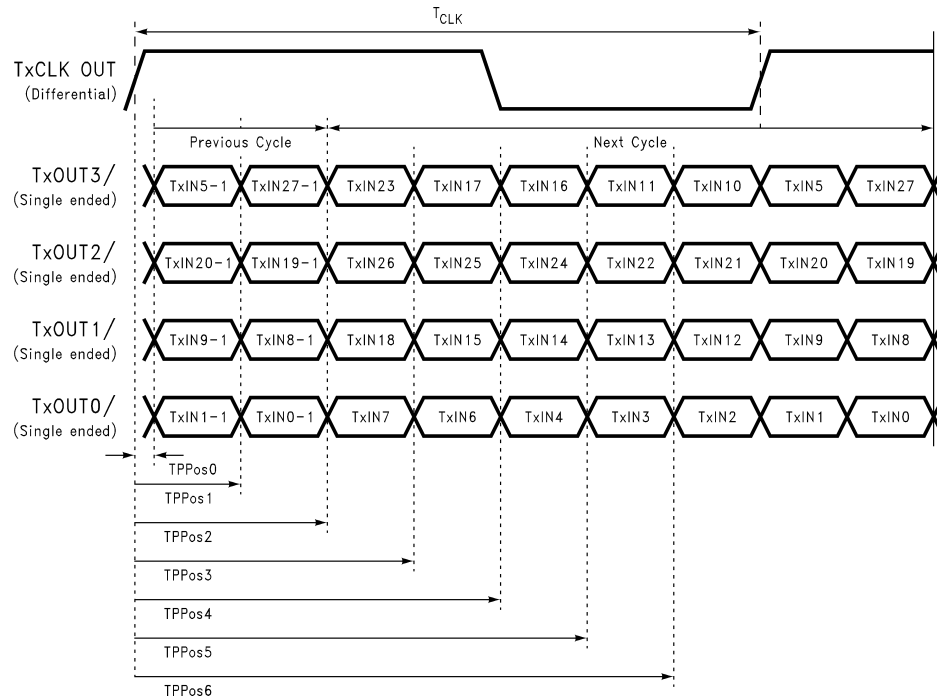


FIGURE 10. Transmitter Powerdown Delay

AC Timing Diagrams (Continued)

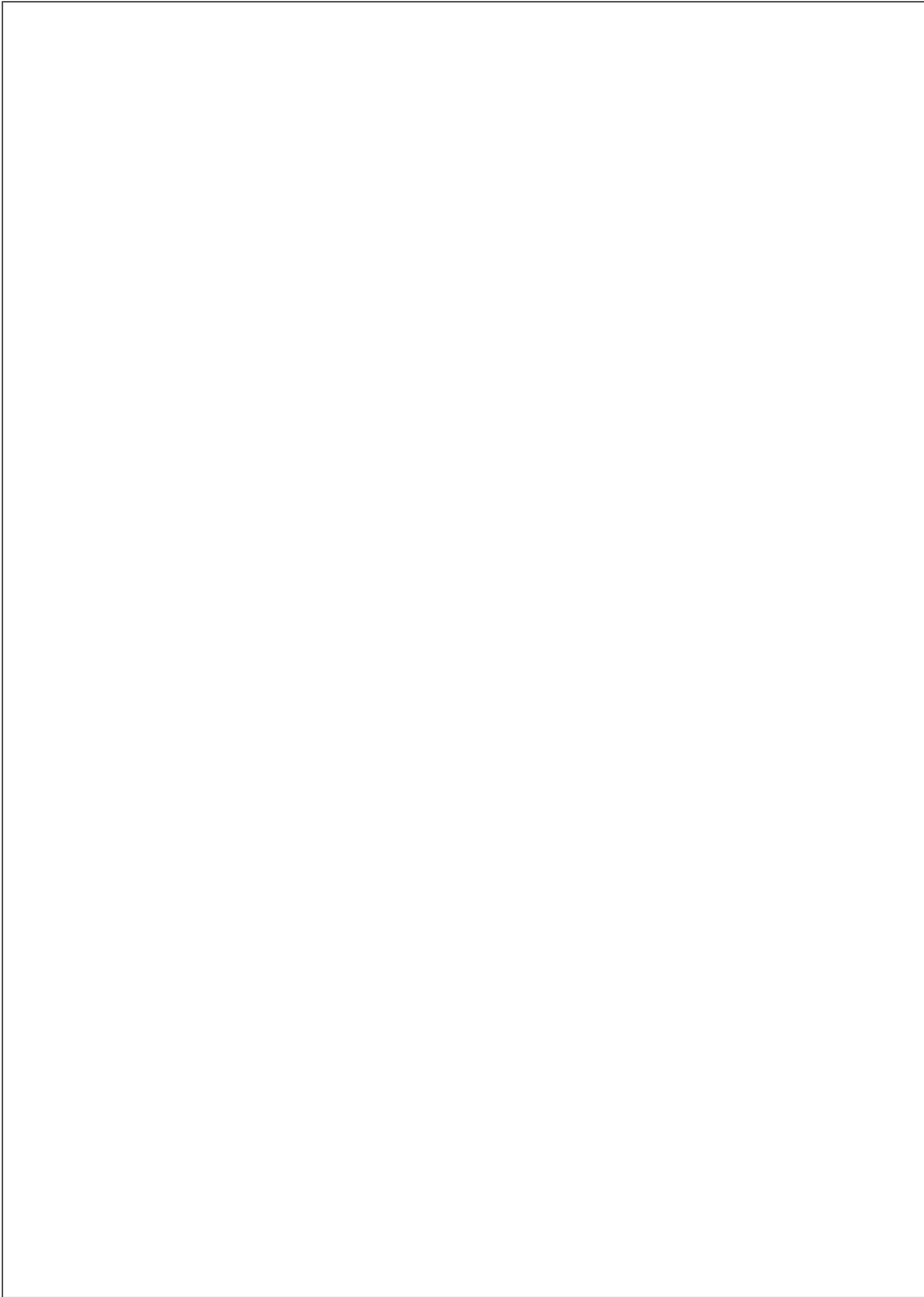


DS012487-27

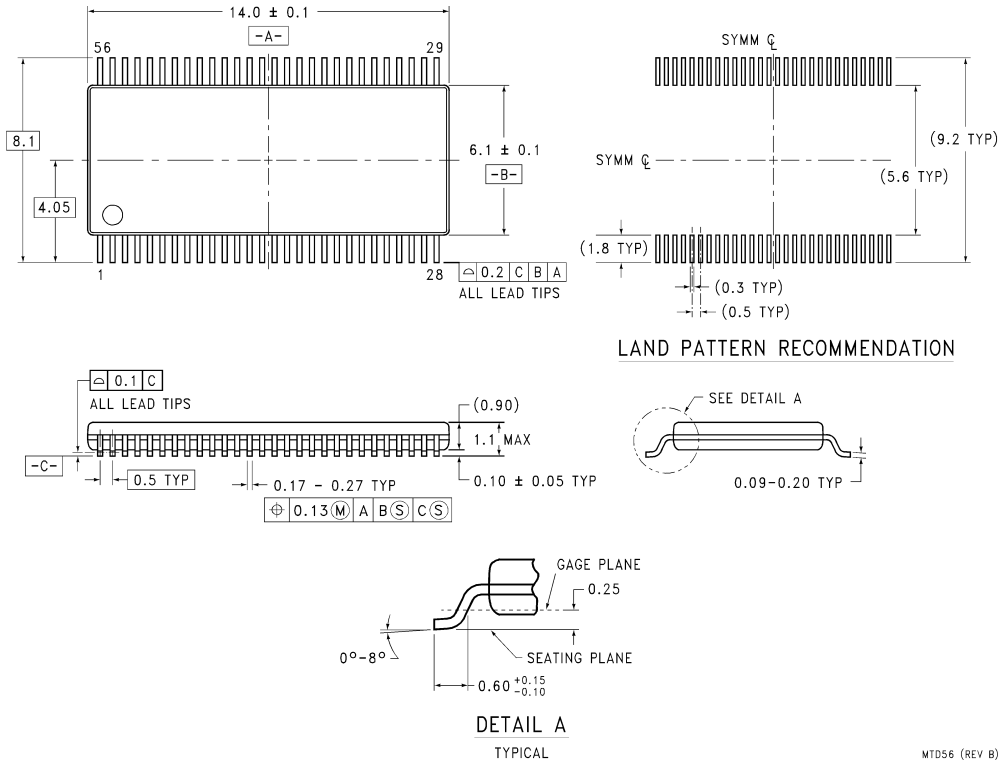
FIGURE 11. Transmitter LVDS Output Pulse Position Measurement

DS90CR581 Pin Description—FPD Link Transmitter

| Pin Name | I/O | No. | Description |
|----------------------|-----|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------|
| TxIN | I | 28 | TTL Level input. This includes: 8 Red, 8 Green, 8 Blue, and 4 control lines (FPLINE, FPFRAME, DRDY, CNTL). (Also referred to as HSYNC, VSYNC and DATA ENABLE) |
| TxOUT+ | O | 4 | Positive LVDS differential data output |
| TxOUT- | O | 4 | Negative LVDS differential data output |
| FPSHIFT IN | I | 1 | TTL level clock input. The rising edge acts as data strobe. |
| TxCLK OUT+ | O | 1 | Positive LVDS differential clock output |
| TxCLK OUT- | O | 1 | Negative LVDS differential clock output |
| PWR DOWN | I | 1 | TTL level input. Assertion (low input) TRI-STATES the outputs, ensuring low current at power down. |
| V _{CC} | I | 4 | Power supply pins for TTL inputs |
| GND | I | 5 | Ground pins for TTL inputs |
| PLL V _{CC} | I | 1 | Power supply pin for PLL |
| PLL GND | I | 2 | Ground pins for PLL |
| LVDS V _{CC} | I | 1 | Power supply pin for LVDS outputs |
| LVDS GND | I | 3 | Ground pins for LVDS outputs |



Physical Dimensions inches (millimeters) unless otherwise noted



**56-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD56**

MTD56 (REV B)

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