

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40194B

MSI

4-bit bidirectional universal shift register

Product specification
File under Integrated Circuits, IC04

January 1995

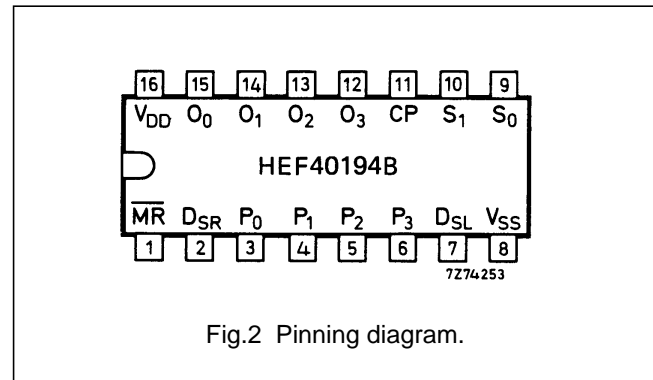
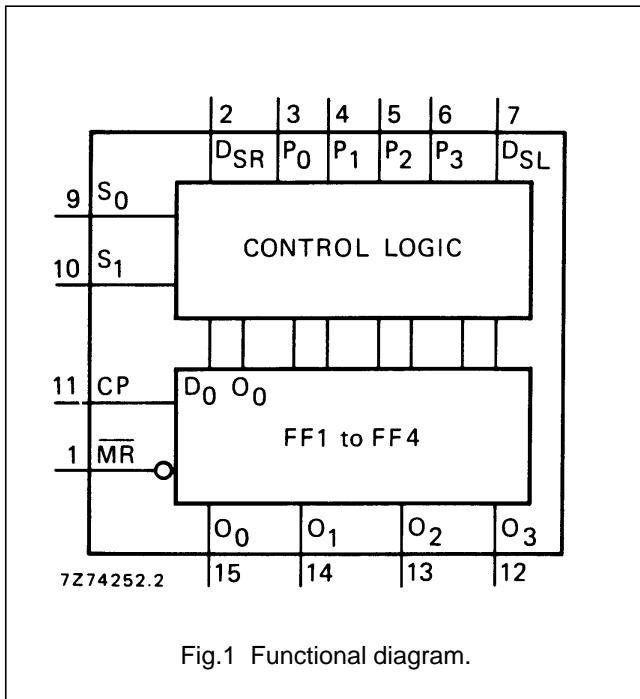
4-bit bidirectional universal shift register

HEF40194B MSI

DESCRIPTION

The HEF40194B is a 4-bit bidirectional shift register with two mode control inputs (S_0 and S_1), a clock input (CP), a serial data shift left input (D_{SL}), a serial data shift right input (D_{SR}), four parallel data inputs (P_0 to P_3), an overriding asynchronous master reset input (\overline{MR}), and four buffered parallel outputs (O_0 to O_3). When LOW, \overline{MR} resets all stages and forces O_0 to O_3 LOW, overriding all other input conditions. When \overline{MR} is HIGH, the operation mode is controlled by S_0 and S_1 as shown in the function table.

Serial and parallel operation are edge-triggered on the LOW to HIGH transition of CP. The inputs at which the data are to be entered and S_0 , S_1 must be stable for a set-up time before the LOW to HIGH transition of CP.



- HEF40194BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF40194BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF40194BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

PINNING

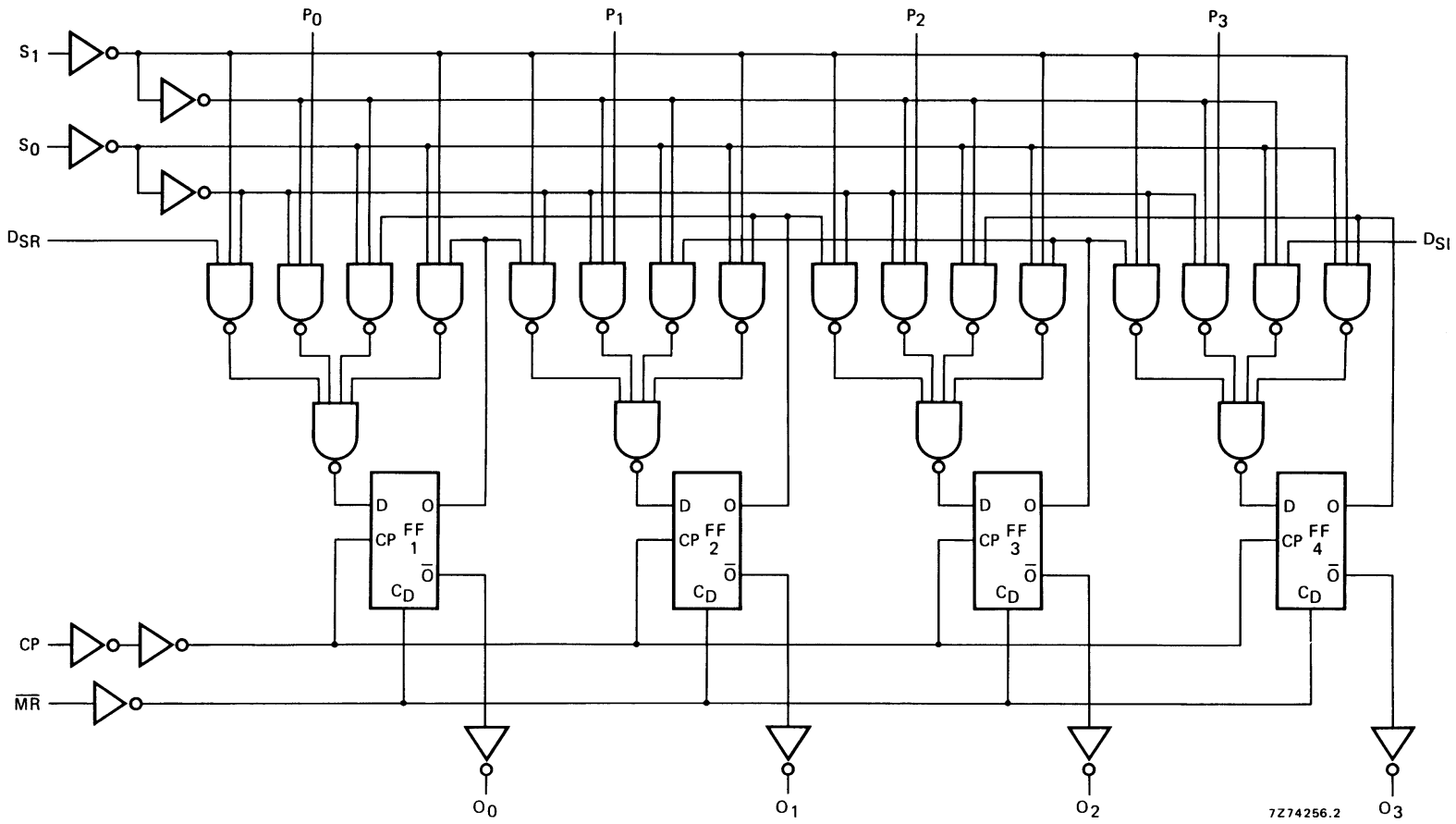
- S_0 , S_1 mode control inputs
- P_0 to P_3 parallel data inputs
- D_{SR} serial data shift right input
- D_{SL} serial data shift left input
- CP clock input (LOW to HIGH edge-triggered)
- \overline{MR} master reset input (active LOW)
- O_0 to O_3 buffered parallel outputs

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

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Fig.3 Logic diagram.

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FUNCTION TABLE

OPERATING MODE	INPUTS ($\overline{MR} = \text{HIGH}$)					OUTPUTS AT T_{n+1}			
	S ₁	S ₀	D _{SR}	D _{SL}	P ₀ TO P ₃	O ₀	O ₁	O ₂	O ₃
hold	L	L	X	X	X	O ₀	O ₁	O ₂	O ₃
shift left	H	L	X	L	X	O ₁	O ₂	O ₃	L
	H	L	X	H	X	O ₁	O ₂	O ₃	H
shift right	L	H	L	X	X	L	O ₀	O ₁	O ₂
	L	H	H	X	X	H	O ₀	O ₁	O ₂
parallel load	H	H	X	X	L	L	L	L	L
	H	H	X	X	H	H	H	H	H

Notes

1. H = HIGH state (the more positive voltage)
2. L = LOW state (the less positive voltage)
3. X = state is immaterial
4. t_{n+1} = state after next LOW to HIGH transition of CP

AC CHARACTERISTICS

$V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; input transition times $\leq 20 \text{ ns}$

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5 10 15	1 500 f _i + Σ (f _o C _L) × V _{DD} ² 6 900 f _i + Σ (f _o C _L) × V _{DD} ² 18 900 f _i + Σ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load cap. (pF) Σ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)

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MSI**AC CHARACTERISTICS** $V_{SS} = 0\text{ V}$; $T_{amb} = 25\text{ }^{\circ}\text{C}$; $C_L = 50\text{ pF}$; input transition times $\leq 20\text{ ns}$

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA		
Propagation delays CP \rightarrow O _n HIGH to LOW	5	t_{PHL}		100	205	ns	73 ns + (0,55 ns/pF) C_L	
	10		40	85	ns	29 ns + (0,23 ns/pF) C_L		
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L		
	LOW to HIGH	5	t_{PLH}		80	165	ns	53 ns + (0,55 ns/pF) C_L
		10		35	70	ns	24 ns + (0,23 ns/pF) C_L	
		15		25	55	ns	17 ns + (0,16 ns/pF) C_L	
$\overline{\text{MR}} \rightarrow \text{O}_n$ HIGH to LOW	5	t_{PHL}		85	175	ns	58 ns + (0,55 ns/pF) C_L	
	10		40	80	ns	29 ns + (0,23 ns/pF) C_L		
	15		30	60	ns	22 ns + (0,16 ns/pF) C_L		
Output transition times HIGH to LOW	5	t_{THL}		60	120	ns	10 ns + (1,0 ns/pF) C_L	
	10		30	60	ns	9 ns + (0,42 ns/pF) C_L		
	15		20	40	ns	6 ns + (0,28 ns/pF) C_L		
	LOW to HIGH	5	t_{TLH}		60	120	ns	10 ns + (1,0 ns/pF) C_L
		10		30	60	ns	9 ns + (0,42 ns/pF) C_L	
		15		20	40	ns	6 ns + (0,28 ns/pF) C_L	

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	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Set-up times P _n , D _{SR} , D _{SL} → CP	5	t _{su}	80	40	ns	see also waveforms Figs 4 and 5
	10		30	15	ns	
	15		20	10	ns	
S _n → CP	5	t _{su}	140	70	ns	
	10		60	30	ns	
	15		40	20	ns	
Hold times P _n , D _{SR} , D _{SL} → CP	5	t _{hold}	10	-30	ns	
	10		5	-10	ns	
	15		5	-5	ns	
S _n → CP	5	t _{hold}	25	-45	ns	
	10		15	-15	ns	
	15		10	-10	ns	
Minimum clock pulse width; LOW	5	t _{WCPL}	50	25	ns	
	10		20	10	ns	
	15		20	10	ns	
Minimum $\overline{\text{MR}}$ pulse width; LOW	5	t _{WMRL}	80	40	ns	
	10		40	20	ns	
	15		30	15	ns	
Recovery time for $\overline{\text{MR}}$	5	t _{RMR}	30	10	ns	
	10		15	5	ns	
	15		15	5	ns	
Maximum clock pulse frequency	5	f _{max}	6	12	MHz	
	10		15	30	MHz	
	15		20	40	MHz	

4-bit bidirectional universal shift register

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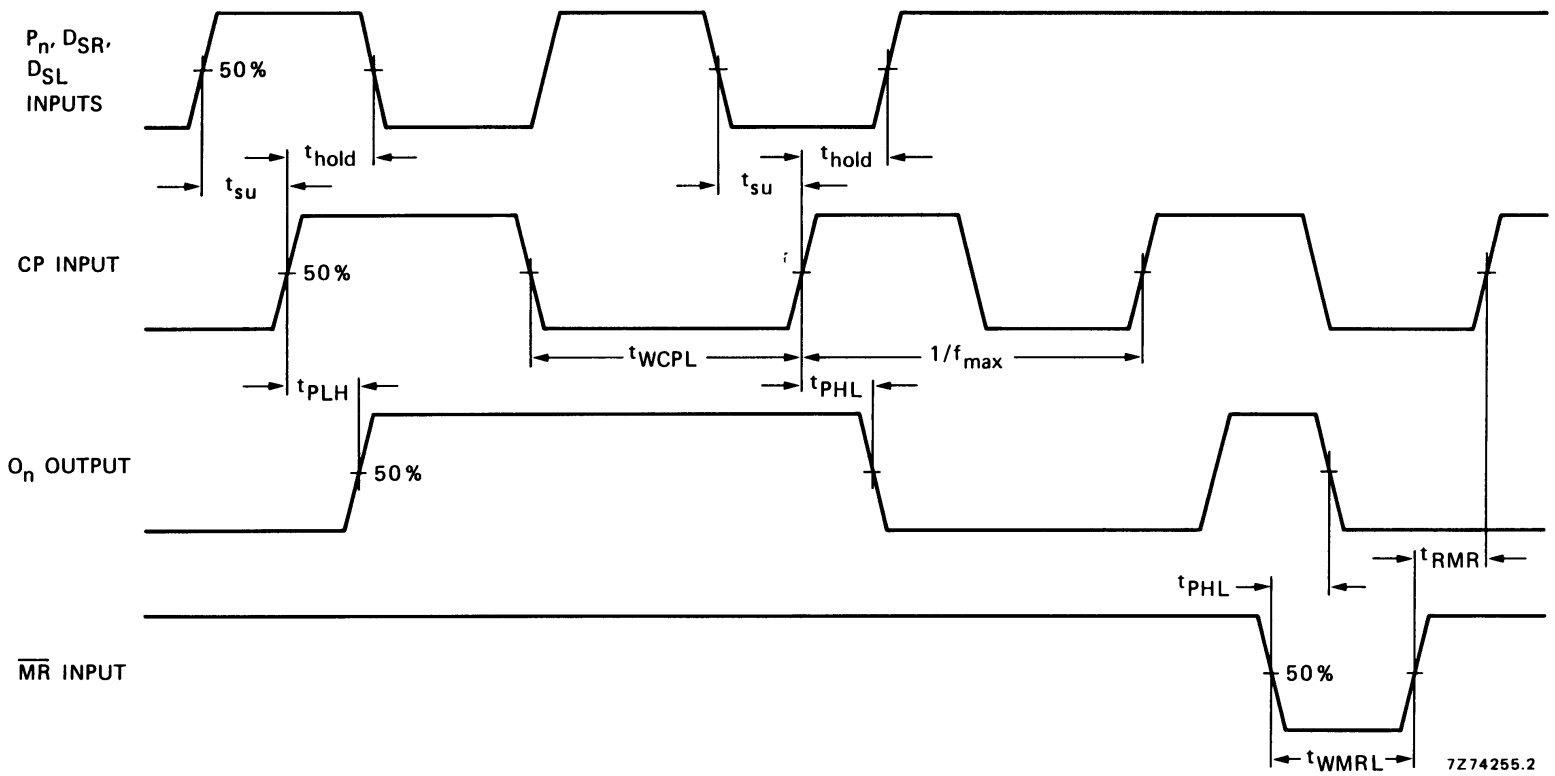


Fig.4 Waveforms showing set-up times, hold times for D_{SR} , D_{SL} and P_n inputs; minimum \overline{MR} pulse width, \overline{MR} to output delays and \overline{MR} to CP recovery time; minimum CP pulse width and CP to output delays. Set-up and hold times are shown as positive values but may be specified as negative values.

7274255.2

4-bit bidirectional universal shift register

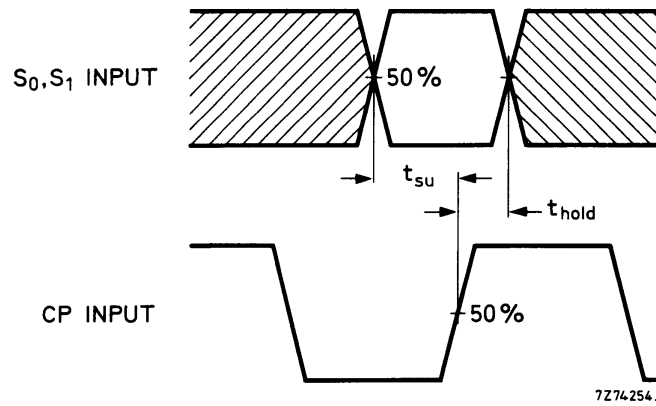
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Fig.5 Waveforms showing set-up times and hold times for S₀ and S₁ inputs. Set-up and hold times are shown as positive values but may be specified as negative values.

APPLICATION INFORMATION

Some examples of applications for the HEF40194B are:

- Arithmetic unit register
- Serial/parallel converter.



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