

DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4021B

MSI

8-bit static shift register

Product specification
File under Integrated Circuits, IC04

January 1995

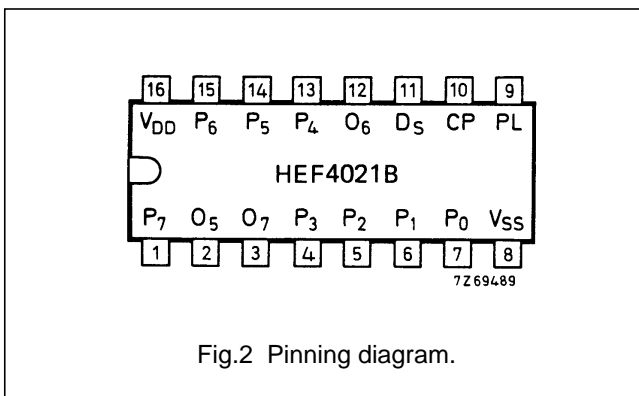
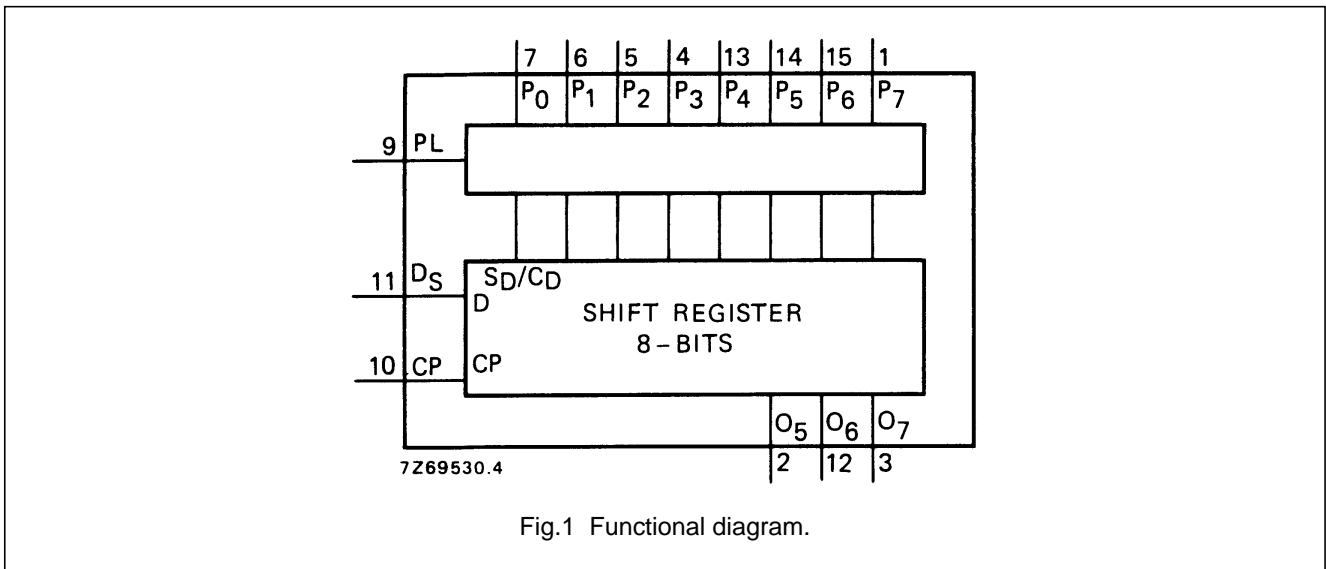
8-bit static shift register

HEF4021B MSI

DESCRIPTION

The HEF4021B is an 8-bit static shift register (parallel-to-serial converter) with a synchronous serial data input (D_S), a clock input (CP), an asynchronous active HIGH parallel load input (PL), eight asynchronous parallel data inputs (P_0 to P_7) and buffered parallel outputs from the last three stages (O_5 to O_7).

Each register stage is a D-type master-slave flip-flop with a set direct/clear direct input. Information on P_0 to P_7 is asynchronously loaded into the register while PL is HIGH, independent of CP and DS. When PL is LOW, data on D_S is shifted into the first register position and all the data in the register is shifted one position to the right on the LOW to HIGH transition of CP. Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.



- HEF4021BP(N): 16-lead DIL; plastic (SOT38-1)
- HEF4021BD(F): 16-lead DIL; ceramic (cerdip) (SOT74)
- HEF4021BT(D): 16-lead SO; plastic (SOT109-1)
- (): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

PINNING

- PL parallel load input
- P_0 to P_7 parallel data inputs
- D_S serial data input
- CP clock input (LOW to HIGH edge-triggered)
- O_5 to O_7 buffered parallel outputs from the last three stages

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FUNCTION TABLES

Serial operation

n	INPUTS			OUTPUTS		
	CP	D _S	PL	O ₅	O ₆	O ₇
1	↗	D ₁	L	X	X	X
2	↗	D ₂	L	X	X	X
3	↗	D ₃	L	X	X	X
6	↗	X	L	D ₁	X	X
7	↗	X	L	D ₂	D ₁	X
8	↗	X	L	D ₃	D ₂	D ₁
	↘	X	L	no change		

Parallel operation

n	INPUTS			OUTPUTS		
	CP	D _S	PL	O ₅	O ₆	O ₇
	X	X	H	P ₅	P ₆	P ₇

Notes

- H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial
↗ = positive-going transition
↘ = negative-going transition
D_n = either HIGH or LOW
n = number of clock pulse transitions

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA	
Propagation delays	5	CP → O _n HIGH to LOW	t _{PHL}	125	250	ns	98 ns + (0,55 ns/pF) C _L
				55	110	ns	44 ns + (0,23 ns/pF) C _L
				40	80	ns	32 ns + (0,16 ns/pF) C _L
	5	LOW to HIGH	t _{PLH}	115	230	ns	88 ns + (0,55 ns/pF) C _L
				50	100	ns	39 ns + (0,23 ns/pF) C _L
				40	80	ns	32 ns + (0,16 ns/pF) C _L
PL → O _n	5	HIGH to LOW	t _{PHL}	120	240	ns	93 ns + (0,55 ns/pF) C _L
				55	110	ns	44 ns + (0,23 ns/pF) C _L
				40	80	ns	32 ns + (0,16 ns/pF) C _L
	5	LOW to HIGH	t _{PLH}	105	210	ns	78 ns + (0,55 ns/pF) C _L
				50	100	ns	39 ns + (0,23 ns/pF) C _L
				40	80	ns	32 ns + (0,16 ns/pF) C _L
Output transition times	5	HIGH to LOW	t _{THL}	60	120	ns	10 ns + (1,0 ns/pF) C _L
				30	60	ns	9 ns + (0,42 ns/pF) C _L
				20	40	ns	6 ns + (0,28 ns/pF) C _L
	5	LOW to HIGH	t _{TLH}	60	120	ns	10 ns + (1,0 ns/pF) C _L
				30	60	ns	9 ns + (0,42 ns/pF) C _L
				20	40	ns	6 ns + (0,28 ns/pF) C _L

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AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V _{DD} V	SYMBOL	MIN.	TYP.	MAX.	
Set-up time D _S → CP	5	t _{su}	25	-15	ns	see also waveforms Figs 4 and 5
	10		25	-10	ns	
	15		15	-5	ns	
P _n → PL	5	t _{su}	50	25	ns	
	10		30	10	ns	
	15		20	5	ns	
Hold times D _S → CP	5	t _{hold}	40	20	ns	
	10		20	10	ns	
	15		15	8	ns	
P _n → PL	5	t _{hold}	15	-10	ns	
	10		15	0	ns	
	15		15	0	ns	
Minimum clock pulse width; LOW	5	t _{WCPL}	70	35	ns	
	10		30	15	ns	
	15		24	12	ns	
Minimum PL pulse width; HIGH	5	t _{WPLH}	70	35	ns	
	10		30	15	ns	
	15		24	12	ns	
Recovery time for PL	5	t _{RPL}	50	10	ns	
	10		40	5	ns	
	15		35	5	ns	
Maximum clock pulse frequency	5	f _{max}	6	13	MHz	
	10		15	30	MHz	
	15		20	40	MHz	

	V _{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power dissipation per package (P)	5	900 f _i + ∑ (f _o C _L) × V _{DD} ²	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) ∑ (f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
	10	4 300 f _i + ∑ (f _o C _L) × V _{DD} ²	
	15	12 000 f _i + ∑ (f _o C _L) × V _{DD} ²	

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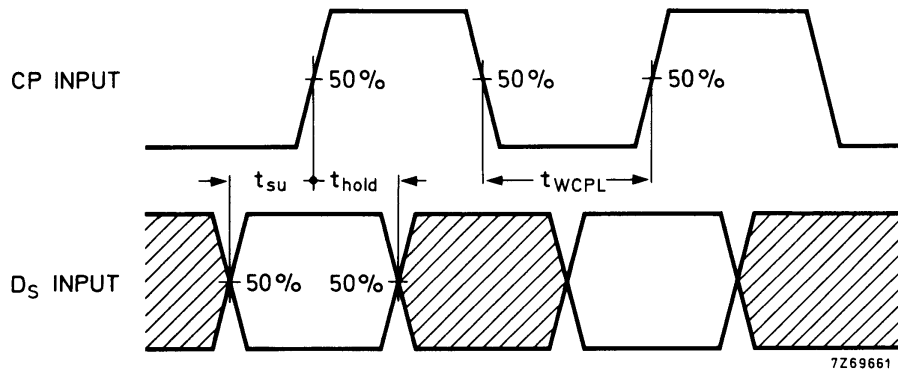


Fig.4 Waveforms showing minimum clock pulse width, set-up and hold time for CP and D_S.

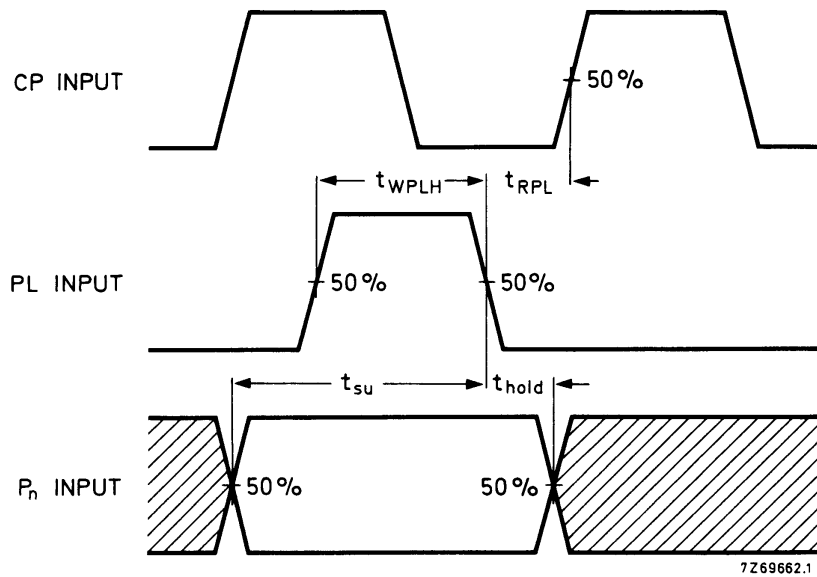


Fig.5 Waveforms showing minimum PL pulse width, recovery time for PL, and set-up and hold times for P_n to PL. Set-up and hold times are shown as positive values but may be specified as negative values.



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