

## 2.4GHz - 2.5GHz 250mW Power Amplifier



The Intersil 2.4GHz PRISM™ chip set is a highly integrated five-chip solution for RF modems employing Direct Sequence Spread Spectrum (DSSS) signaling. The HFA3925 2.4GHz-

2.5GHz, 250mW power amplifier is one of the five chips in the PRISM™ chip set (see the Typical Application Diagram).

The Intersil HFA3925 is an integrated power amplifier with transmit/receive switch in a low cost SSOP 28 plastic package. The power amplifier delivers +27dB of gain with high efficiency and can be operated with voltages as low as 2.7V. The power amplifier switch is fully monolithic and can be controlled with CMOS logic levels.

The HFA3925 is ideally suited for QPSK, BPSK or other linearly modulated systems in the 2.4GHz Industrial, Scientific, and Medical (ISM) frequency band. It can also be used in GFSK systems where levels of +25dBm are required. Typical applications include Wireless Local Area Network (WLAN) and wireless portable data collection.

**REMEMBER:** Always apply Negative power to the VG pins before applying the Positive V<sub>DD</sub> bias. Failure to do so may result in the destruction of the HFA3925 Power Amplifier.

## Features

- Highly Integrated Power Amplifier with T/R Switch
- Operates Over 2.7V to 6V Supply Voltage
- High Linear Output Power (P<sub>1dB</sub>: +24dBm)
- Individual Gate Control for Each Amplifier Stage
- Low Cost SSOP-28 Plastic Package

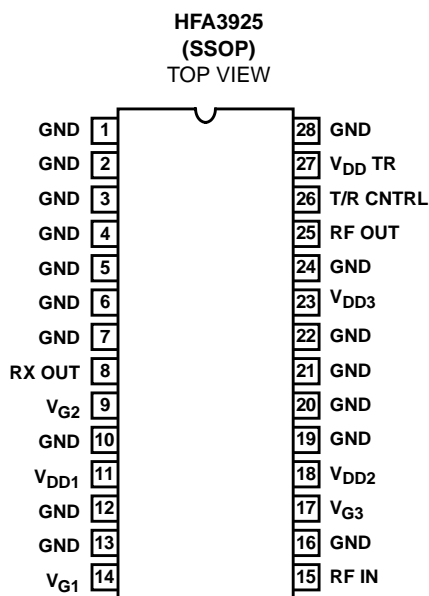
## Applications

- Systems Targeting IEEE 802.11 Standard
- TDD Quadrature-Modulated Communication Systems
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems
- TDMA Packet Protocol Radios
- PCS/Wireless PBX

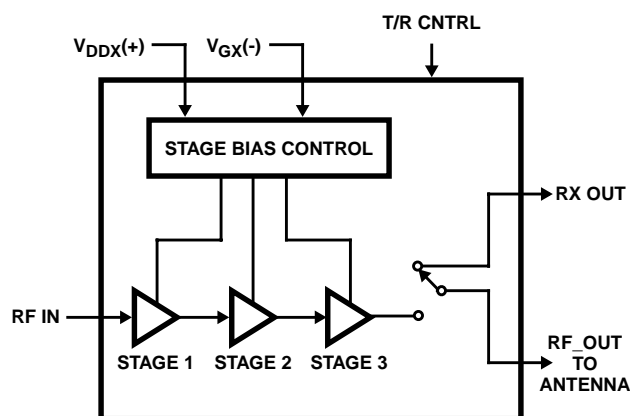
## Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HFA3925IA	-40 to 85	28 Ld SSOP	M28.15
HFA3925IA96	-40 to 85	Tape and Reel	

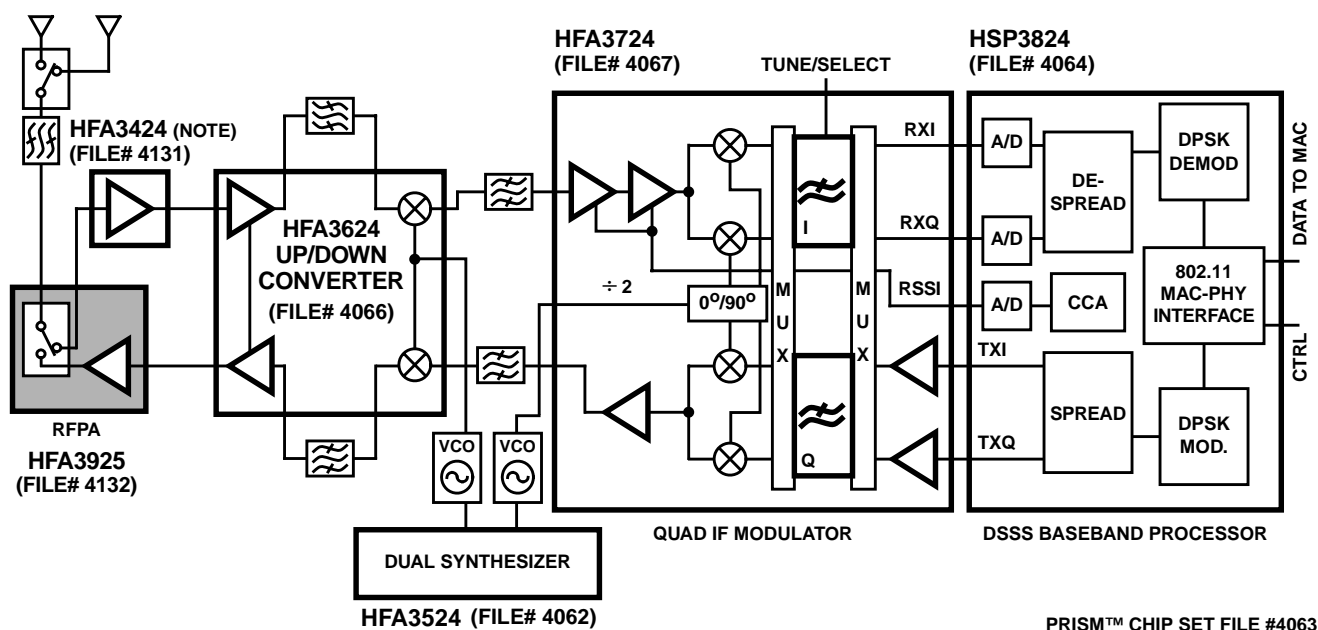
## Pinout



## Functional Block Diagram



**Typical Application Diagram**



**TYPICAL TRANSCEIVER APPLICATION USING THE HFA3925**

NOTE: Required for systems targeting 802.11 specifications.

For additional information on the PRISM™ chip set, call (407) 724-7800 to access Intersil AnswerFAX system. When prompted, key in the four-digit document number (File #) of the datasheets you wish to receive.

The four-digit file numbers are shown in the Typical Application Diagram, and correspond to the appropriate circuit

# HFA3925

## Absolute Maximum Ratings

Maximum Input Power (Note 2) ..... +23dBm  
 Operating Voltages (Notes 2, 3).....  $V_{DD} = 8V, V_{GG} = -8V$

## Thermal Information

Thermal Resistance (Typical, Note 1)  $\theta_{JA}$  (°C/W)  
 SSOP Package ..... 88  
 Maximum Storage Temperature Range..... -65°C to 150°C

## Operating Conditions

Temperature Range ..... -40°C to 85°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

1.  $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications $T_A = 25^\circ\text{C}, Z_0 = 50\Omega, V_{DD} = +5V, P_{IN} = -30\text{dBm}, f = 2.45\text{GHz}$ , Unless Otherwise Specified

PARAMETER	MIN	TYP	MAX	UNITS
<b>POWER AMPLIFIER</b>				
Linear Gain	27	28	32	dB
VSWR In/Out	-	1.75:1	-	
Input Return Loss	-	-11.3	-	dB
Output Return Loss	-	-11.3	-	dB
Output Power at $P_{1\text{dB}}$	22.5	24.5	-	dBm
Second Harmonic at $P_{1\text{dB}}$	-	-20	0	dBc
Third Harmonic at $P_{1\text{dB}}$	-	-30	-10	dBc
IDD at $P_{1\text{dB}}$ ( $V_{DD1} + V_{DD2} + V_{DD3}$ )	-	270	375	mA

### NOTES:

2. Ambient temperature ( $T_A$ ) = 25°C.
3.  $|V_{DD}| + |V_{GG}|$  not to exceed 12V.

## Pin Description

PINS	SYMBOL	DESCRIPTION
1	GND	DC and RF Ground.
2	GND	DC and RF Ground.
3	GND	DC and RF Ground.
4	GND	DC and RF Ground.
5	GND	DC and RF Ground.
6	GND	DC and RF Ground.
7	GND	DC and RF Ground.
8	RX OUT	Output of T/R Switch for receive mode.
9	$V_{G2}$	Negative bias control for the second PA stage, adjusted to set $V_{DD2}$ quiescent bias current, which is typically 53mA. Typical voltage at pin = -0.75V. Input impedance: > 1M $\Omega$ .
10	GND	DC and RF Ground.
11	$V_{DD1}$	Positive bias for the first stage of the PA, 2.7V to 6V.
12	GND	DC and RF Ground.
13	GND	DC and RF Ground.
14	$V_{G1}$	Negative bias control for the first PA stage, adjusted to set $V_{DD1}$ quiescent bias current, which is typically 20mA. Typical voltage at pin = -0.75V. Input impedance: > 1M $\Omega$ .
15	RF IN	RF Input of the Power Amplifier.
16	GND	DC and RF Ground.

**Pin Description** (Continued)

PINS	SYMBOL	DESCRIPTION
17	$V_{G3}$	Negative bias control for the third PA stage, adjusted to set $V_{DD3}$ quiescent bias current, which is typically 90mA. Typical voltage at pin = -0.95V. Input impedance: > 1M $\Omega$ .
18	$V_{DD2}$	Positive bias for the second stage of the PA. 2.7V to 6V.
19-22	GND	DC and RF Ground.
23	$V_{DD3}$	Positive bias for the third stage of the PA. 2.7V to 6V.
24	GND	DC and RF Ground.
25	RF OUT	RF output of T/R switch and power amplifier for transmit mode.
26	T/R CTRL	0V for transmit mode, +5V for receive mode. Low < = 0.2V, high > = $V_{DD}$ -0.2V.
27	$V_{DD}$ TR	$V_{DD}$ for T/R switch.
28	GND	DC and RF Ground.

NOTE: Process variation will effect  $V_{G3}$  voltage requirement to develop 90mA stage 3 quiescent current, maximum range = -0.69V to -1.04V.

**Typical Performance Curves**

**Power Amplifier Small Signal Performance** NOTE: All data measured at  $T_A = 25^\circ\text{C}$  and  $V_{G1}$ ,  $V_{G2}$  and  $V_{G3}$  adjusted for first stage quiescent current of 20mA, second stage current of 53mA and third stage current of 90mA, respectively

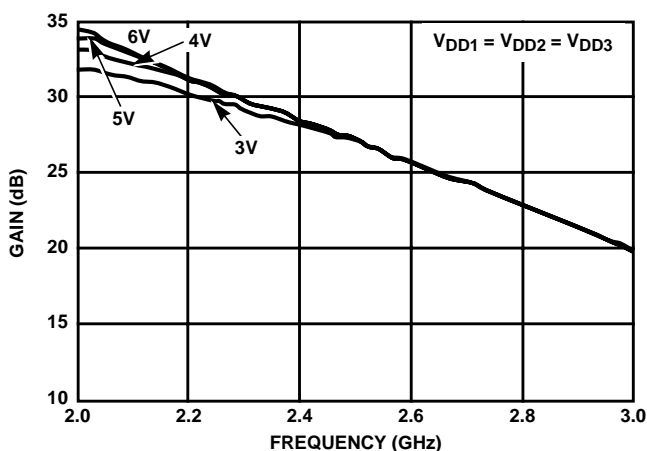


FIGURE 1. LINEAR GAIN

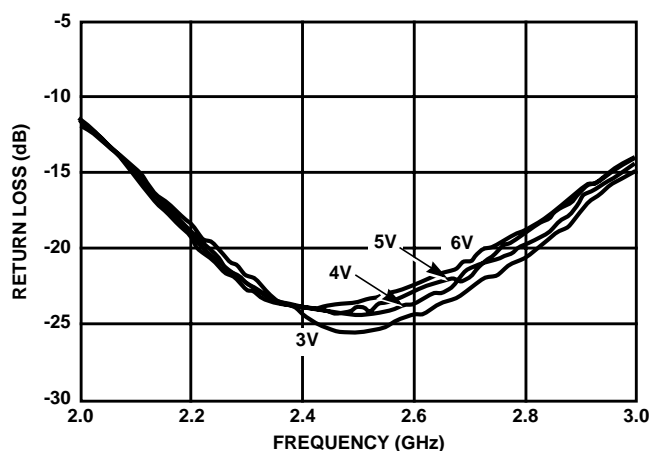


FIGURE 2. INPUT MATCH

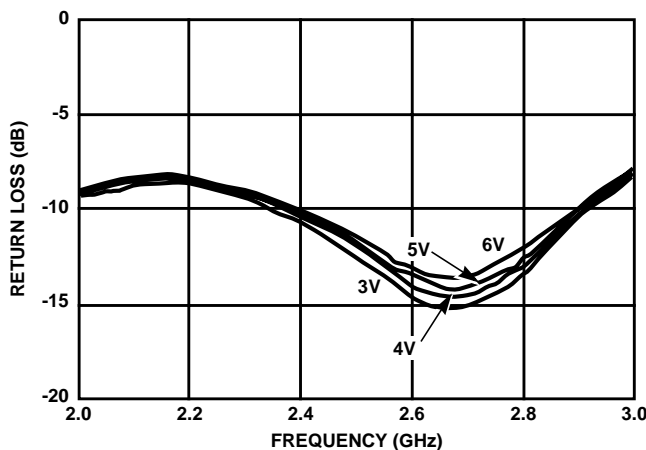


FIGURE 3. OUTPUT MATCH

**Typical Performance Curves** (Continued)

**Power Amplifier CW Performance at Various Supply Voltages** NOTE: All data measured at  $T_A = 25^\circ\text{C}$  and  $V_{G1}$ ,  $V_{G2}$  and  $V_{G3}$  adjusted for first stage quiescent current of 20mA, second stage current of 53mA and third stage current of 90mA, respectively.

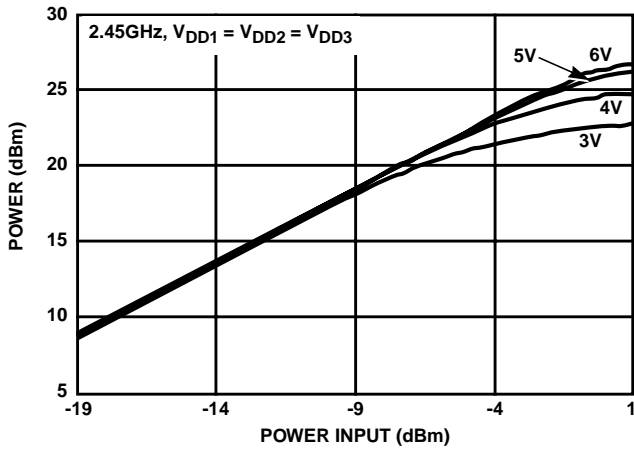


FIGURE 4. POWER OUTPUT

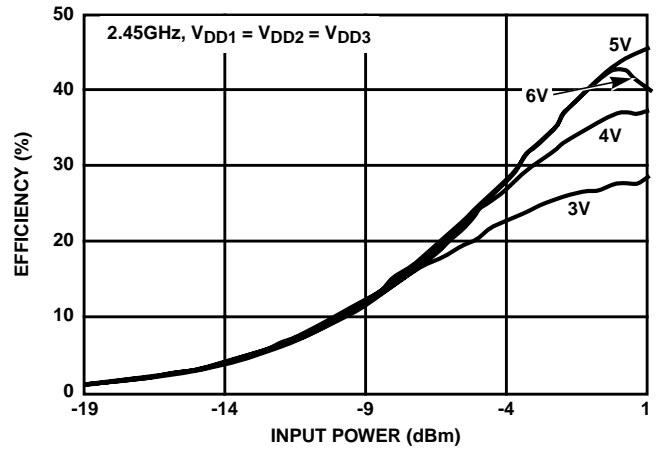


FIGURE 5. POWER ADDED EFFICIENCY

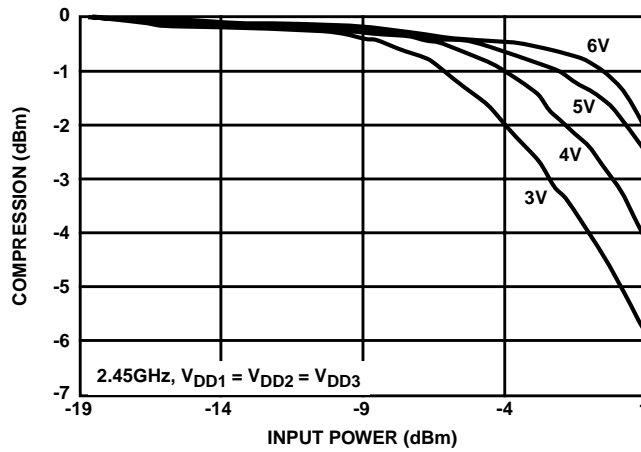


FIGURE 6. GAIN COMPRESSION

**Power Amplifier Temperature Performance** NOTE: All data measured at  $T_A = 25^\circ\text{C}$  and  $V_{G1}$ ,  $V_{G2}$  and  $V_{G3}$  adjusted for first stage quiescent current of 20mA, second stage current of 53mA and third stage current of 90mA, respectively.

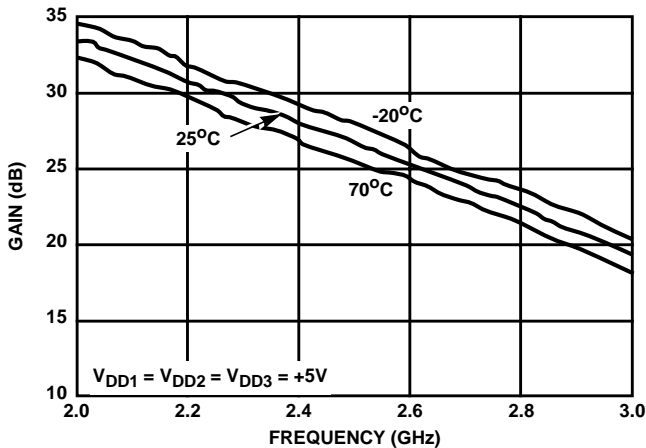


FIGURE 7. LINEAR GAIN

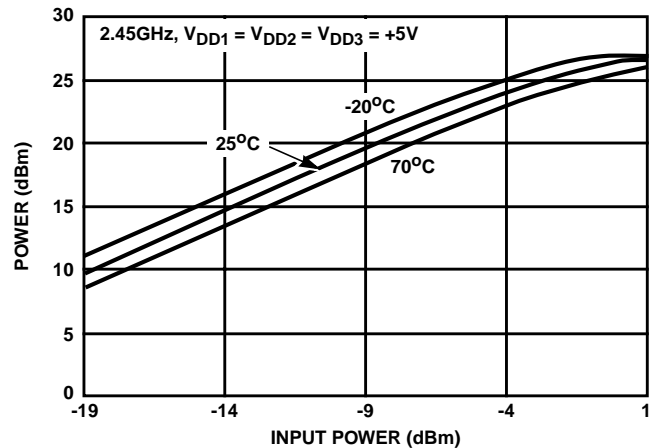


FIGURE 8. POWER OUTPUT

Typical Performance Curves (Continued)

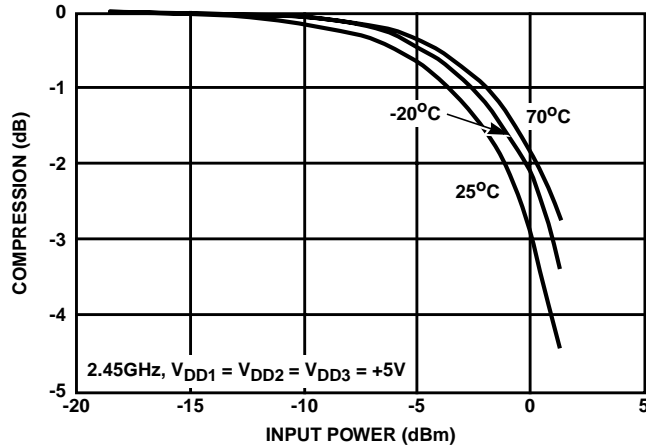


FIGURE 9. GAIN COMPRESSION

**Power Amplifier Spurious Response at Various Supply Voltages** NOTE: All data measured at  $T_A = 25^\circ\text{C}$  and  $V_{G1}$ ,  $V_{G2}$  and  $V_{G3}$  adjusted for first stage quiescent current of 20mA, second stage current of 53mA and third stage current of 90mA, respectively.

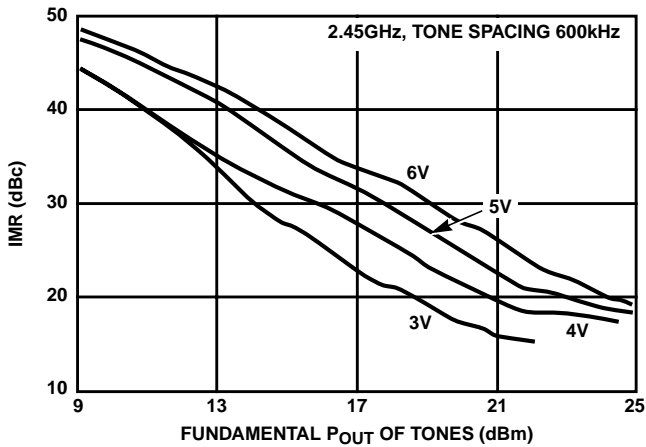


FIGURE 10. THIRD ORDER INTERMODULATION RATIO

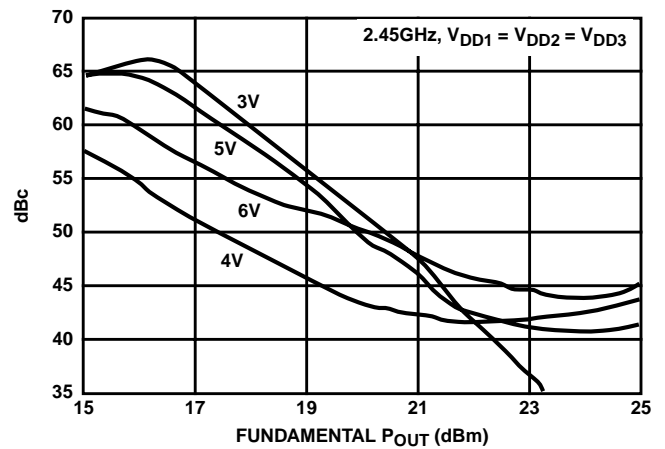


FIGURE 11. SECOND HARMONIC RATIO

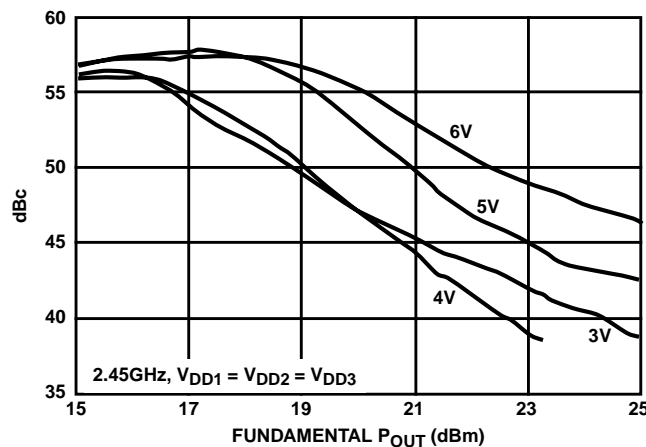


FIGURE 12. THIRD HARMONIC RATIO

**Typical Performance Curves** (Continued)

**Transmit/Receive Switch Performance** NOTE: All data measured with  $V_{DD}$  TR = +5V,  $T_A$  = 25°C.

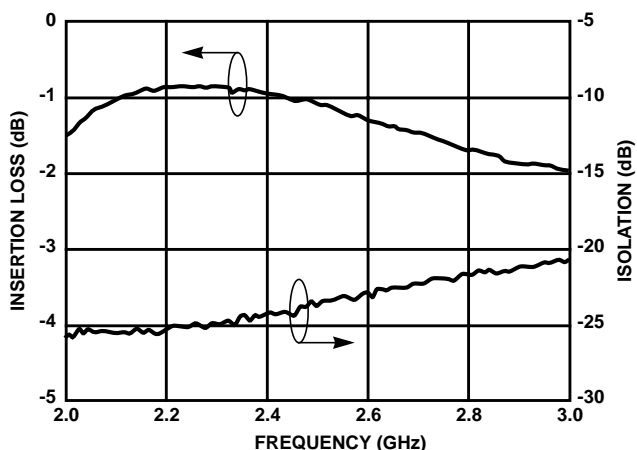


FIGURE 13. RECEIVE MODE T/R INSERTION LOSS/ISOLATION

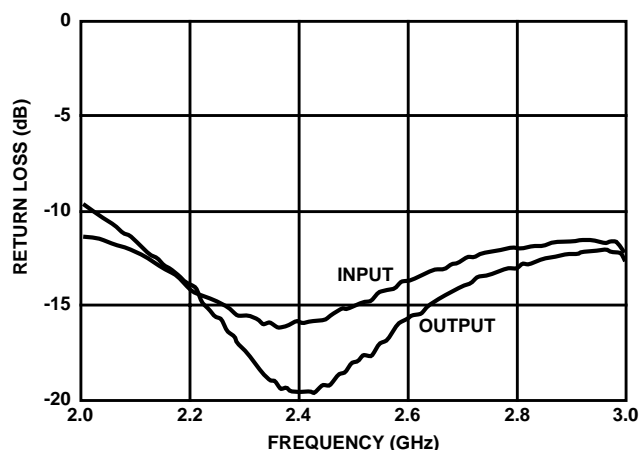
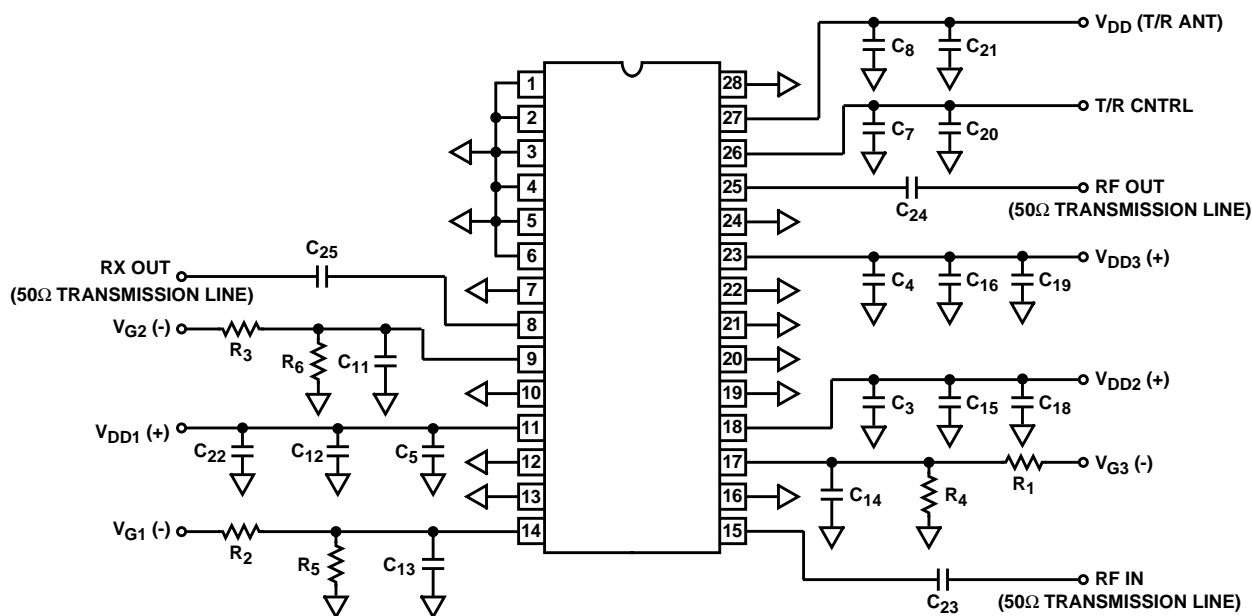


FIGURE 14. RECEIVE MODE T/R SWITCH MATCH

**Typical Application Example**



**EXTERNAL CIRCUITRY PARTS LIST**

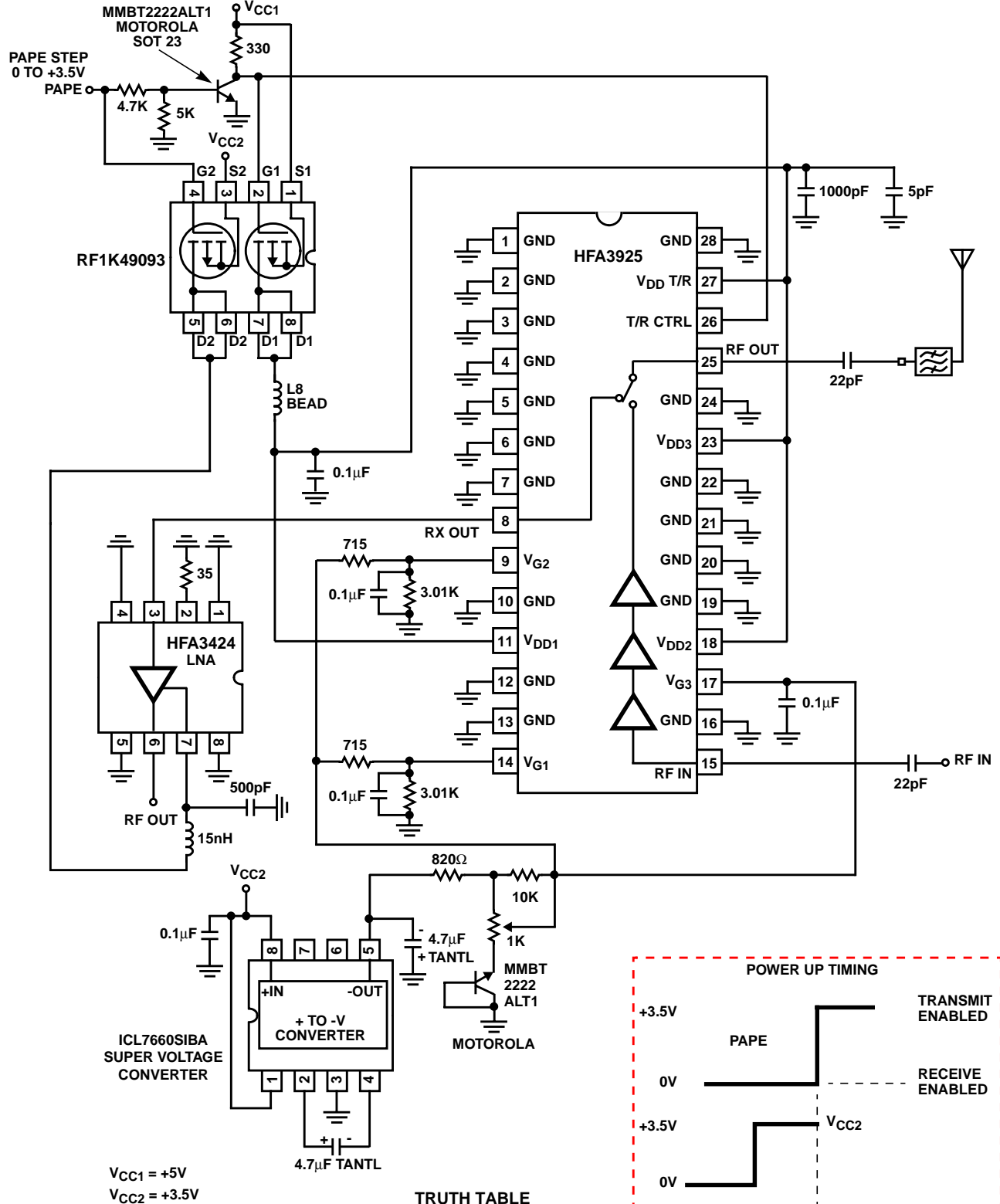
LABEL	VALUE	PURPOSE
C <sub>3</sub> -C <sub>5</sub> , C <sub>7</sub> , C <sub>8</sub>	22pF	Bypass (GHz)
C <sub>23</sub> -C <sub>24</sub>	22pF	DC Block
C <sub>11</sub> -C <sub>16</sub>	1000pF	Bypass (MHz)
C <sub>18</sub> -C <sub>22</sub>	0.01μF	Bypass (kHz)
R <sub>1</sub> , R <sub>6</sub>	1.5kΩ	FET Gate Divider Network
R <sub>3</sub> , R <sub>5</sub>	5kΩ	
R <sub>2</sub>	12kΩ	
R <sub>4</sub>	1kΩ	

NOTE: All off-chip components are low cost surface mount components obtainable from multiple sources. (0.020in x 0.040in or 0.030in x 0.050in.)

# HFA3925

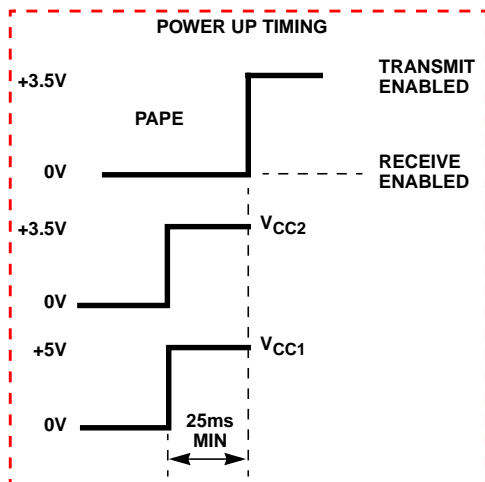
## Typical Application Diagram

Positive Supply, Single Stage 3 Adjustment Circuit



TRUTH TABLE

PAPE	TR/CTRL	MODE
Low (0)	High (1)	Receive
High (1)	Low (0)	Transmit



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