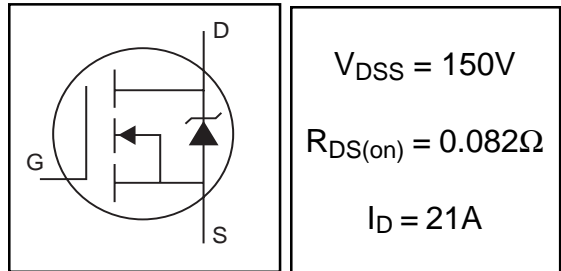


- Advanced Process Technology
- Surface Mount (IRF3315S)
- Low-profile through-hole (IRF3315L)
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

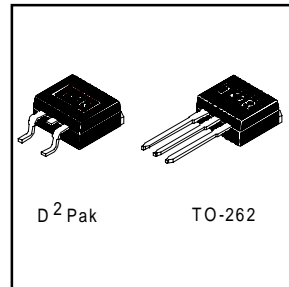


Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF3315L) is available for low-profile applications.



Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---------------------------------|---|------------------------|-------|
| $I_D @ T_C = 25^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10V \textcircled{5}$ | 21 | A |
| $I_D @ T_C = 100^\circ\text{C}$ | Continuous Drain Current, $V_{GS} @ 10V \textcircled{5}$ | 15 | |
| I_{DM} | Pulsed Drain Current $\textcircled{1} \textcircled{5}$ | 84 | |
| $P_D @ T_A = 25^\circ\text{C}$ | Power Dissipation | 3.8 | W |
| $P_D @ T_C = 25^\circ\text{C}$ | Power Dissipation | 94 | W |
| | Linear Derating Factor | 0.63 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy $\textcircled{2} \textcircled{5}$ | 350 | mJ |
| I_{AR} | Avalanche Current $\textcircled{1}$ | 12 | A |
| E_{AR} | Repetitive Avalanche Energy $\textcircled{1}$ | 9.4 | mJ |
| dv/dt | Peak Diode Recovery dv/dt $\textcircled{3} \textcircled{5}$ | 2.5 | V/ns |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case) | |

Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|-----------------|--|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case | — | 1.6 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mounted, steady-state)** | — | 40 | |

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---------------------------------|--------------------------------------|------|-------|-----------|----------|--|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 150 | — | — | V | $V_{GS} = 0V, I_D = 250\mu A$ |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | — | 0.187 | — | V/°C | Reference to $25^\circ\text{C}, I_D = 1mA$ ⑤ |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | — | — | 0.082 | Ω | $V_{GS} = 10V, I_D = 12A$ ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 2.0 | — | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250\mu A$ |
| g_{fs} | Forward Transconductance | 17 | — | — | S | $V_{DS} = 50V, I_D = 12A$ ⑤ |
| I_{DSS} | Drain-to-Source Leakage Current | — | — | 25 250 | μA | $V_{DS} = 150V, V_{GS} = 0V$ $V_{DS} = 120V, V_{GS} = 0V, T_J = 125^\circ\text{C}$ |
| I_{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | $V_{GS} = 20V$ |
| | Gate-to-Source Reverse Leakage | — | — | -100 | nA | $V_{GS} = -20V$ |
| Q_g | Total Gate Charge | — | — | 95 | nC | $I_D = 12A$ |
| Q_{gs} | Gate-to-Source Charge | — | — | 11 | nC | $V_{DS} = 120V$ |
| Q_{gd} | Gate-to-Drain ("Miller") Charge | — | — | 47 | nC | $V_{GS} = 10V$, See Fig. 6 and 13 ④⑤ |
| $t_{d(on)}$ | Turn-On Delay Time | — | 9.6 | — | ns | $V_{DD} = 75V$ $I_D = 12A$ $R_G = 5.1\Omega$ $R_D = 5.9\Omega$, See Fig. 10 ④⑤ |
| t_r | Rise Time | — | 32 | — | | |
| $t_{d(off)}$ | Turn-Off Delay Time | — | 49 | — | | |
| t_f | Fall Time | — | 38 | — | | |
| L_S | Internal Source Inductance | — | 7.5 | — | nH | Between lead, and center of die contact |
| C_{iss} | Input Capacitance | — | 1300 | — | pF | $V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$, See Fig. 5⑤ |
| C_{oss} | Output Capacitance | — | 300 | — | | |
| C_{rss} | Reverse Transfer Capacitance | — | 160 | — | | |

Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------|---|---|------|------|---------|---|
| I_S | Continuous Source Current (Body Diode) | — | — | 21 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| I_{SM} | Pulsed Source Current (Body Diode) ① | — | — | 84 | | |
| V_{SD} | Diode Forward Voltage | — | — | 1.3 | V | $T_J = 25^\circ\text{C}, I_S = 43A, V_{GS} = 0V$ ④ |
| t_{rr} | Reverse Recovery Time | — | 174 | 260 | ns | $T_J = 25^\circ\text{C}, I_F = 43A$ |
| Q_{rr} | Reverse Recovery Charge | — | 1.2 | 1.7 | μC | $di/dt = 100A/\mu s$ ④⑤ |
| t_{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$) | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ\text{C}$, $L = 4.9\text{ mH}$
 $R_G = 25\Omega$, $I_{AS} = 12A$. (See Figure 12)
- ③ $I_{SD} \leq 12A$, $di/dt \leq 140A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ⑤ Uses IRF3315 data and test conditions

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

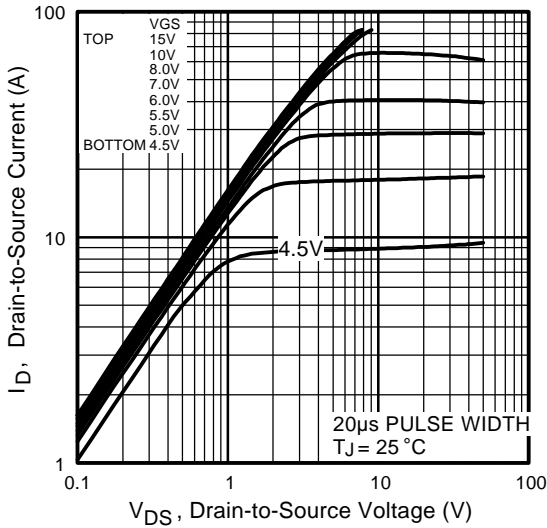


Fig 1. Typical Output Characteristics

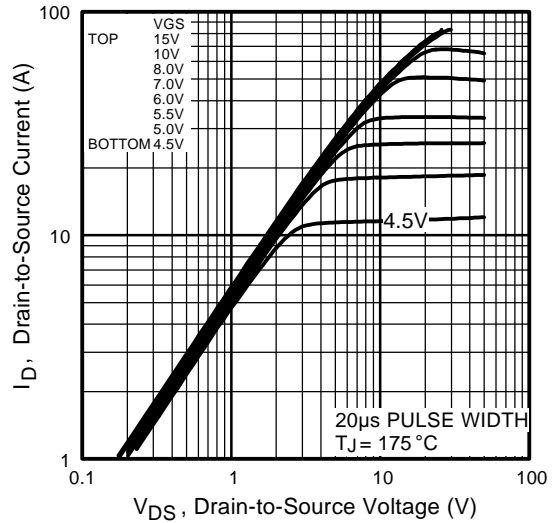


Fig 2. Typical Output Characteristics

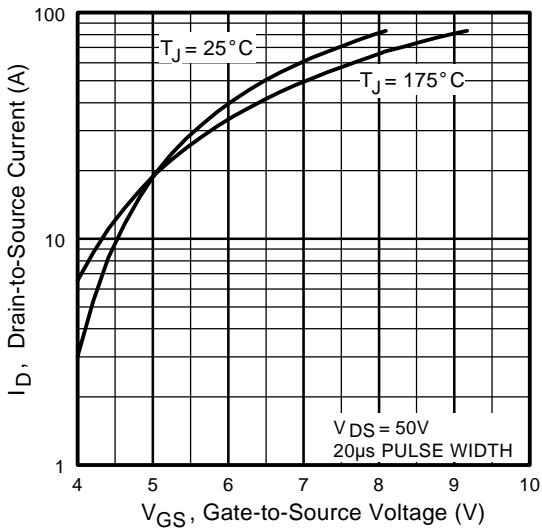


Fig 3. Typical Transfer Characteristics

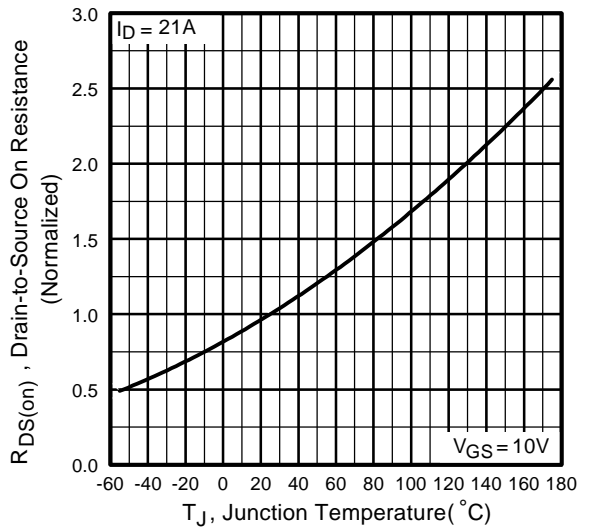


Fig 4. Normalized On-Resistance Vs. Temperature

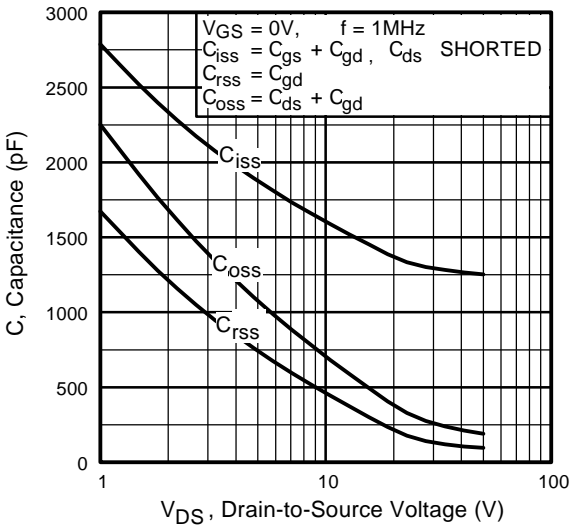


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

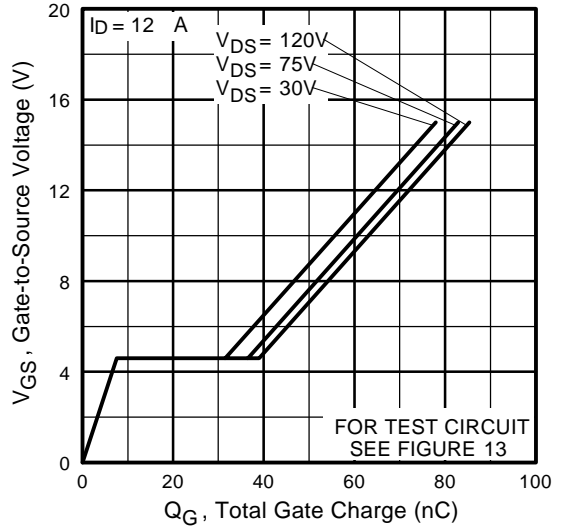


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

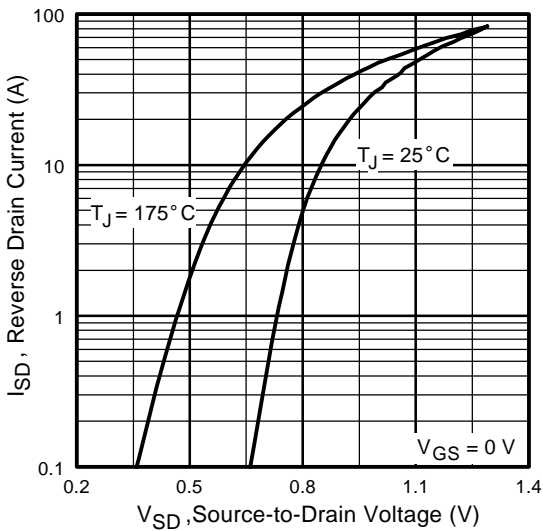


Fig 7. Typical Source-Drain Diode Forward Voltage

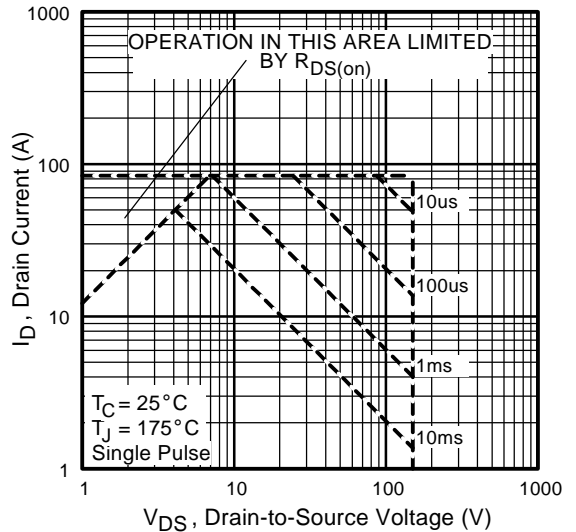


Fig 8. Maximum Safe Operating Area

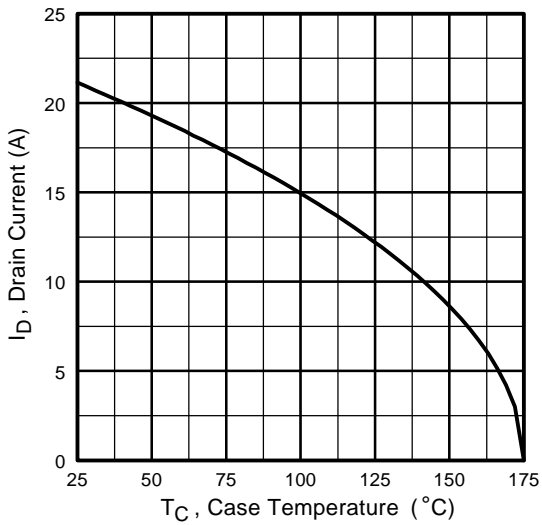


Fig 9. Maximum Drain Current Vs. Case Temperature

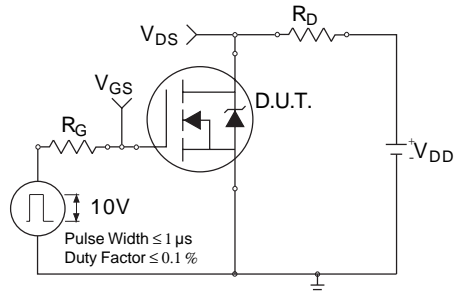


Fig 10a. Switching Time Test Circuit

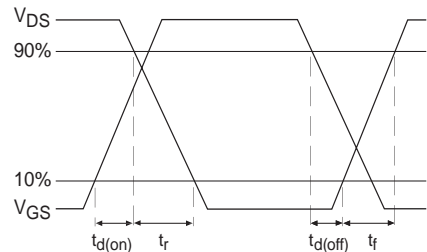


Fig 10b. Switching Time Waveforms

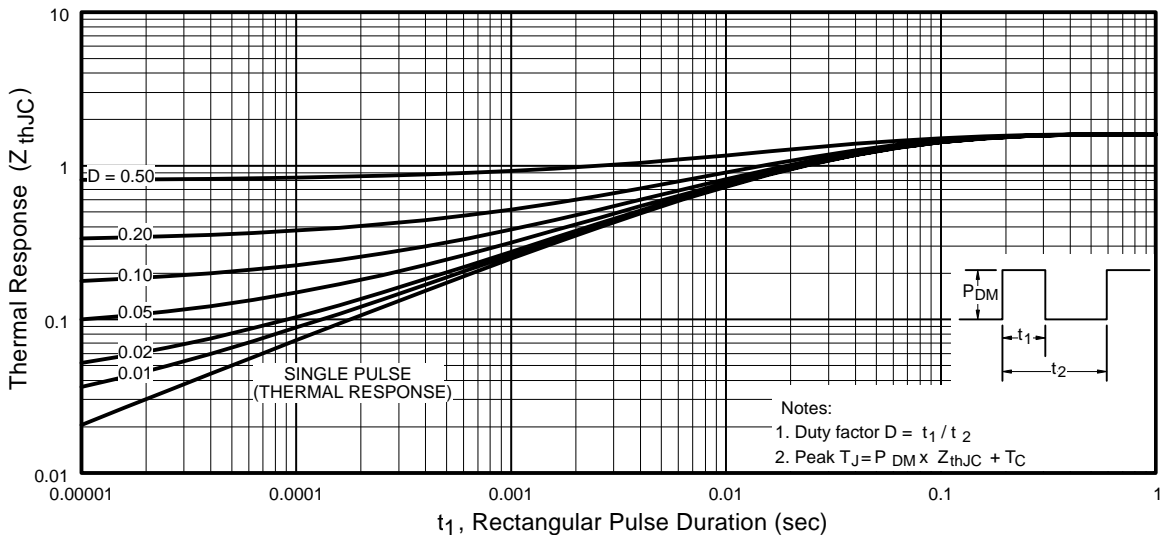


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

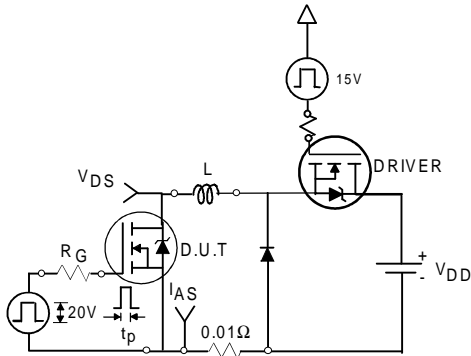


Fig 12a. Unclamped Inductive Test Circuit

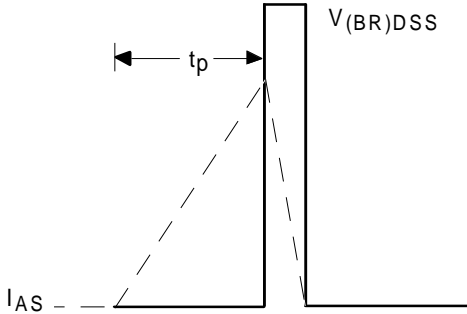


Fig 12b. Unclamped Inductive Waveforms

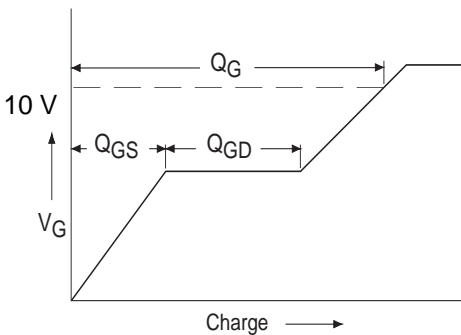


Fig 13a. Basic Gate Charge Waveform

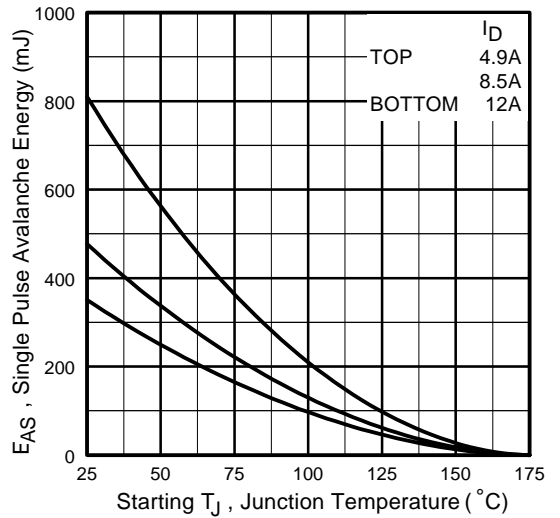


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

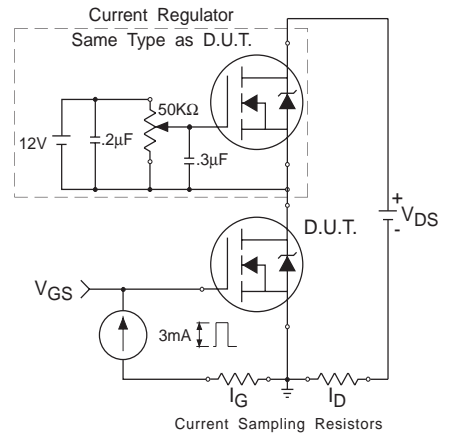
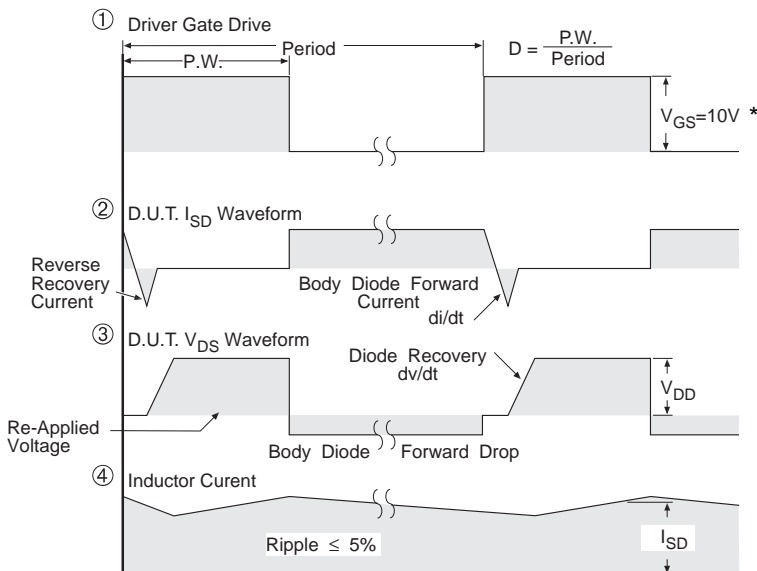
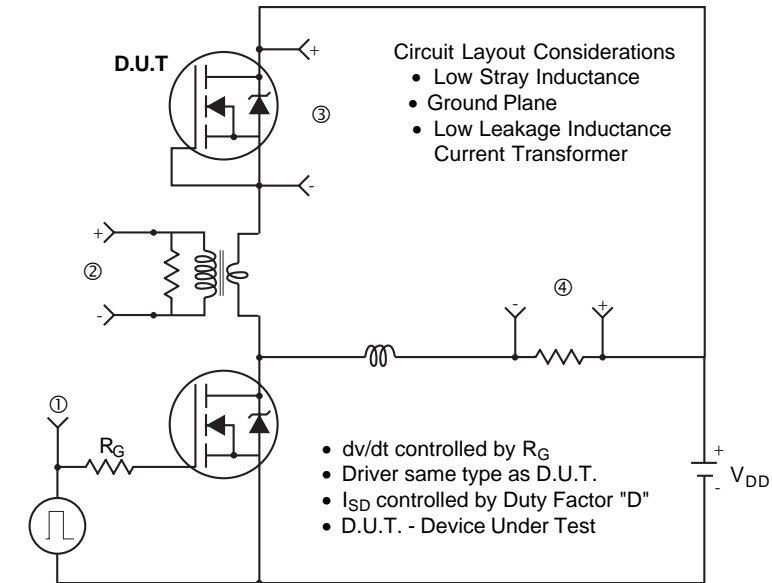


Fig 13b. Gate Charge Test Circuit

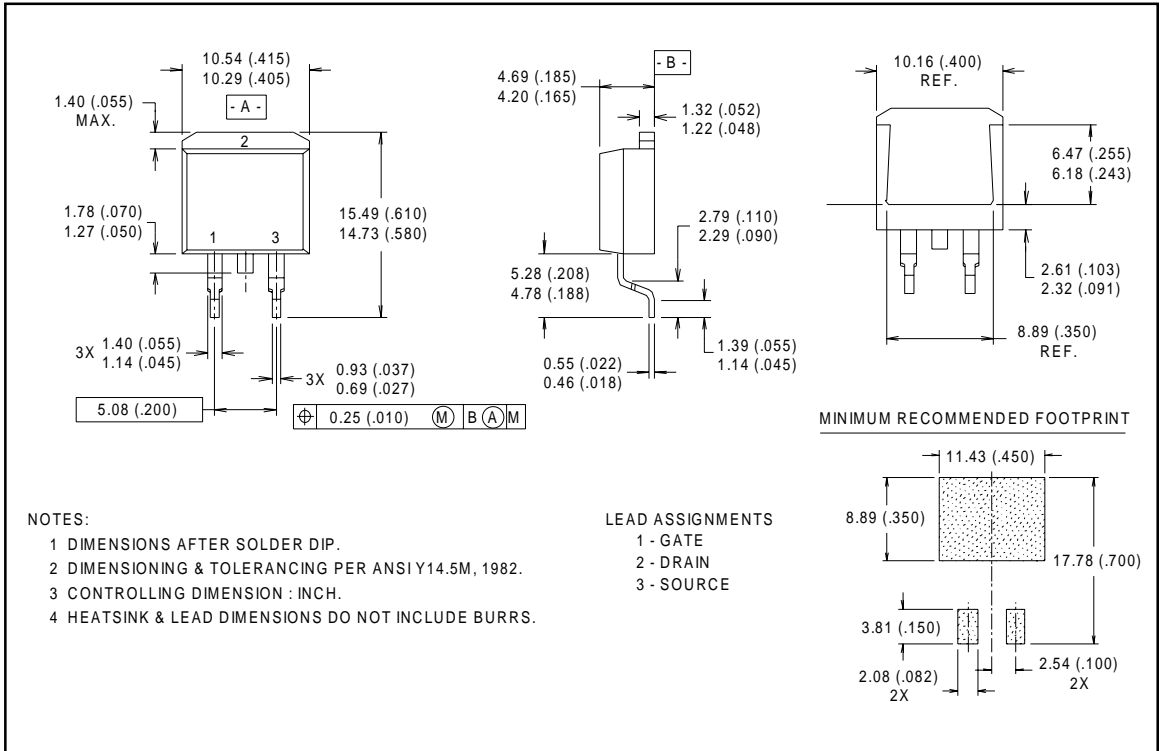
Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

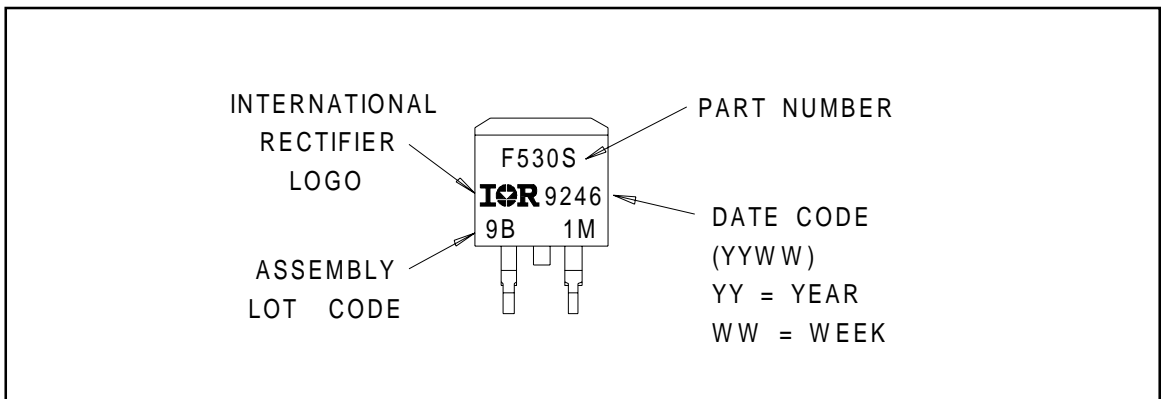
Fig 14. For N-Channel HEXFETS

D²Pak Package Outline



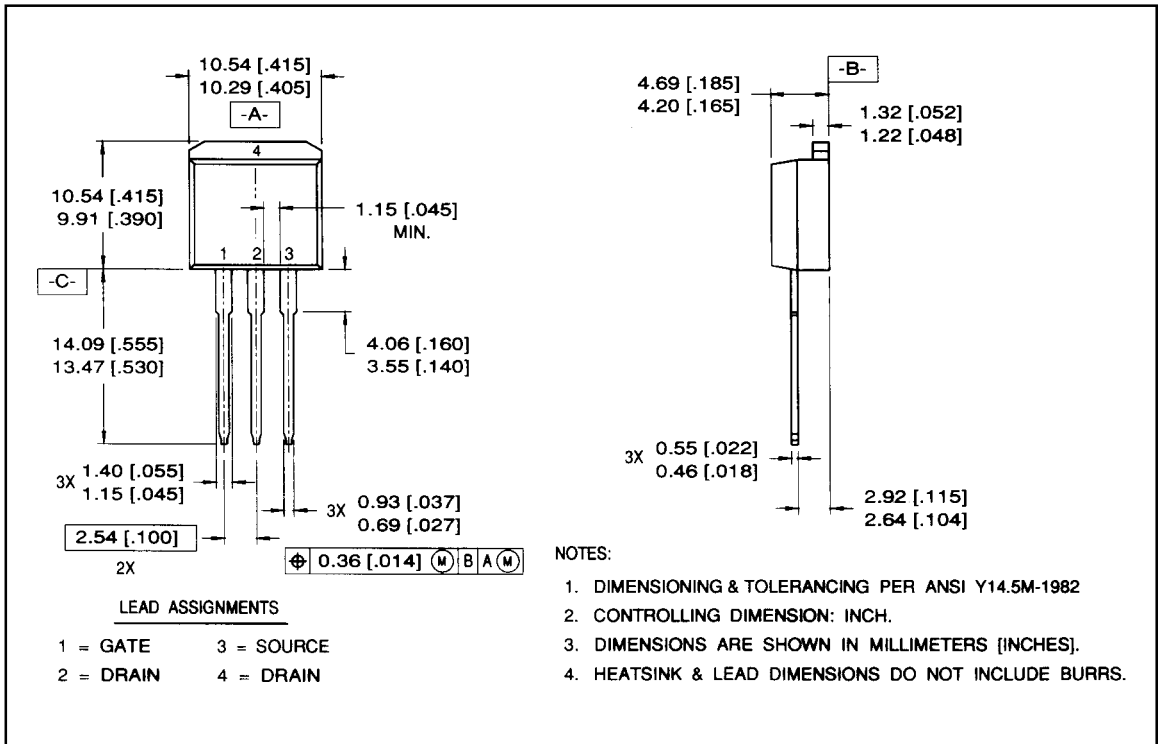
Part Marking Information

D²Pak



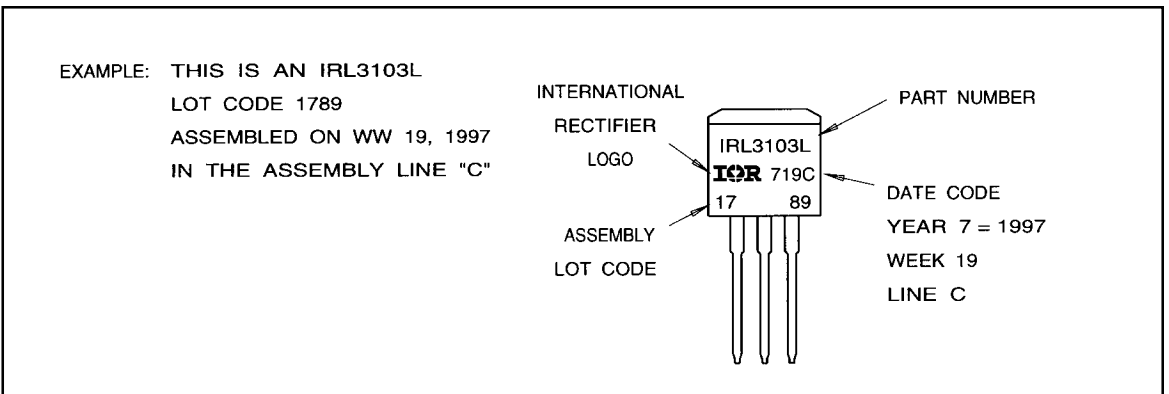
Package Outline

TO-262 Outline



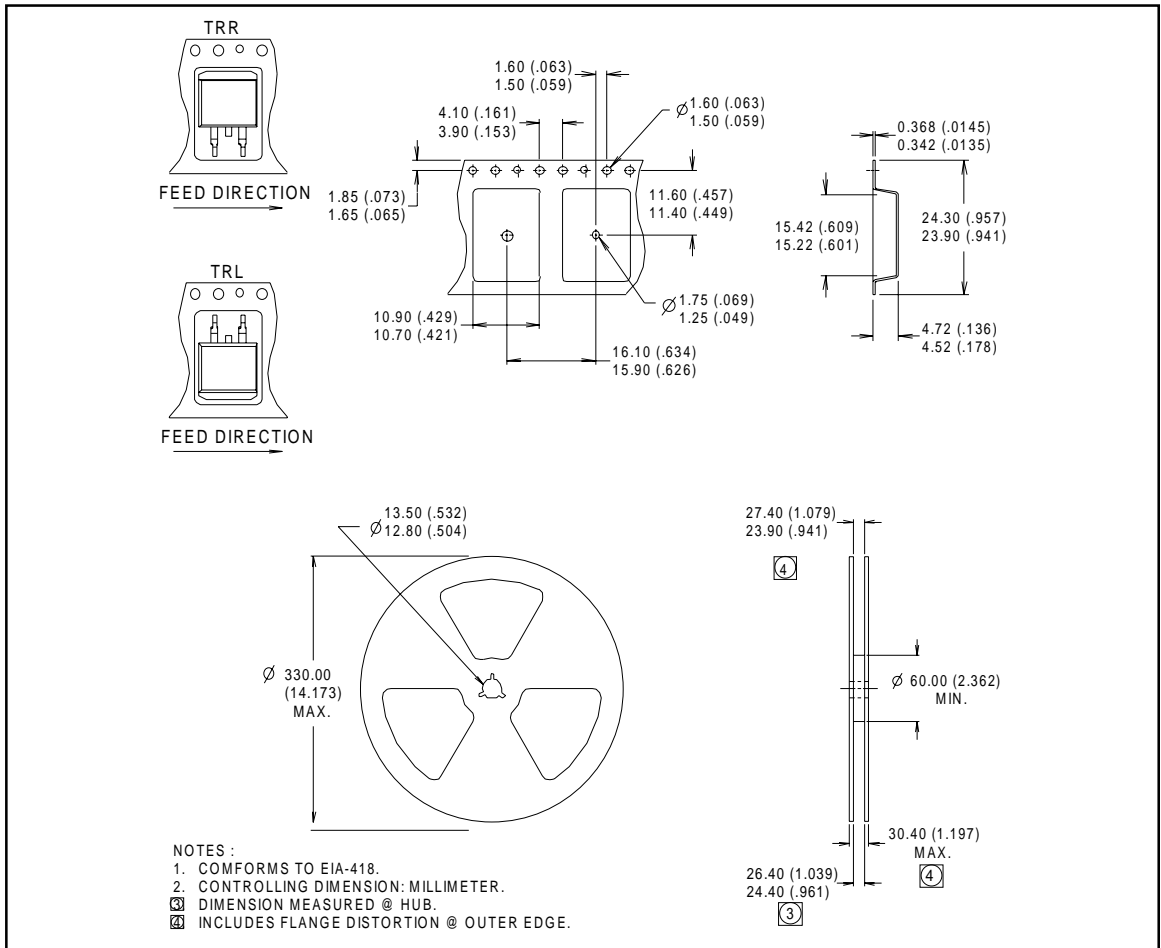
Part Marking Information

TO-262



Tape & Reel Information

D²Pak





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