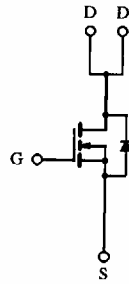
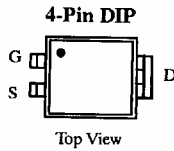


### N-Channel Enhancement-Mode Transistor

#### Product Summary

$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A)
50	0.10	2.4



N-Channel MOSFET

#### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	50	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	
Continuous Drain Current	$I_D$	$T_A = 25^\circ\text{C}$	A
		$T_A = 100^\circ\text{C}$	
Pulsed Drain Current	$I_{DM}$	19	
Power Dissipation	$P_D$	$T_A = 25^\circ\text{C}$	W
		$T_A = 100^\circ\text{C}$	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to 150	$^\circ\text{C}$
Lead Temperature ( $1/16''$ from case for 10 sec.)	$T_L$	300	

**6**  
 N-/P-Channel  
 MOSFETs

#### Thermal Resistance Ratings

Parameter	Symbol	Maximum	Unit
Junction-to-Ambient	$R_{thJA}$	120	$^\circ\text{C/W}$

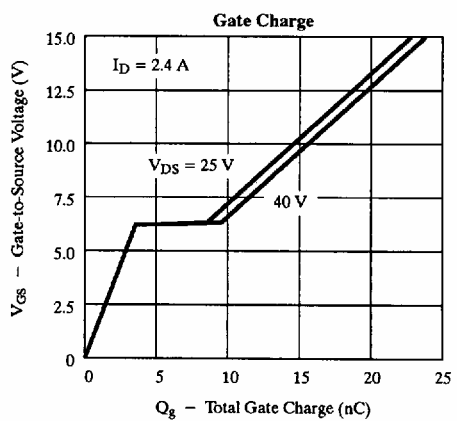
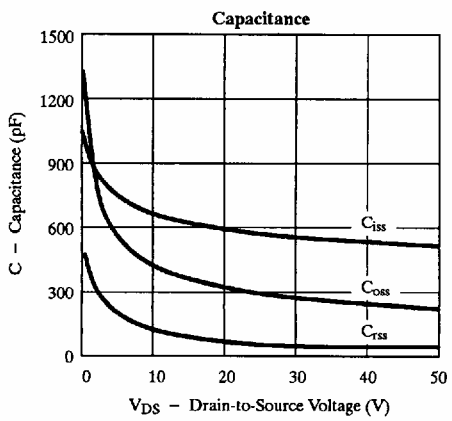
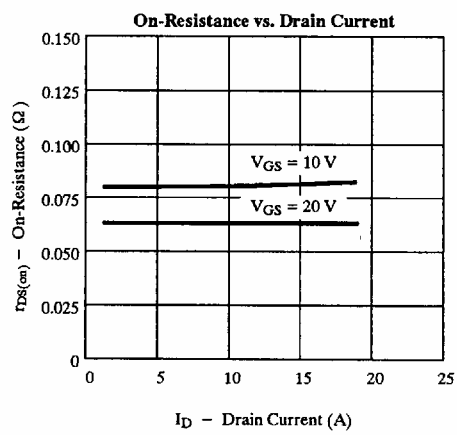
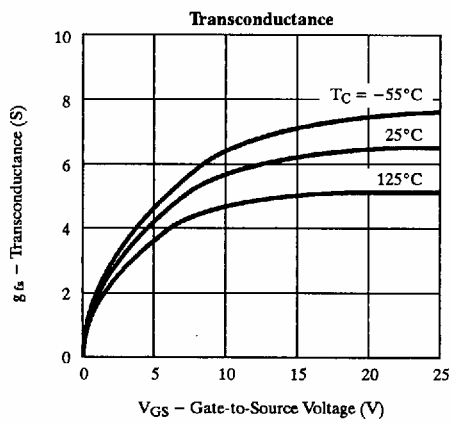
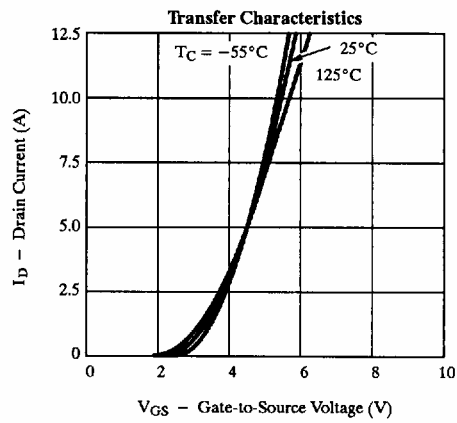
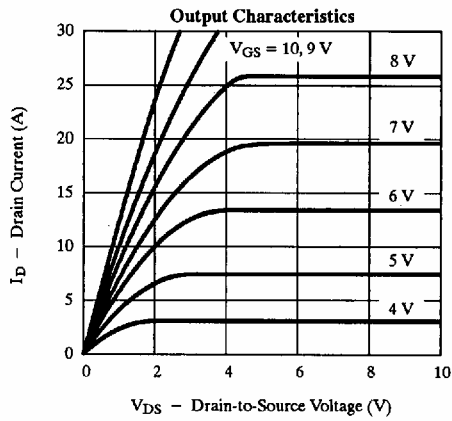
### Specifications ( $T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ <sup>a</sup>	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	50			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.0		4.0	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			$\pm 500$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			250	$\mu\text{A}$
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$			1000	
On-State Drain Current <sup>b</sup>	$I_{D(on)}$	$V_{DS} = 2\text{ V}, V_{GS} = 10\text{ V}$	2.4			A
Drain-Source On-State Resistance <sup>b</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}$		0.08	0.10	$\Omega$
		$V_{GS} = 10\text{ V}, I_D = 1.4\text{ A}, T_J = 125^\circ\text{C}$		0.16	0.18	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}, I_D = 7.5\text{ A}$	4.9	5.5		S
<b>Dynamic</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1\text{ MHz}$		550	850	$\text{pF}$
Output Capacitance	$C_{oss}$			300	350	
Reverse Transfer Capacitance	$C_{rss}$			80	100	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{DS} = 25\text{ V}, V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		13	24	$\text{nC}$
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			3.5		
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			5		
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 25\text{ V}, R_{JL} = 1.7\ \Omega$ $I_D \approx 15\text{ A}, V_{GEN} = 10\text{ V}, R_G = 18\ \Omega$		10	13	$\text{ns}$
Rise Time <sup>c</sup>	$t_r$			60	83	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			30	40	
Fall Time <sup>c</sup>	$t_f$			35	50	
<b>Source-Drain Diode Ratings and Characteristics (<math>T_A = 25^\circ\text{C}</math>)</b>						
Continuous Current	$I_S$				2.4	A
Pulsed Current	$I_{SM}$				19	
Forward Voltage <sup>b</sup>	$V_{SD}$	$I_F = 2.4\text{ A}, V_{GS} = 0\text{ V}$			1.25	V
Reverse Recovery Time	$t_{rr}$	$I_F = 2.4\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$		65		ns
Reverse Recovery Charge	$Q_{rr}$			0.16	0.85	$\mu\text{C}$

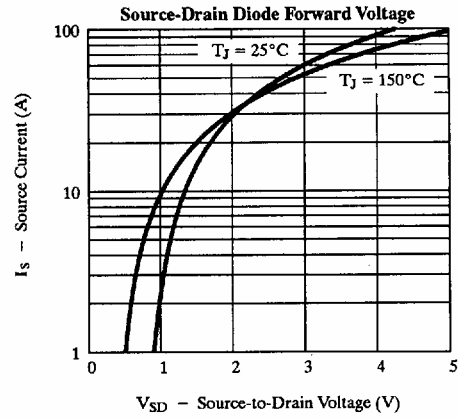
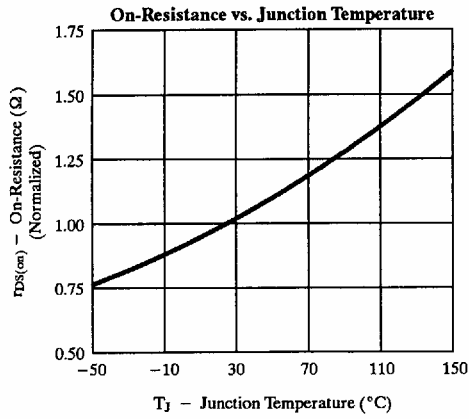
Notes:

- For design aid only; not subject to production testing.
- Pulse test; pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .
- Independent of operating temperature.

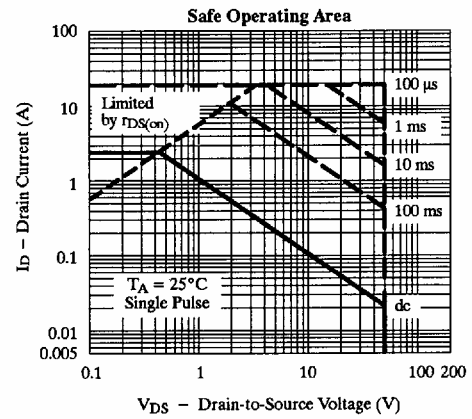
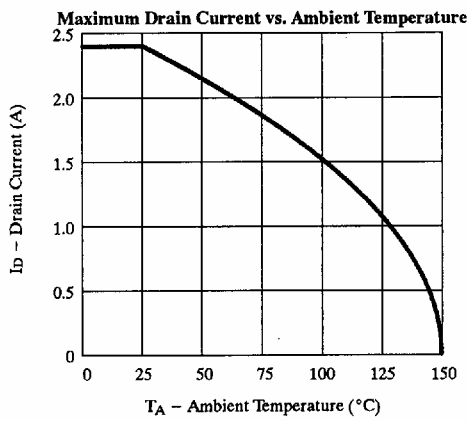
## Typical Characteristics (25°C Unless Otherwise Noted)



### Typical Characteristics (25°C Unless Otherwise Noted)



### Thermal Ratings



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