

SMPS MOSFET

IRFP32N50K

HEXFET® Power MOSFET

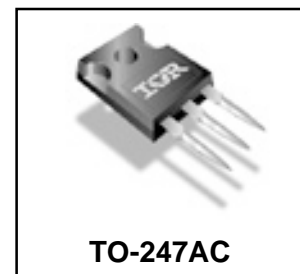
Applications

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

V_{DSS}	$R_{DS(on)}$ typ.	I_D
500V	0.135Ω	32A

Benefits

- Low Gate Charge Qg results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dv/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Low $R_{DS(on)}$



Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	32	A
I_D @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, V_{GS} @ 10V	20	
I_{DM}	Pulsed Drain Current ①	130	
P_D @ $T_C = 25^\circ\text{C}$	Power Dissipation	460	W
	Linear Derating Factor	3.7	W/°C
V_{GS}	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	13	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150	°C
	Soldering Temperature, for 10 seconds (1.6mm from case)	300	
	Mounting torque, 6-32 or M3 screw		

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	—	450	mJ
I_{AR}	Avalanche Current①	—	32	A
E_{AR}	Repetitive Avalanche Energy①	—	46	mJ

Thermal Resistance

Symbol	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.26	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	—	
$R_{\theta JA}$	Junction-to-Ambient	—	40	

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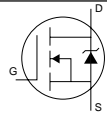
Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	500	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.54	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ④
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.135	0.16	Ω	$V_{GS} = 10V, I_D = 32A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	3.0	—	5.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	—	—	50	μA	$V_{DS} = 500V, V_{GS} = 0V$
		—	—	250	μA	$V_{DS} = 400V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 30V$
	Gate-to-Source Reverse Leakage	—	—	-100	nA	$V_{GS} = -30V$

Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	14	—	—	S	$V_{DS} = 50V, I_D = 32A$
Q_g	Total Gate Charge	—	—	190	nC	$I_D = 32A$ $V_{DS} = 400V$ $V_{GS} = 10V$ ④
Q_{gs}	Gate-to-Source Charge	—	—	59		
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	84		
$t_{d(on)}$	Turn-On Delay Time	—	28	—	ns	$V_{DD} = 250V$ $I_D = 32A$ $R_G = 4.3\Omega$ $V_{GS} = 10V$ ④
t_r	Rise Time	—	120	—		
$t_{d(off)}$	Turn-Off Delay Time	—	48	—		
t_f	Fall Time	—	54	—		
C_{iss}	Input Capacitance	—	5280	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$, See Fig. 5
C_{oss}	Output Capacitance	—	550	—		
C_{rss}	Reverse Transfer Capacitance	—	45	—		
C_{oss}	Output Capacitance	—	5630	—		
C_{oss}	Output Capacitance	—	155	—		
$C_{oss\ eff.}$	Effective Output Capacitance	—	265	—		

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	32	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	130		
V_{SD}	Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}, I_S = 32A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	530	800	ns	$T_J = 25^\circ\text{C}, I_F = 32A$
Q_{rr}	Reverse Recovery Charge	—	9.0	13.5	μC	$di/dt = 100A/\mu s$ ④
I_{RRM}	Reverse Recovery Current	—	30	—	A	
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting $T_J = 25^\circ\text{C}$, $L = 0.87\text{mH}$, $R_G = 25\Omega$, $I_{AS} = 32A$,
- ③ $I_{SD} \leq 32A$, $di/dt \leq 197A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.
- ⑤ $C_{oss\ eff.}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

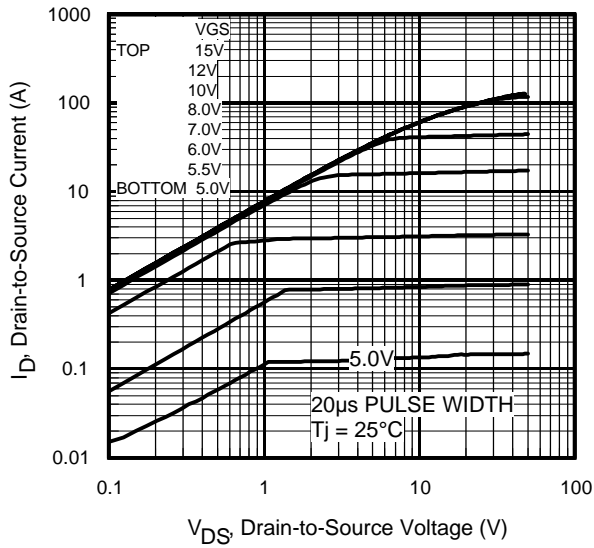


Fig 1. Typical Output Characteristics

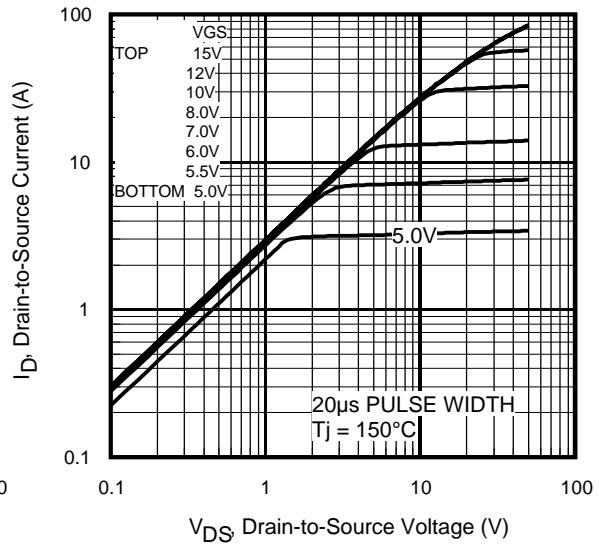


Fig 2. Typical Output Characteristics

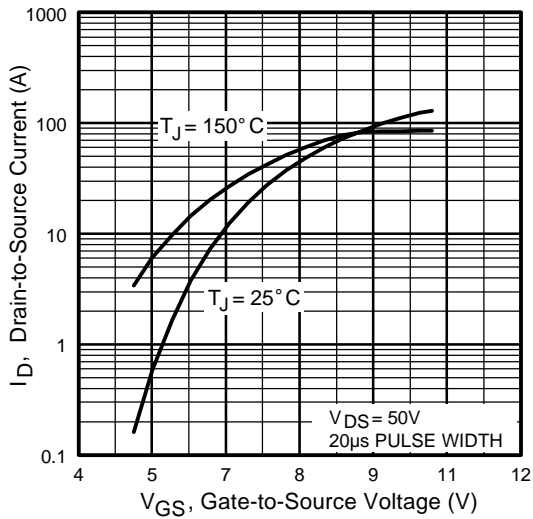


Fig 3. Typical Transfer Characteristics

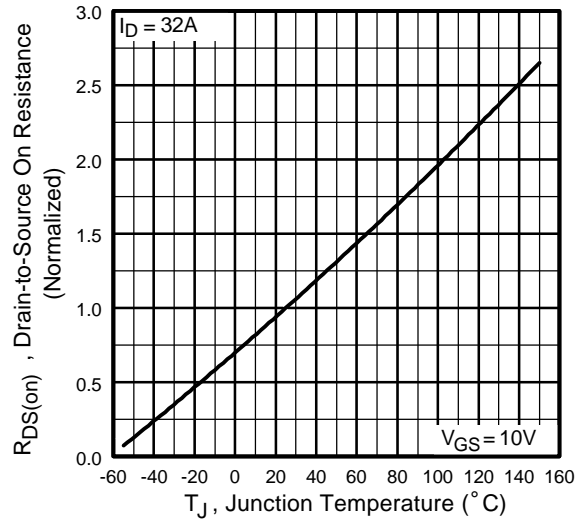


Fig 4. Normalized On-Resistance Vs. Temperature

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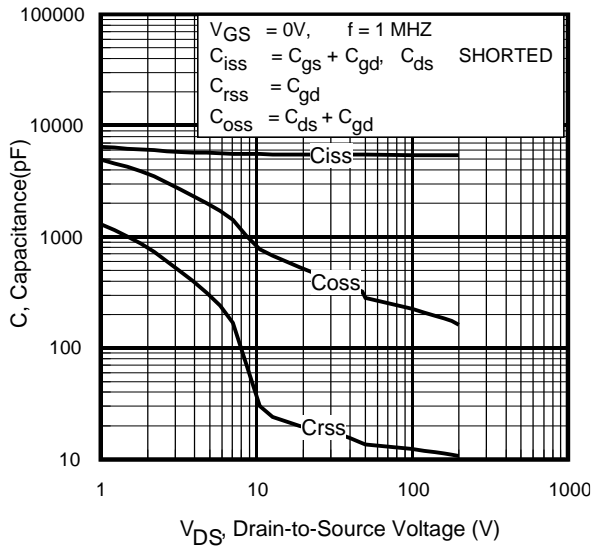


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

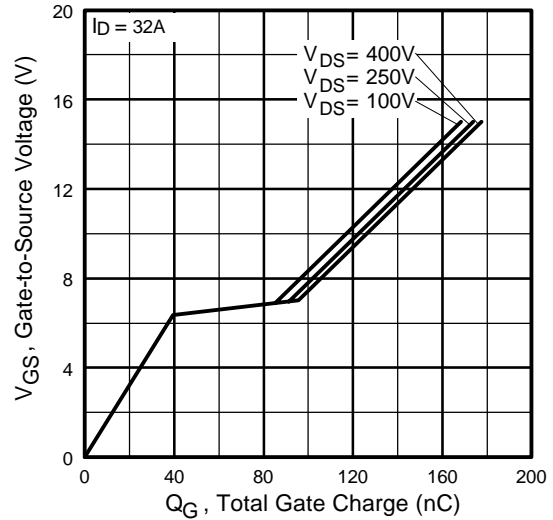


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

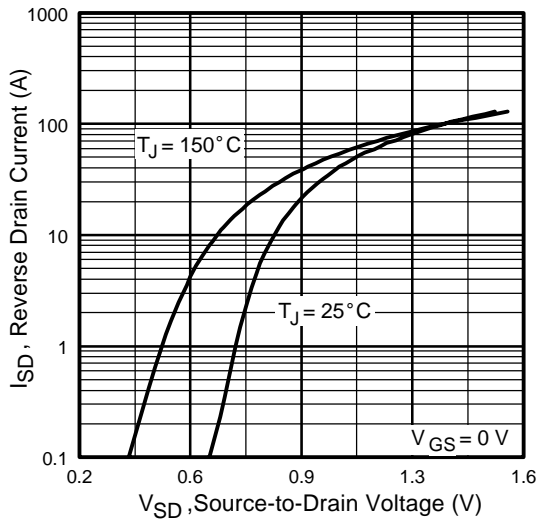


Fig 7. Typical Source-Drain Diode Forward Voltage

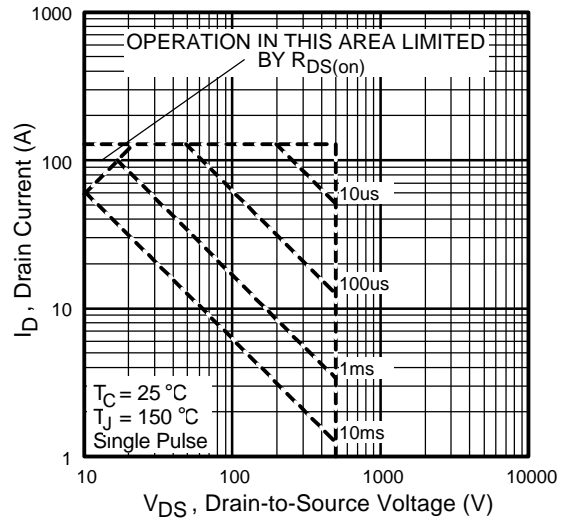


Fig 8. Maximum Safe Operating Area

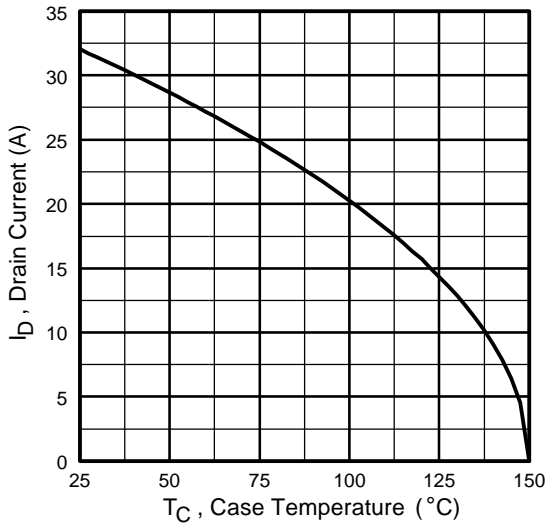


Fig 9. Maximum Drain Current Vs. Case Temperature

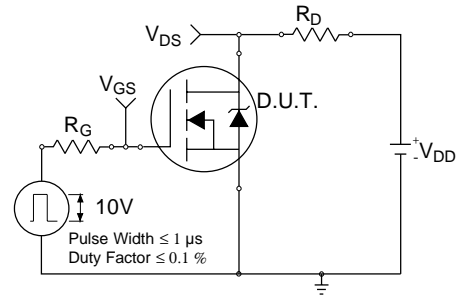


Fig 10a. Switching Time Test Circuit

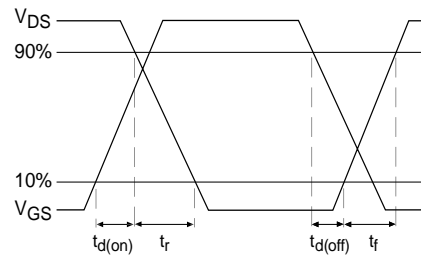


Fig 10b. Switching Time Waveforms

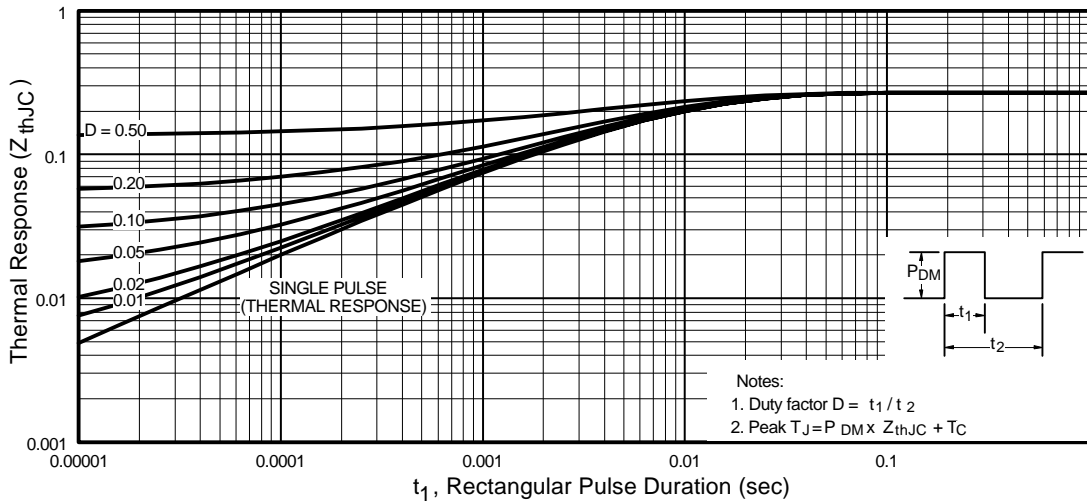


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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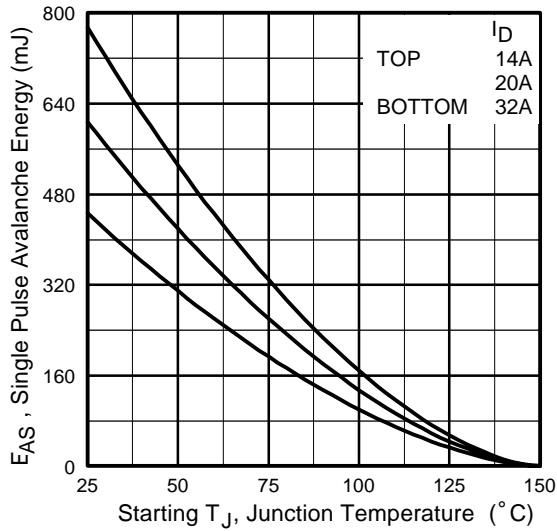


Fig 12a. Maximum Avalanche Energy Vs. Drain Current

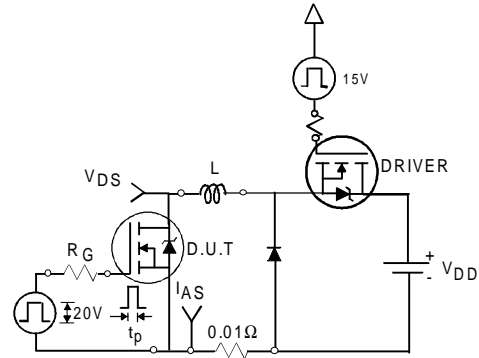


Fig 12c. Unclamped Inductive Test Circuit

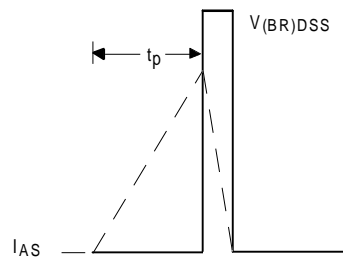


Fig 12d. Unclamped Inductive Waveforms

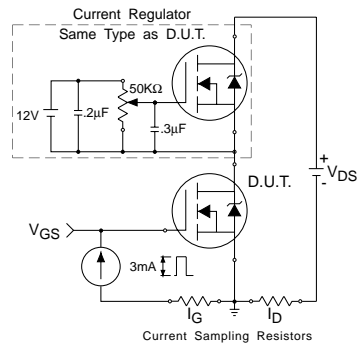


Fig 13a. Gate Charge Test Circuit

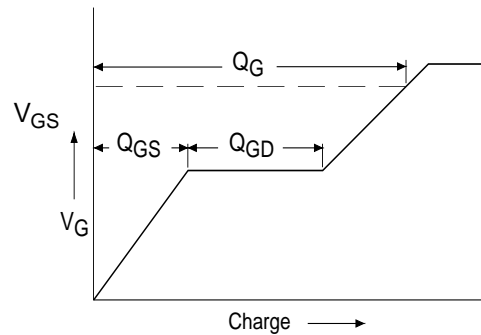
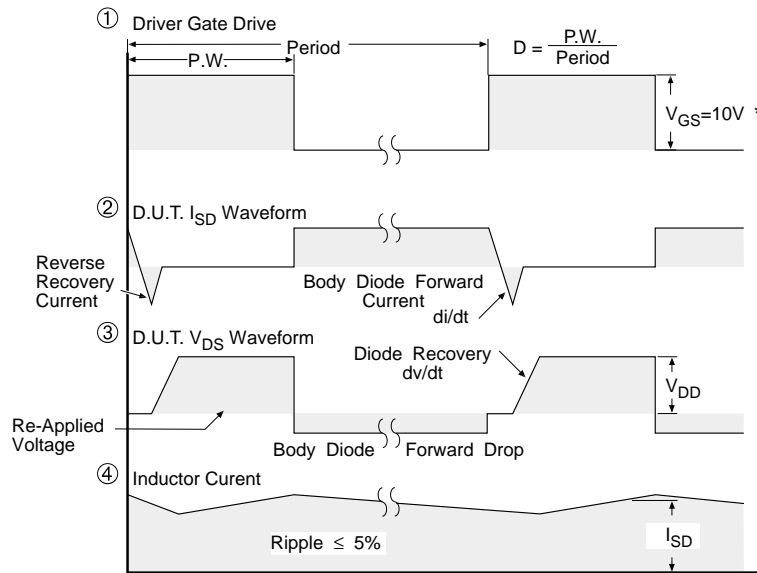
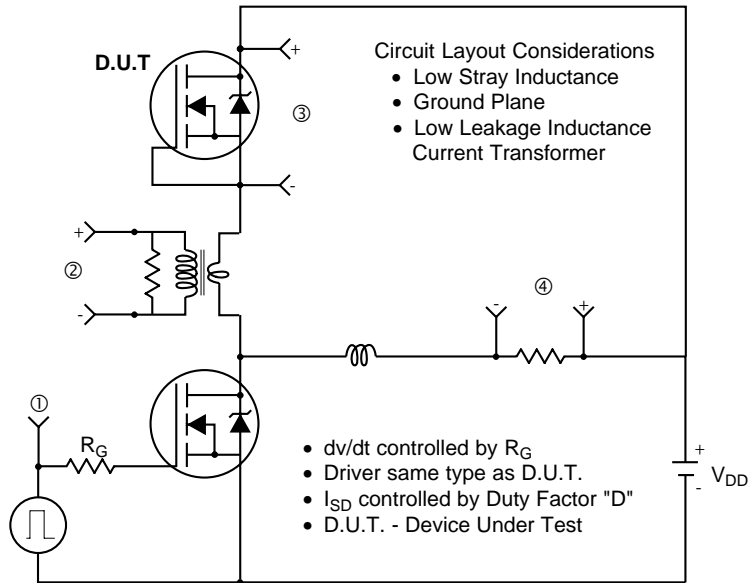


Fig 13b. Basic Gate Charge Waveform

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

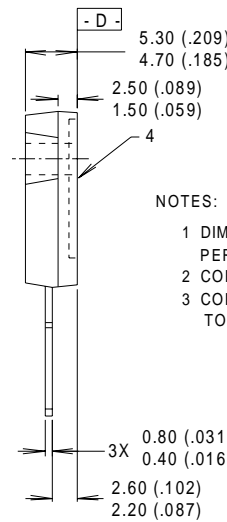
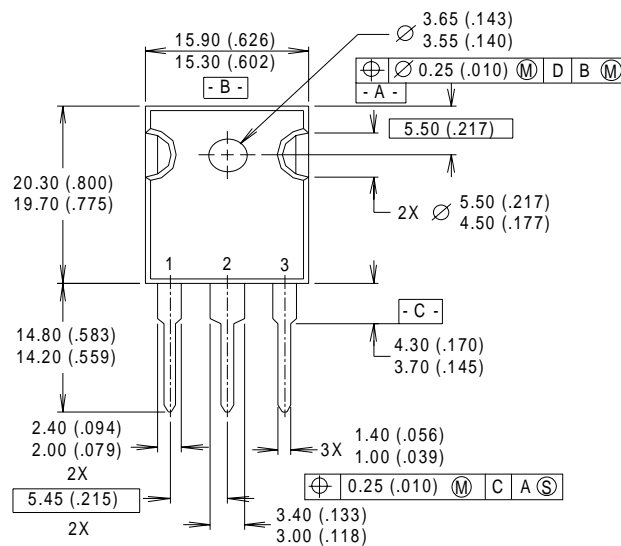
Fig 14. For N-Channel HEXFET® Power MOSFETs

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TO - 247 Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 2 CONTROLLING DIMENSION : INCH.
- 3 CONFORMS TO JEDEC OUTLINE TO-247-AC.

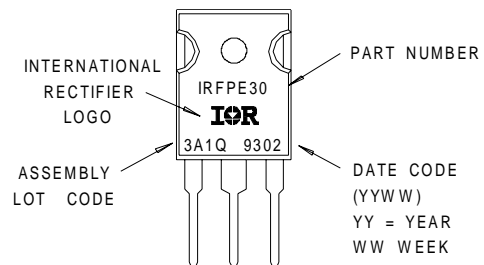
LEAD ASSIGNMENTS

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE
- 4 - DRAIN

Part Marking Information

TO-247AC

EXAMPLE : THIS IS AN IRFPE30 WITH ASSEMBLY LOT CODE 3A1Q



This product has been designed and qualified for the industrial market. Qualification Standards can be found on IR's Web site.

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