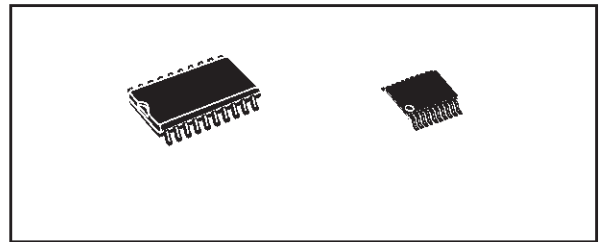




- HIGH SPEED: $t_{PD} = 5.0 \text{ ns}$ (TYP.) at $V_{CC} = 5V$
- LOW POWER DISSIPATION:
 $I_{CC} = 4 \mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8 \text{ mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC(OPR)} = 2V \text{ to } 5.5V$
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 573
- IMPROVED LATCH-UP IMMUNITY
- LOW NOISE: $V_{OLP} = 0.9V$ (MAX.)

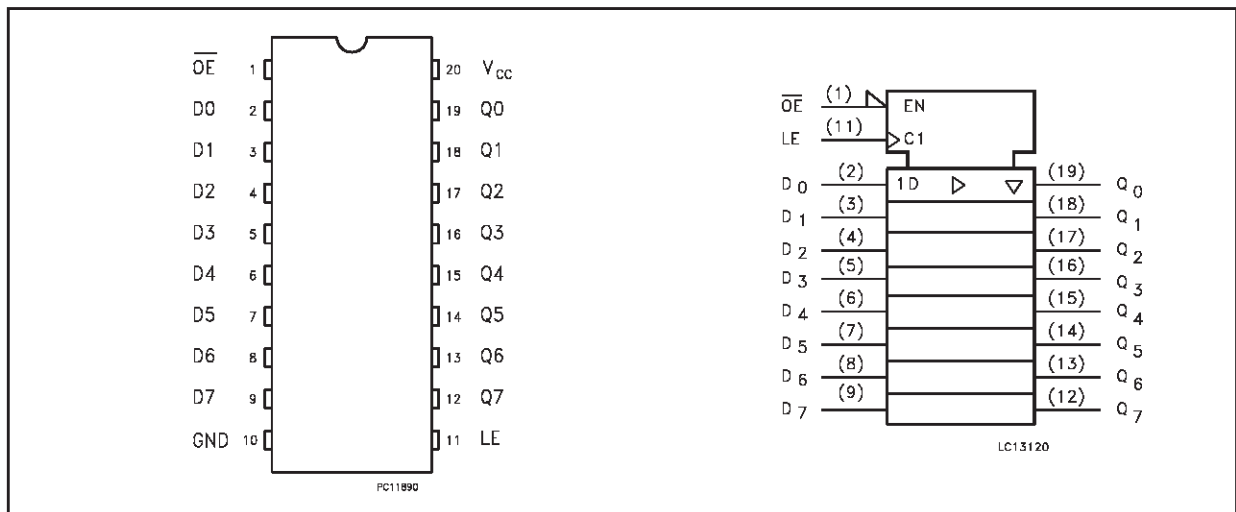


precisely at the logic level of D input data. While the (\overline{OE}) input is low, the 8 outputs will be in

DESCRIPTION

The 74VHC573 is an advanced high-speed CMOS OCTAL D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

These 8 bit D-Type latch are controlled by a latch enable input (LE) and an output enable input (\overline{OE}). While the LE inputs is held at a high level, the Q outputs will follow the data input precisely. When the LE is taken low, the Q outputs will be latched





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