

# Hermetically Sealed, Transistor Output Optocouplers for Analog and Digital Applications

## Technical Data

4N55\*  
 5962-87679 HCPL-655X  
 HCPL-553X 5962-90854  
 HCPL-653X HCPL-550X

\*See matrix for available extensions.

### Features

- Dual Marked with Device Part Number and DESC Drawing Number
- Manufactured and Tested on a MIL-PRF-38534 Certified Line
- QML-38534, Class H and K
- Five Hermetically Sealed Package Configurations
- Performance Guaranteed, Over -55°C to +125°C
- High Speed: Typically 400 kBit/s
- 9 MHz Bandwidth
- Open Collector Output
- 2-18 Volt  $V_{CC}$  Range
- 1500 Vdc Withstand Test Voltage
- High Radiation Immunity
- 6N135, 6N136, HCPL-2530/-2531, Function Compatibility
- Reliability Data

### Applications

- Military and Space
- High Reliability Systems
- Vehicle Command, Control, Life Critical Systems
- Line Receivers
- Switching Power Supply
- Voltage Level Shifting

- Analog Signal Ground Isolation (see Figures 7, 8, and 13)
- Isolated Input Line Receiver
- Isolated Output Line Driver
- Logic Ground Isolation
- Harsh Industrial Environments
- Isolation for Test Equipment Systems

### Description

These units are single, dual and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either standard product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DESC Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and are included in the DESC Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each channel contains a GaAsP light emitting diode which is optically coupled to an integrated photon detector. Separate connections for the photodiodes and output transistor collectors

improve the speed up to a hundred times that of a conventional phototransistor optocoupler by reducing the base-collector capacitance.

These devices are suitable for wide bandwidth analog applications, as well as for interfacing TTL to LSTTL or CMOS. Current Transfer Ratio (CTR) is 9% minimum at  $I_F = 16$  mA. The 18 V  $V_{CC}$

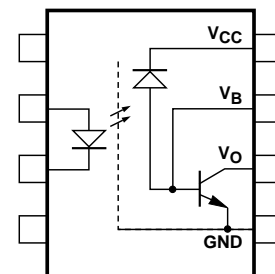
### Truth Table

(Positive Logic)

| Input   | Output |
|---------|--------|
| On (H)  | L      |
| Off (L) | H      |

### Functional Diagram

Multiple Channel Devices Available



*CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.*

capability will enable the designer to interface any TTL family to CMOS. The availability of the base lead allows optimized gain/bandwidth adjustment in analog applications. The shallow depth of the IC photodiode provides better radiation immunity than conventional phototransistor couplers.

These products are also available with the transistor base node connected to improve common mode noise immunity and ESD susceptibility. In addition, higher CTR minimums are available by special request.

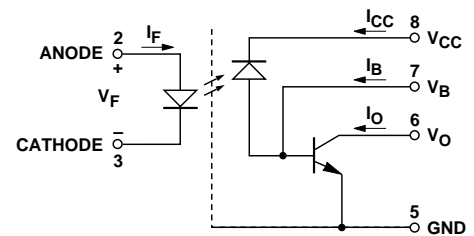
Package styles for these parts are 8 and 16 pin DIP through hole (case outlines P and E respectively), 16 pin DIP flat pack (case outline F), and leadless ceramic

chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options, see Selection Guide Table for details. Standard Military Drawing (SMD) parts are available for each package and lead style.

Because the same functional die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These

similarities give justification for the use of data obtained from one part to represent other part's performance for die related reliability and certain limited radiation test results.

### 8 Pin Ceramic DIP Single Channel Schematic



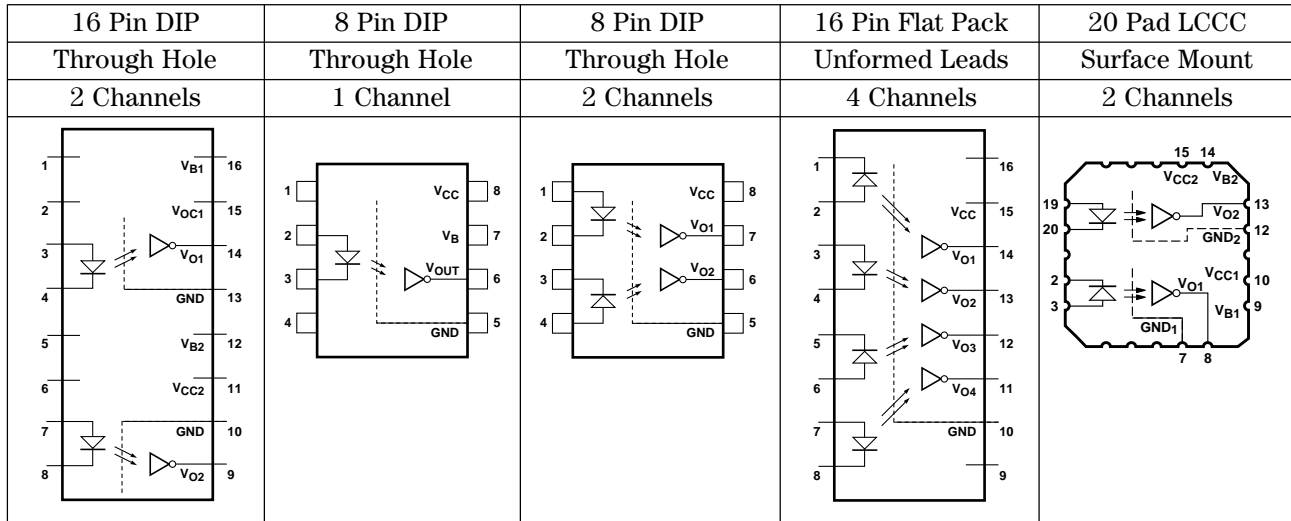
Note base pin 7.

## Selection Guide—Package Styles and Lead Configuration Options

| Package                        | 16 Pin DIP   | 8 Pin DIP    | 8 Pin DIP           | 16 Pin Flat Pack    | 20 Pad LCCC   |
|--------------------------------|--------------|--------------|---------------------|---------------------|---------------|
| Lead Style                     | Through Hole | Through Hole | Through Hole        | Unformed Leads      | Surface Mount |
| Channels                       | 2            | 1            | 2                   | 4                   | 2             |
| Common Channel Wiring          | None         | None         | V <sub>CC</sub> GND | V <sub>CC</sub> GND | None          |
| <b>HP Part # &amp; Options</b> |              |              |                     |                     |               |
| Commercial                     | 4N55*        | HCPL-5500    | HCPL-5530           | HCPL-6550           | HCPL-6530     |
| MIL-PRF-38534, Class H         | 4N55/883B    | HCPL-5501    | HCPL-5531           | HCPL-6551           | HCPL-6531     |
| MIL-PRF-38534, Class K         | HCPL-257K    | HCPL-550K    | HCPL-553K           | HCPL-655K           | HCPL-653K     |
| Standard Lead Finish           | Gold Plate   | Gold Plate   | Gold Plate          | Gold Plate          | Solder Pads   |
| Solder Dipped                  | Option #200  | Option #200  | Option #200         |                     |               |
| Butt Cut/Gold Plate            | Option #100  | Option #100  | Option #100         |                     |               |
| Gull Wing/Soldered             | Option #300  | Option #300  | Option #300         |                     |               |
| <b>SMD Part #</b>              |              |              |                     |                     |               |
| Prescript for all below        | 5962-        | 5962-        | 5962-               | 5962-               | 5962-         |
| Either Gold or Solder          | 8767901EX    | 9085401HPX   | 8767902PX           | 8767904FX           | 87679032X     |
| Gold Plate                     | 8767901EC    | 9085401HPC   | 8767902PC           | 8767904FC           |               |
| Solder Dipped                  | 8767901EA    | 9085401HPA   | 8767902PA           |                     | 87679032A     |
| Butt Cut/Gold Plate            | 8767901UC    | 9085401HYC   | 8767902YC           |                     |               |
| Butt Cut/Soldered              | 8767901UA    | 9085401HYA   | 8767902YA           |                     |               |
| Gull Wing/Soldered             | 8767901TA    | 9085401HXA   | 8767902XA           |                     |               |

\*JEDEC registered part.

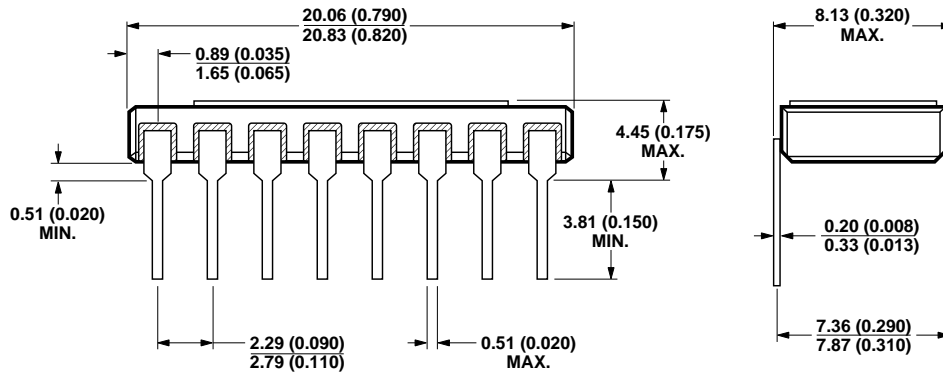
## Functional Diagrams



**Note:** 8 pin DIP and flat pack devices have common  $V_{CC}$  and ground. 16 pin DIP and LCCC (leadless ceramic chip carrier) packages have isolated channels with separate  $V_{CC}$  and ground connections.

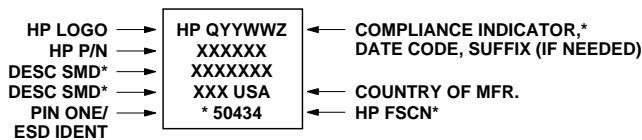
## Outline Drawings

16 Pin DIP Through Hole, 2 Channels



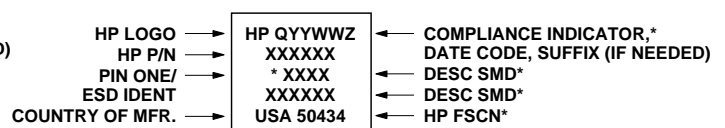
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

## Leaded Device Marking



\* QUALIFIED PARTS ONLY

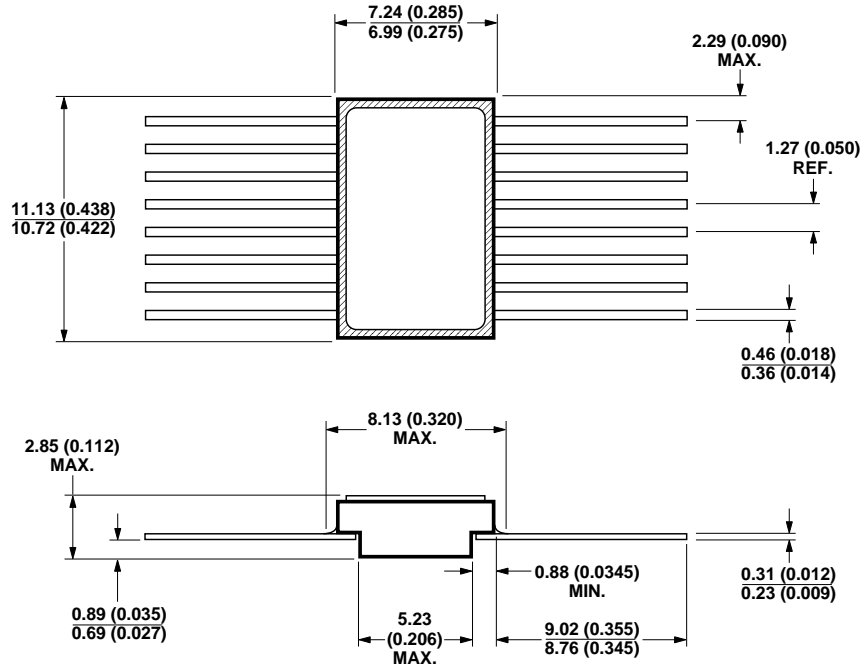
## Leadless Device Marking



\* QUALIFIED PARTS ONLY

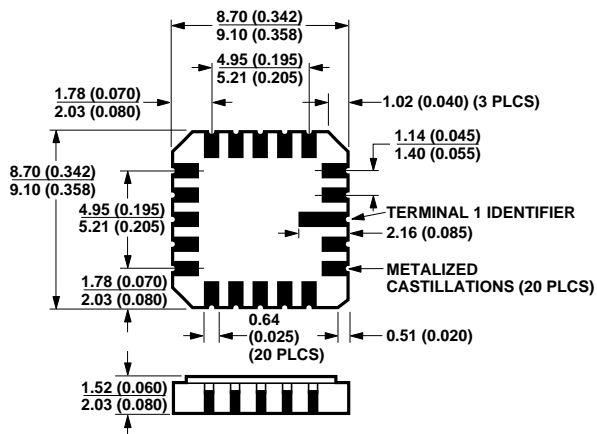
## Outline Drawings (contd.)

### 16 Pin Flat Pack, 4 Channels



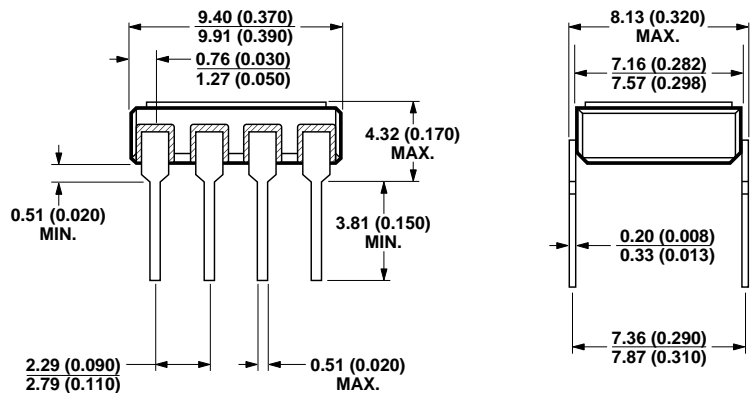
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

### 20 Terminal LCCC Surface Mount, 2 Channels



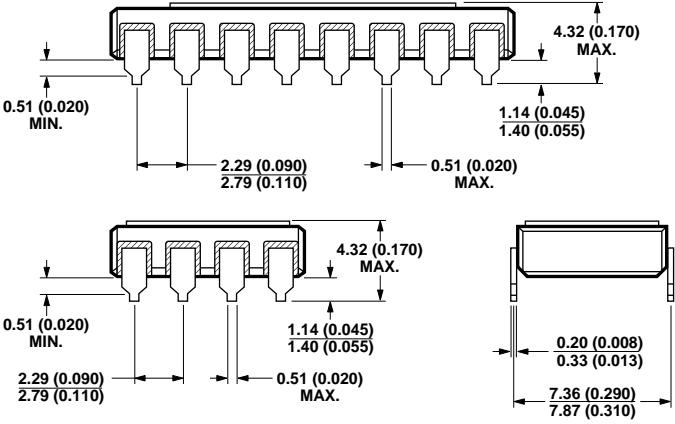
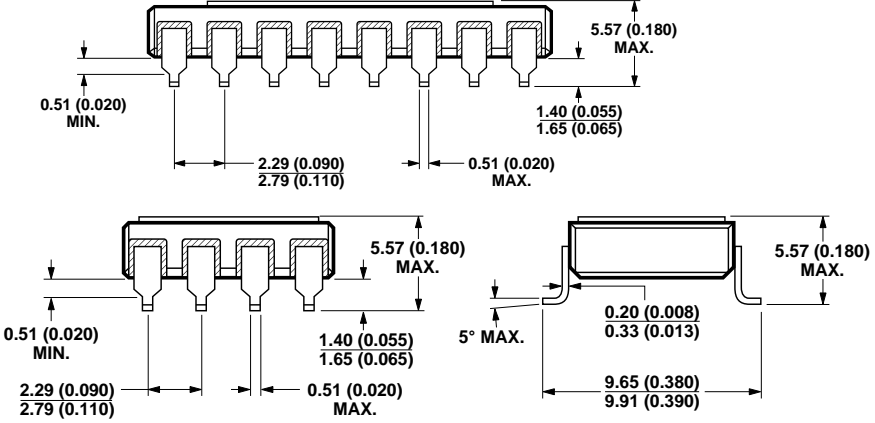
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).  
SOLDER THICKNESS 0.127 (0.005) MAX.

### 8 Pin DIP Through Hole, 1 and 2 Channel



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

## Hermetic Optocoupler Options

| Option | Description  |
|--------|--|
| 100    | <p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details).</p>  <p>NOTE: DIMENSIONS IN MILLIMETERS (INCHES).</p>  |
| 200    | <p>Lead finish is solder dipped rather than gold plated. This option is available on commercial and hi-rel product in 8 and 16 pin DIP. DESC drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.</p>  |
| 300    | <p>Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on commercial and hi-rel product in 8 and 16 pin DIP (see drawings below for details). This option has solder dipped leads.</p>  <p>NOTE: DIMENSIONS IN MILLIMETERS (INCHES).</p> |

## Absolute Maximum Ratings

(No derating required up to +125°C)

|  |                                |
|--|--------------------------------|
| Storage Temperature Range, $T_S$ .....   | -65°C to +150°C                |
| Operating Temperature, $T_A$ .....   | -55°C to +125°C                |
| Case Temperature, $T_C$ .....  | +170°C                         |
| Junction Temperature, $T_J$ .....  | +175°C                         |
| Lead Solder Temperature .....  | 260°C for 10 s                 |
| Peak Forward Input Current, (each channel,<br>≤ 1 ms duration), $I_{F PK}$ ..... | 40 mA                          |
| Average Input Forward Current, $I_{F AVG}$ (each channel) .....                  | 20 mA                          |
| Reverse Input Voltage, $BV_R$ .....  | See Electrical Characteristics |
| Average Output Current, $I_O$ (each channel) .....                               | 8 mA                           |
| Peak Output Current, $I_O$ (each channel) .....                                  | 16 mA                          |
| Supply Voltage, $V_{CC}$ .....   | -0.5 V to 20 V                 |
| Output Voltage, $V_O$ (each channel) .....                                       | -0.5 V to 20 V                 |
| Input Power Dissipation (each channel) .....                                     | 36 mW                          |
| Output Power Dissipation (each channel) .....                                    | 50 mW                          |
| Package Power Dissipation, $P_D$ (each channel) .....                            | 200 mW                         |

## Single Channel 8 Pin, Dual Channel 16 Pin, and LCCC Only

|   |       |
|---|-------|
| Emitter Base Reverse Voltage, $V_{EBO}$ ..... | 3.0 V |
| Base Current, $I_B$ (each channel) .....      | 5 mA  |

## ESD Classification

(MIL-STD-883, Method 3015)

4N55, 4N55/883B, HCPL-5500/01, and

HCPL-6530/31 .....

(Δ), Class 1

HCPL-5530/31, HCPL-6550/51 .....

(Dot), Class 3

## Recommended Operating Conditions

| Parameter                 | Symbol   | Min. | Max. | Units |
|---------------------------|----------|------|------|-------|
| Input Current, Low Level  | $I_{FL}$ |      | 250  | μA    |
| Input Current, High Level | $I_{FH}$ | 12   | 20   | mA    |
| Supply Voltage, Output    | $V_{CC}$ | 2    | 18   | V     |

**Electrical Characteristics** ( $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$ , unless otherwise specified)

| Parameter                                      | Symbol         | Test Conditions   | Group A <sup>[12]</sup><br>Sub-groups | Limits |  |            | Units         | Fig. | Note           |      |
|--|----------------|---|---------------------------------------|--------|--|------------|---------------|------|----------------|------|
|  |                |   |                                       | Min.   | Typ.**   | Max.       |               |      |                |      |
| Current Transfer Ratio                         | CTR*           | $V_O = 0.4\text{ V}$ , $I_F = 16\text{ mA}$ ,<br>$V_{CC} = 4.5\text{ V}$  | 1, 2, 3                               | 9      | 20   |            | %             | 2, 3 | 1, 2, 10       |      |
| Logic High Output Current                      | $I_{OH}$       | $I_F = 0$ ,<br>$I_{F(\text{other channels})} = 20\text{ mA}$ ,<br>$V_O = V_{CC} = 18\text{ V}$                      | 1, 2, 3                               |        | 5  | 100        | $\mu\text{A}$ | 4    | 1              |      |
| Output Leakage Current                         | $I_{OLeak}^*$  | $I_F = 250\text{ }\mu\text{A}$ ,<br>$I_{F(\text{other channels})} = 20\text{ mA}$ ,<br>$V_O = V_{CC} = 18\text{ V}$ | 1, 2, 3                               |        | 30   | 250        | $\mu\text{A}$ | 4    | 1              |      |
| Input-Output Insulation Leakage Current        | $I_{I-O}^*$    | $V_{I-O} = 1500\text{ Vdc}$ ,<br>RH = 45%<br>$T_A = 25^\circ\text{C}$ , $t = 5\text{ s}$                            | 1                                     |        |  | 1.0        | $\mu\text{A}$ |      | 3, 9           |      |
| Input Forward Voltage                          | $V_F^*$        | $I_F = 20\text{ mA}$  | 1, 2, 3                               |        | 1.55   | 1.8<br>1.9 | V             | 1    | 1, 14<br>1, 13 |      |
| Reverse Breakdown Voltage                      | $BV_R^*$       | $I_R = 10\text{ }\mu\text{A}$   | 1, 2, 3                               | 5<br>3 |  |            | V             |      | 1, 14<br>1, 13 |      |
| Logic High Supply Current                      | Single Channel | $I_{CCH}^*$<br>$V_{CC} = 18\text{ V}$ , $I_F = 0\text{ mA}$   | 1, 2, 3                               |        | 0.1  | 10         | $\mu\text{A}$ |      | 1              |      |
|  | Dual Channel   |   |                                       |        | 0.2  | 20         |               |      | 1, 4           |      |
|  | Quad Channel   |   |                                       |        | 0.4  | 40         |               |      | 1              |      |
| Logic Low Supply Current                       | Single Channel | $I_{CCL}^*$<br>$V_{CC} = 18\text{ V}$ , $I_F = 20\text{ mA}$  | 1, 2, 3                               |        | 35   | 200        | $\mu\text{A}$ | 5    | 1              |      |
|  | Dual Channel   |   |                                       |        | $V_{CC} = 18\text{ V}$ ,<br>$I_{F1} = I_{F2} = 20\text{ mA}$                     | 70         |               |      | 400            | 1, 4 |
|  | Quad Channel   |   |                                       |        | $V_{CC} = 18\text{ V}$ , $I_{F1} = I_{F2} =$<br>$I_{F3} = I_{F4} = 20\text{ mA}$ | 140        |               |      | 800            | 1    |
| Propagation Delay Time to Logic High at Output | $t_{PLH}^*$    | $R_L = 8.2\text{ k}\Omega$ ,<br>$C_L = 50\text{ pF}$ ,<br>$I_F = 16\text{ mA}$ ,<br>$V_{CC} = 5\text{ V}$           | 9, 10, 11                             |        | 1.0  | 6.0        | $\mu\text{s}$ | 6, 9 | 1, 6           |      |
| Propagation Delay Time to Logic Low at Output  | $t_{PHL}^*$    |   |                                       |        | 0.4  | 2.0        |               |      |                |      |

\*For JEDEC registered parts.

\*\*All typical values are at  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

### Typical Characteristics, $T_A = 25^\circ\text{C}$ , $V_{CC} = 5\text{ V}$

| Parameter   | Symbol                          | Typ.      | Units            | Test Conditions   | Fig. | Note  |
|---|---------------------------------|-----------|------------------|---|------|-------|
| Input Capacitance   | $C_{IN}$                        | 60        | pF               | $V_F = 0\text{ V}$ , $f = 1\text{ MHz}$   |      | 1     |
| Input Diode Temperature Coefficient                       | $\frac{\Delta V_F}{\Delta T_A}$ | -1.5      | mV/°C            | $I_F = 20\text{ mA}$  |      | 1     |
| Resistance (Input-Output)                                 | $R_{I-O}$                       | $10^{12}$ | $\Omega$         | $V_{I-O} = 500\text{ V}$  |      | 3     |
| Capacitance (Input-Output)                                | $C_{I-O}$                       | 1.0       | pF               | $f = 1\text{ MHz}$  |      | 1, 11 |
| Transistor DC Current Gain                                | $h_{FE}$                        | 250       | -                | $V_O = 5\text{ V}$ , $I_O = 3\text{ mA}$  |      | 1     |
| Small Signal Current Transfer Ratio                       | $\frac{\Delta I_O}{\Delta I_F}$ | 21        | %                | $V_{CC} = 5\text{ V}$ , $V_O = 2\text{ V}$  | 7    | 1     |
| Common Mode Transient Immunity at Logic High Level Output | $ CM_H $                        | 1000      | V/ $\mu\text{s}$ | $I_F = 0\text{ mA}$ , $R_L = 8.2\text{ k}\Omega$ ,<br>$V_O(\text{min}) = 2.0\text{ V}$<br>$V_{CM} = 10\text{ V}_{P-P}$  | 10   | 1, 7  |
| Common Mode Transient Immunity at Logic Low Level Output  | $ CM_L $                        | -1000     | V/ $\mu\text{s}$ | $I_F = 16\text{ mA}$ , $R_L = 8.2\text{ k}\Omega$ ,<br>$V_O(\text{max}) = 0.8\text{ V}$<br>$V_{CM} = 10\text{ V}_{P-P}$ | 10   | 1, 7  |
| Bandwidth   | BW                              | 9         | MHz              |   | 8    | 8     |

### Multi-Channel Product Only

|  |           |           |          |  |  |      |
|--|-----------|-----------|----------|--|--|------|
| Input-Input Insulation Leakage Current | $I_{I-I}$ | 1         | pA       | Relative Humidity = 45%<br>$V_{I-I} = 500\text{ V}$ , $t = 5\text{ s}$ |  | 5, 9 |
| Resistance (Input-Input)               | $R_{I-I}$ | $10^{12}$ | $\Omega$ | $V_{I-I} = 500\text{ V}$   |  | 5    |
| Capacitance (Input-Input)              | $C_{I-I}$ | 0.8       | pF       | $f = 1\text{ MHz}$   |  | 5    |

### Notes:

- Each channel of a multi-channel device.
- Current Transfer Ratio is defined as the ratio of output collector current,  $I_O$ , to the forward LED input current,  $I_F$ , times 100%. CTR is known to degrade slightly over the unit's lifetime as a function of input current, temperature, signal duty cycle, and system on time. Refer to Application Note 1002 for more detail. In short, it is recommended that designers allow at least 20-25% guardband for CTR degradation.
- All devices are considered two-terminal devices; measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
- The 4N55, 4N55/883B, HCPL-6530 and HCPL-6531 dual channel parts function as two independent single channel units. Use the single channel parameter limits.  $I_F = 0\text{ mA}$  for channel under test and  $I_F = 20\text{ mA}$  for other channels.
- Measured between adjacent input pairs shorted together for each multichannel device.
- $t_{PHL}$  propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The  $t_{PLH}$  propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
- $CM_L$  is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ( $V_O < 0.8\text{ V}$ ).  $CM_H$  is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ( $V_O > 2.0\text{ V}$ ).
- Bandwidth is the frequency at which the ac output voltage is 3 dB below the low frequency asymptote. For the HCPL-5530 the typical bandwidth is 2 MHz.
- This is a momentary withstand test, not an operating condition.
- Higher CTR minimums are available to support special applications.
- Measured between each input pair shorted together and all output connections for that channel shorted together.
- Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25, 125, and -55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
- Not required for 4N55, 4N55/883B and 5962-8767901 types.
- Required for 4N55, 4N55/883B and 5962-8767901 types only.

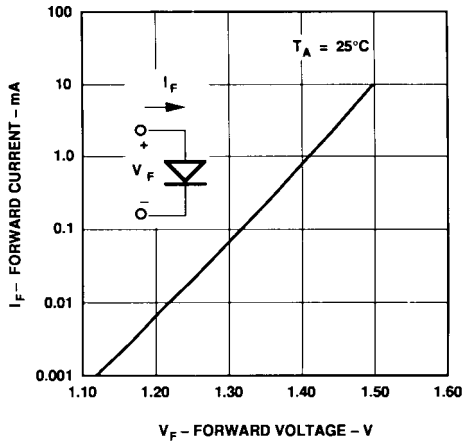


Figure 1. Input Diode Forward Current vs. Forward Voltage.

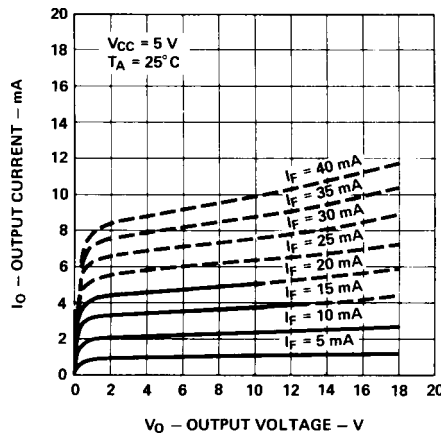


Figure 2. DC and Pulsed Transfer Characteristic.

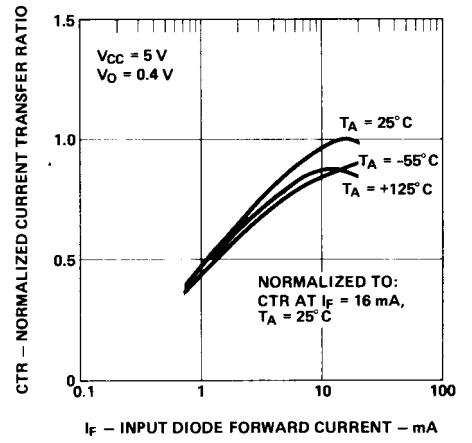


Figure 3. Normalized Current Transfer Ratio vs. Input Diode Forward Current.

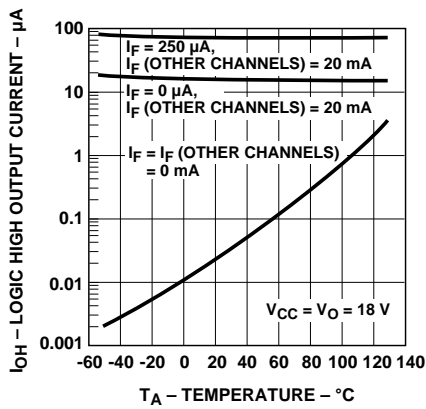


Figure 4. Logic High Output Current vs. Temperature.

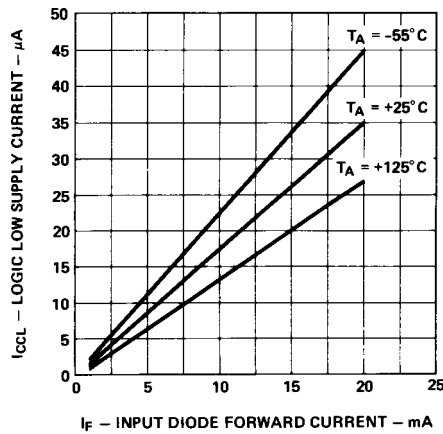


Figure 5. Logic Low Supply Current vs. Input Diode Forward Current.

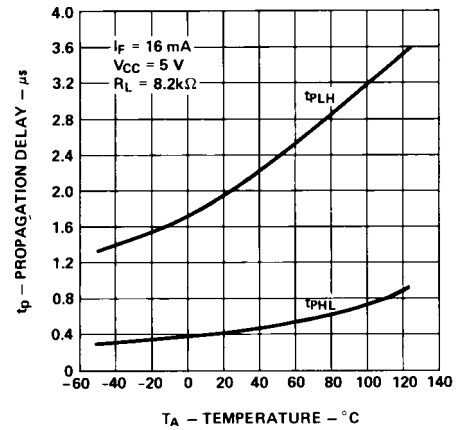


Figure 6. Propagation Delay vs. Temperature.

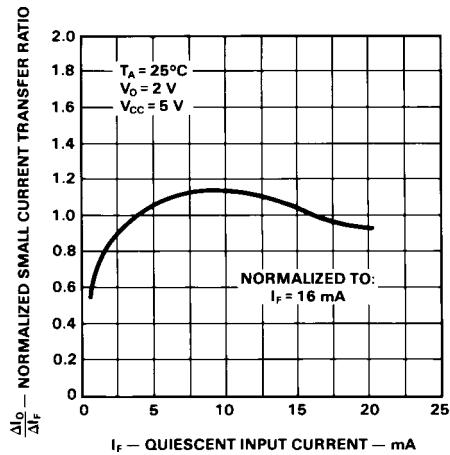


Figure 7. Normalized Small Signal Current Transfer Ratio vs. Quiescent Input Current.

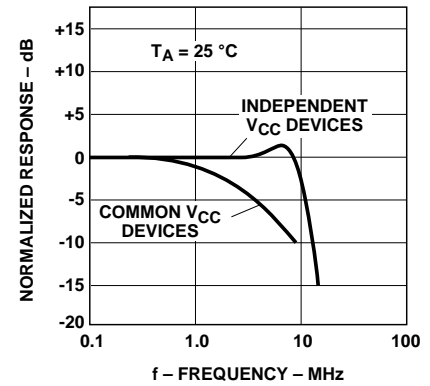
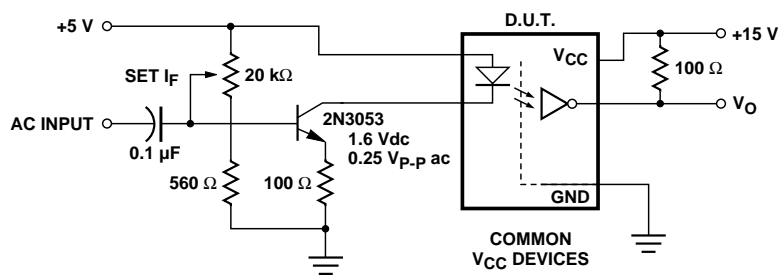
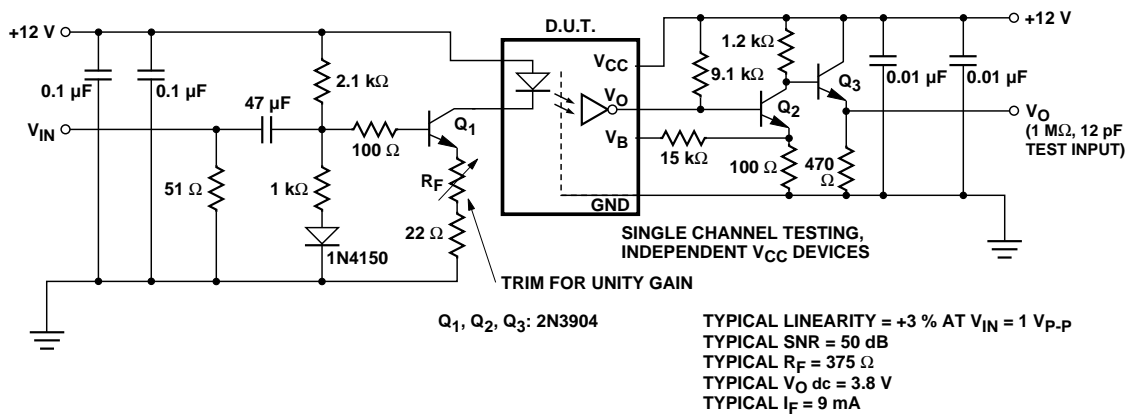


Figure 8. Frequency Response.

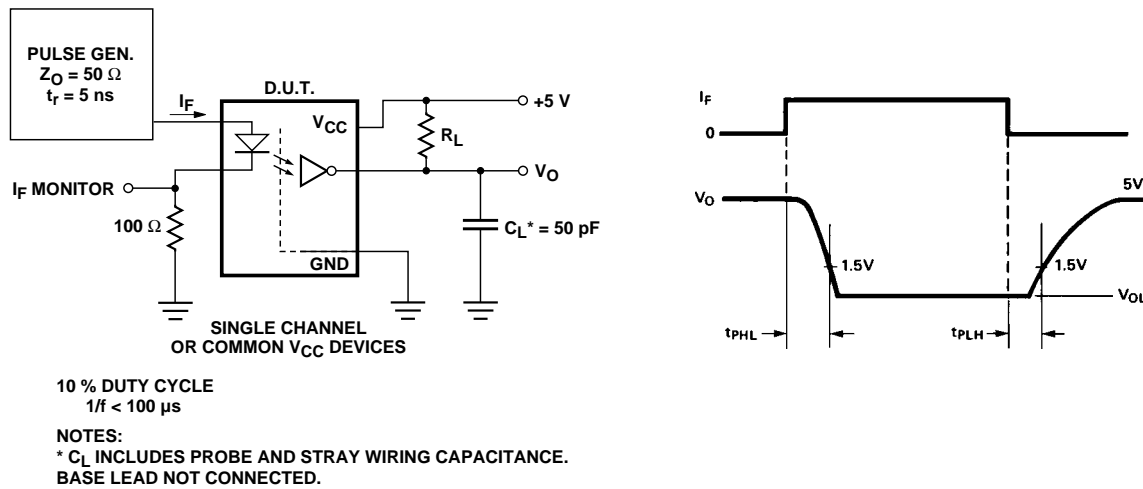
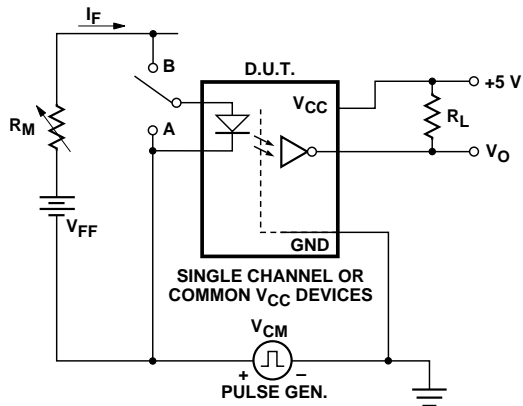


Figure 9. Switching Test Circuit.\*

\*JEDEC Registered Data.



NOTE: BASE LEAD NOT CONNECTED.

Figure 10. Test Circuit for Transient Immunity and Typical Waveforms.

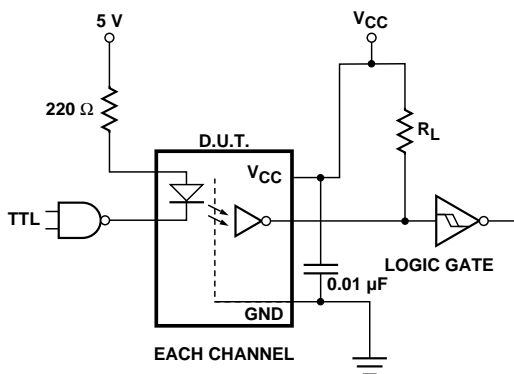
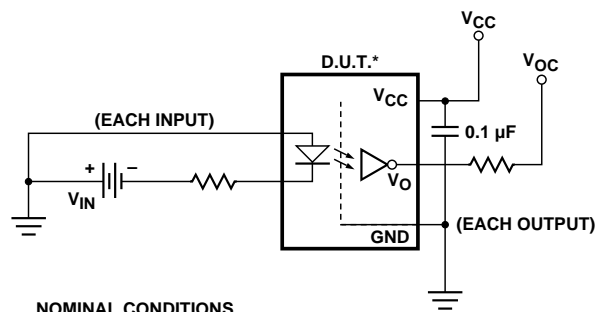


Figure 11. Recommended Logic Interface.

| Logic Family                | LSTTL  | CMOS      |       |
|-----------------------------|--------|-----------|-------|
| Device No.                  | 54LS14 | CD40106BM |       |
| V <sub>CC</sub>             | 5 V    | 5 V       | 15 V  |
| R <sub>L</sub> 5% Tolerance | 18 kΩ* | 8.2 kΩ    | 22 kΩ |

\*The equivalent output load resistance is affected by the LSTTL input current and is approximately 8.2 kΩ.

This is a worst case design which takes into account 25% degradation of CTR. See App. Note 1002 to assess actual degradation and lifetime.



NOMINAL CONDITIONS  
 PER CHANNEL:  $I_F = 20 \text{ mA}$   
 $I_O = 4 \text{ mA}$   
 $I_{CC} = 30 \mu\text{A}$

NOTE: BASE LEAD NOT CONNECTED.

$T_A = +125^\circ\text{C}$

Figure 12. Operating Circuit for Burn-In and Steady State Life Tests. All Channels Tested Simultaneously.

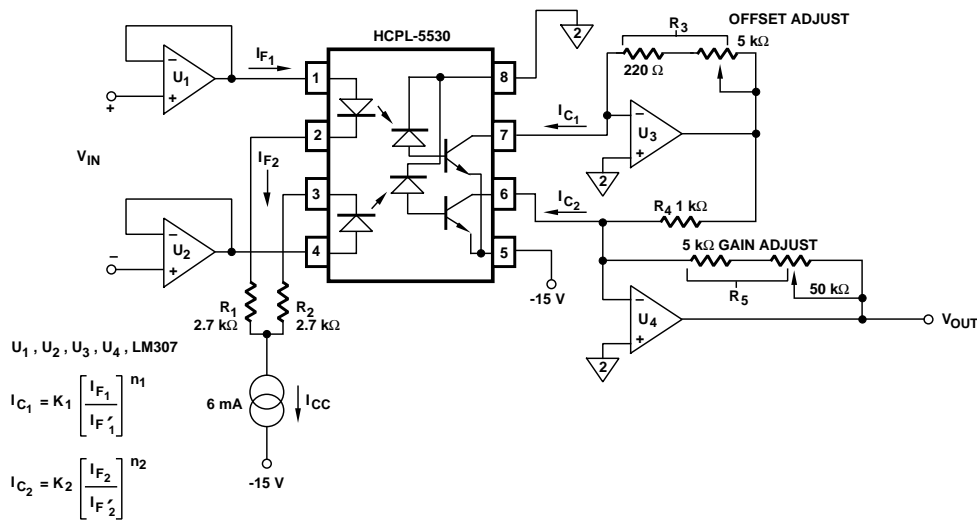


Figure 13. Isolation Amplifier Application Circuit.

### Description

The schematic uses a dual-channel, high-speed optocoupler (HCPL-5530) to function as a servo type dc isolation amplifier. This circuit operates on the principle that two optocouplers will track each other if their gain changes by the same amount over a specific operating region.

### Performance of Circuit

- 1% linearity for 10 V peak-to-peak dynamic range
- Gain drift: -0.03%/°C
- Offset Drift:  $\pm 1$  mV/°C
- 25 kHz bandwidth (limited by Op-Amps U1, U2)

### MIL-PRF-38534 Class H, Class K, and DESC SMD Test Program

Hewlett-Packard's Hi-Rel Optocouplers are in compliance with MIL-PRF-38534 Classes H and K. Class H devices are also in compliance with DESC drawings 5962-87679, and 5962-90854.

Testing consists of 100% screening and quality conformance inspection to MIL-PRF-38534.



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