

FSB50450S

Motion SPM® 5 FRFET® Series

Features

- 500 V $R_{DS(on)}$ = 2.4 Ω (Max) FRFET MOSFET 3-Phase Inverter Including HVICs
- Three Separate Negative DC-Link Terminals for Inverter Current Sensing Applications
- HVIC for Gate Driving and Undervoltage Protection
- Active-High Interface, Can Work With 3.3 V / 5 V Logic
- Optimized for Low Electromagnetic Interference
- Isolation Voltage Rating of 1500 Vrms for 1 min.
- Surface Mounted Device Package
- Moisture Sensitive Level (MSL) 3

Applications

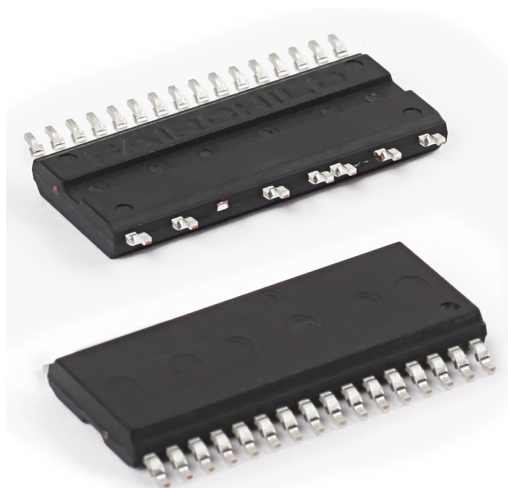
- 3-Phase Inverter Driver for Small Power AC Motor Drives

General Description

FSB50450S is a Motion SPM5 Series Based on Fast-Recovery MOSFET(FRFET) Technology as a Compact Inverter Solution for Small Power Motor Drive Applications Such as Fans and Pumps. It is Composed of Six FRFET MOSFETs and Three Half-Bridge Gate Drive HVICs. FSB50450S Provides Low Electromagnetic Interference(EMI) Characteristics with Optimizing Switching Speed. Moreover, Since It Employs MOSFETs as Power Switches, It has Greater Ruggedness and a Larger Safe Operating Area(SOA) than IGBT-Based Power Modules. The Package is Optimized for Thermal Performance and Compactness for use in Applications Where Space is Limited. FSB50450S is the Right Solution for Inverters Requiring Energy Efficiency, Compactness, and Low Electromagnetic Interference.

Related Source

- [AN9042 : Motion SPM5 Series Ver.1 User's Guide](#)
- [AN-9082 : Motion SPM5 Series Thermal Performance by Contact Pressure](#)



Package Marking & Ordering Information

Device Marking	Device	Package	Reel Size	Packing Type	Quantity
FSB50450S	FSB50450S	SPM5D-023	330mm	TAPE & REEL	450

Absolute Maximum Ratings

Inverter Part (Each MOSFET® Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Unit
V_{PN}	DC Link Input Voltage, Drain-Source Voltage of Each MOSFET		500	V
$*I_{D\ 25}$	Each MOSFET Drain Current, Continuous	$T_C = 25^\circ\text{C}$	1.5	A
$*I_{D\ 80}$	Each MOSFET Drain Current, Continuous	$T_C = 80^\circ\text{C}$	1.1	A
$*I_{DP}$	Each MOSFET Drain Current, Peak	$T_C = 25^\circ\text{C}$, $PW < 100\ \mu\text{s}$	3.0	A
$*I_{DRMS}$	Each MOSFET Drain Current, Rms	$T_C = 80^\circ\text{C}$, $F_{PWM} < 20\text{KHz}$	0.8	A_{RMS}
$*P_D$	Maximum Power Dissipation	$T_C = 25^\circ\text{C}$, For Each MOSFET	10	W

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Unit
V_{CC}	Control Supply Voltage	Applied Between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied Between V_B and V_S	20	V
V_{IN}	Input Signal Voltage	Applied Between IN and COM	$-0.3 \sim V_{CC}+0.3$	V

Thermal Resistance

Symbol	Parameter	Conditions	Rating	Unit
$R_{\theta JC}$	Junction to Case Thermal Resistance	Each MOSFET under Inverter Operating Condition (Note 1)	8.9	$^\circ\text{C/W}$

Total System

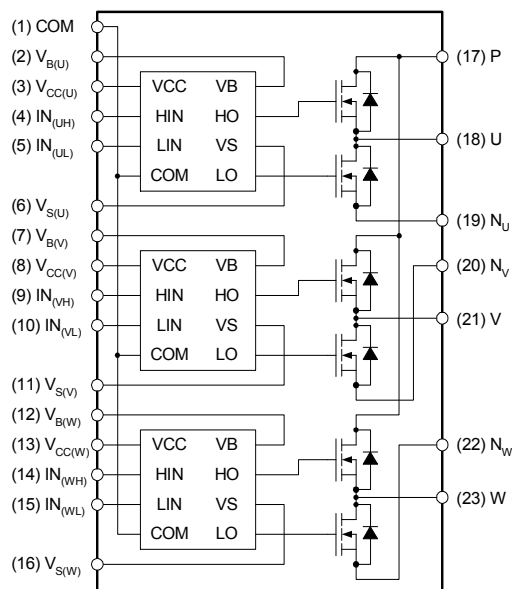
Symbol	Parameter	Conditions	Rating	Unit
T_J	Operating Junction Temperature		$-40 \sim 150$	$^\circ\text{C}$
T_{STG}	Storage Temperature		$-50 \sim 150$	$^\circ\text{C}$
V_{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1 minute, Connection Pins to Heatsink	1500	V_{rms}

Note:

- For the Measurement Point of Case Temperature T_C , Please refer to Figure 4.
- Marking " * " Is Calculation Value or Design Factor.

Pin descriptions

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side MOSFET® Driving
3	$V_{CC(U)}$	Bias Voltage for U Phase IC and Low Side MOSFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-Side
5	$IN_{(UL)}$	Signal Input for U Phase Low-Side
6	$V_{S(U)}$	Bias Voltage Ground for U Phase High Side MOSFET Driving
7	$V_{B(V)}$	Bias Voltage for V Phase High Side MOSFET Driving
8	$V_{CC(V)}$	Bias Voltage for V Phase IC and Low Side MOSFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-Side
10	$IN_{(VL)}$	Signal Input for V Phase Low-Side
11	$V_{S(V)}$	Bias Voltage Ground for V Phase High Side MOSFET Driving
12	$V_{B(W)}$	Bias Voltage for W Phase High Side MOSFET Driving
13	$V_{CC(W)}$	Bias Voltage for W Phase IC and Low Side MOSFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase High-Side
15	$IN_{(WL)}$	Signal Input for W Phase Low-Side
16	$V_{S(W)}$	Bias Voltage Ground for W Phase High Side MOSFET Driving
17	P	Positive DC-Link Input
18	U	Output for U Phase
19	N_U	Negative DC-Link Input for U Phase
20	N_V	Negative DC-Link Input for V Phase
21	V	Output for V Phase
22	N_W	Negative DC-Link Input for W Phase
23	W	Output for W Phase



Note:

Source Terminal of Each Low-Side MOSFET is Not Connected to Supply Ground or Bias Voltage Ground Inside Motion SPM®.

External Connections Should be Made as Indicated in Figure 3

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

Electrical Characteristics ($T_J = 25^\circ\text{C}$, $V_{CC}=V_{BS}= 15\text{ V}$ Unless Otherwise Specified)**Inverter Part** (Each MOSFET® Unless Otherwise Specified)

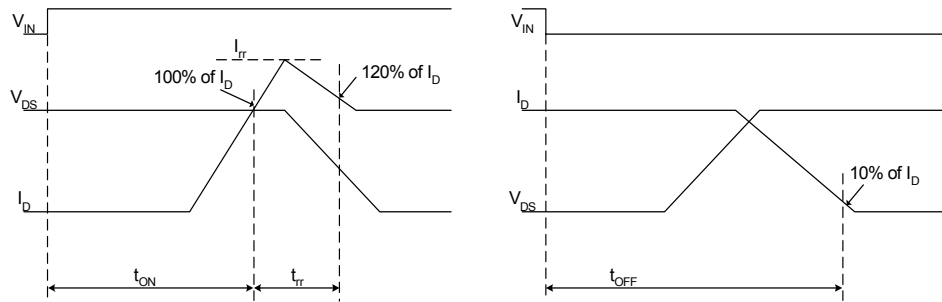
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{IN}=0\text{ V}$, $I_D = 250\mu\text{A}$ (Note 1)	500	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.53	-	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{IN}=0\text{ V}$, $V_{DS} = 500\text{ V}$	-	-	250	μA
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{CC} = V_{BS} = 15\text{ V}$, $V_{IN} = 5\text{ V}$, $I_D = 0.5\text{ A}$	-	1.9	2.4	Ω
V_{SD}	Drain-Source Diode Forward Voltage	$V_{CC} = V_{BS} = 15\text{ V}$, $V_{IN} = 0\text{ V}$, $I_D = -0.5\text{ A}$	-	-	1.2	V
t_{ON}	Switching Times	$V_{PN} = 300\text{ V}$, $V_{CC} = V_{BS} = 15\text{ V}$, $I_D = 0.5\text{ A}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$, Inductive Load $L = 3\text{ mH}$ High- and Low-Side MOSFET Switching (Note 2)	-	1152	-	ns
t_{OFF}			-	600	-	ns
t_{rr}			-	185	-	ns
E_{ON}			-	85	-	μJ
E_{OFF}			-	11	-	μJ
RBSOA	Reverse-Bias Safe Operating Area	$V_{PN} = 400\text{ V}$, $V_{CC} = V_{BS} = 15\text{ V}$, $I_D = I_{DP}$, $V_{DS}=BV_{DSS}$, $T_J = 150^\circ\text{C}$ High- and Low-Side MOSFET Switching (Note 3)	Full Square			

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{QCC}	Quiescent V_{CC} Current	$V_{CC}=15\text{ V}$, $V_{IN}=0\text{ V}$ Applied Between V_{CC} and COM	-	-	160	μA
I_{QBS}	Quiescent V_{BS} Current	$V_{BS}=15\text{ V}$, $V_{IN}=0\text{ V}$ Applied Between $V_{B(U)}-U$, $V_{B(V)}-V$, $V_{B(W)}-W$	-	-	100	μA
UV_{CCD}	Low-Side Undervoltage Protection (Figure 6)	V_{CC} Undervoltage Protection Detection Level	7.4	8.0	9.4	V
UV_{CCR}		V_{CC} Undervoltage Protection Reset Level	8.0	8.9	9.8	V
UV_{BSD}	High-Side Undervoltage Protection (Figure 7)	V_{BS} Undervoltage Protection Detection Level	7.4	8.0	9.4	V
UV_{BSR}		V_{BS} Undervoltage Protection Reset Level	8.0	8.9	9.8	V
V_{IH}	ON Threshold Voltage	Logic High Level	3.0	-	-	V
V_{IL}	OFF Threshold Voltage	Logic Low Level				
I_{IH}	Input Bias Current	$V_{IN} = 5\text{ V}$	-	10	20	μA
I_{IL}		$V_{IN} = 0\text{ V}$	-	-	2	μA

Note:

- BV_{DSS} is the Absolute Maximum Voltage Rating Between Drain and Source Terminal of Each MOSFET Inside Motion SPM®. V_{PN} Should be Sufficiently Less Than This Value Considering the Effect of the Stray Inductance so that V_{DS} Should Not Exceed BV_{DSS} in Any Case.
- t_{ON} and t_{OFF} Include the Propagation Delay Time of the Internal Drive IC. Listed Values are Measured at the Laboratory Test Condition, and They Can be Different According to the Field Applications Due to the Effect of Different Printed Circuit Boards and Wirings. Please see Figure 4 for the Switching Time Definition with the Switching Test Circuit of Figure 5.
- The peak current and voltage of each MOSFET during the switching operation should be included in the safe operating area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.



(a) Turn-on (b) Turn-off
Figure 4. Switching Time Definitions

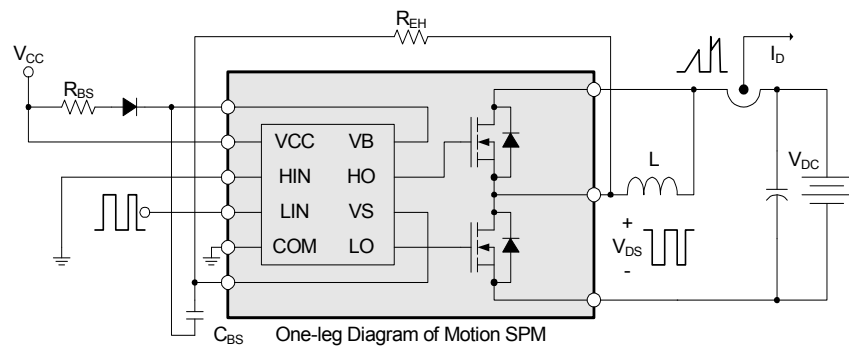


Figure 5. Switching and RBSOA (Single-pulse) Test Circuit (Low-side)

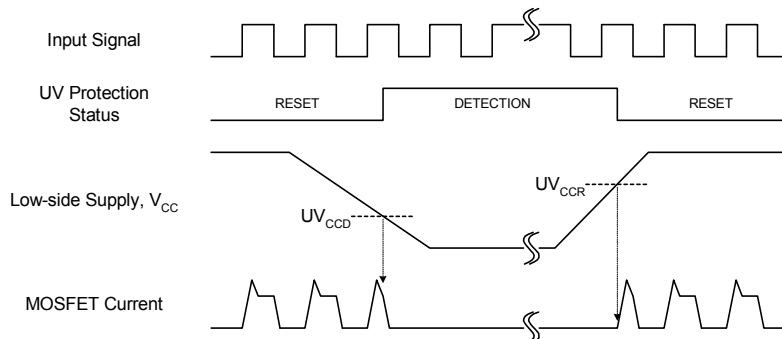


Figure 6. Undervoltage Protection (Low-side)

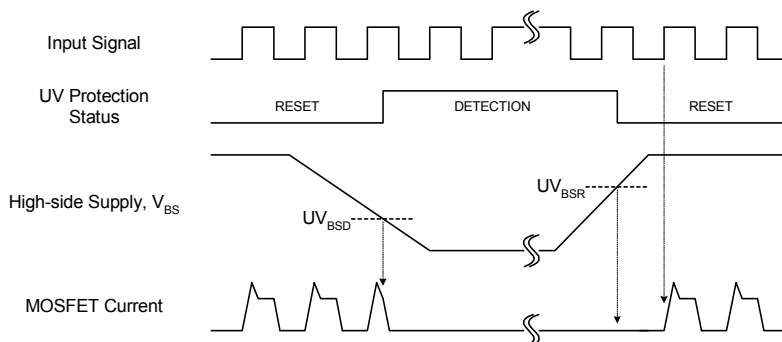
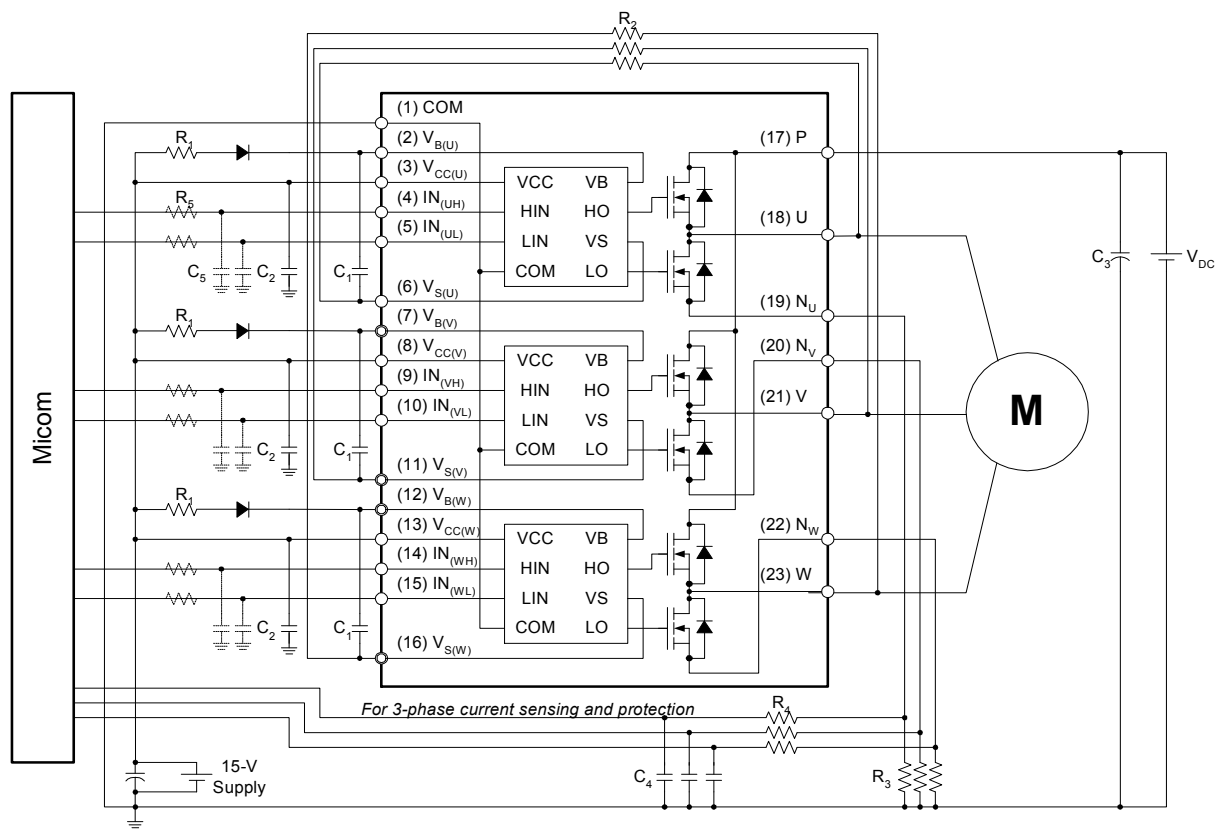


Figure 7. Undervoltage Protection (High-side)

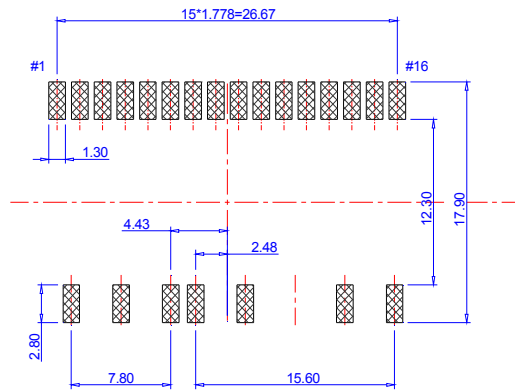
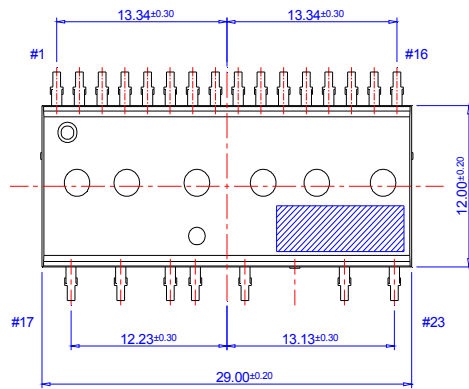
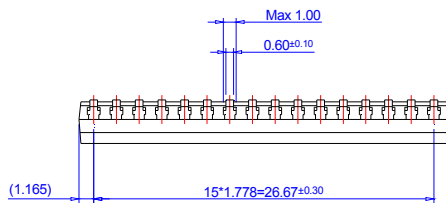


Note:

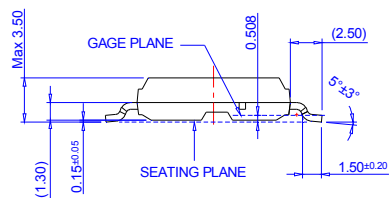
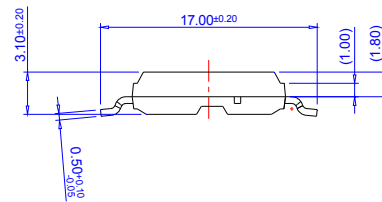
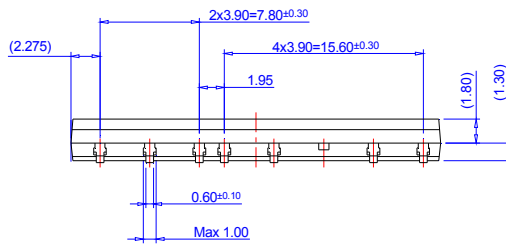
1. About Pin Position, Refer to Figure 1.
2. RC Coupling (R_5 and C_5 , R_4 and C_4) at Each Input of Motion SPM® and Micom are Useful to Prevent Improper Input Signal Caused by Surge Noise.
3. The voltage Drop Across R_3 Affects the Low Side Switching Performance and the Bootstrap Characteristics Since it is Placed Between COM and the Source Terminal of the Low Side MOSFET. For this Reason, the Voltage Drop Across R_3 Should Be Less Than 1 V in the Steady-State.
4. Ground Wires and Output Terminals, Should Be Thick and Short in Order to Avoid Surge Voltage and Malfunction of HVIC.
5. All the Filter Capacitors Should Be Connected Close to Motion SPM, and They Should Have Good Characteristics for Rejecting High-Frequency Ripple Current.

Figure 8. Example of Application Circuit

Detailed Package Outline Drawings



LAND PATTERN RECOMMENDATIONS





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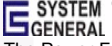
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