

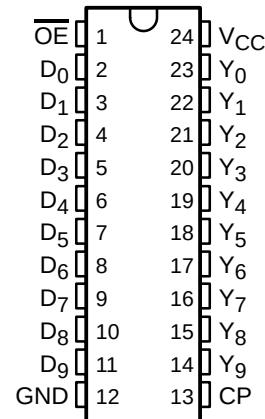
CY74FCT821T

10-BIT BUS-INTERFACE REGISTER WITH 3-STATE OUTPUTS

SCCS033B—MAY 1994—REVISED NOVEMBER 2001

- Function, Pinout, and Drive Compatible With FCT, F Logic, and AM29821
- Reduced V_{OH} (Typically = 3.3 V) Version of Equivalent FCT Functions
- Edge-Rate Control Circuitry for Significantly Improved Noise Characteristics
- I_{off} Supports Partial-Power-Down Mode Operation
- Matched Rise and Fall Times
- Fully Compatible With TTL Input and Output Logic Levels
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- 64-mA Output Sink Current
32-mA Output Source Current
- High-Speed Parallel Register With Positive-Edge-Triggered D-Type Flip-Flops
- 3-State Outputs

P, Q, OR SO PACKAGE
(TOP VIEW)



description

This bus-interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider address/data paths or buses carrying parity. The CY74FCT821T is a 10-bit-wide buffered version of the popular CY74FCT374 function. This device is ideal for use as an output port requiring high I_{OL}/I_{OH} .

This device is designed for high-capacitance load drive capability, while providing low-capacitance bus loading at both inputs and outputs. Outputs are designed for low-capacitance bus loading in the high-impedance state.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
D	I	D flip-flop data inputs
CP	O	Clock pulse for the register. Enters data into the register on the low-to-high clock transition.
Y	O	Register 3-state outputs
$\overline{OE}$	I	Output control. When $\overline{OE}$ is high, the Y outputs are in the high-impedance state. When $\overline{OE}$ is low, true register data is present at the Y outputs.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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CY74FCT821T

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WITH 3-STATE OUTPUTS

SCCS033B– MAY 1994 – REVISED NOVEMBER 2001

ORDERING INFORMATION

T _A	PACKAGE†		SPEED (ns)	ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	QSOP – Q	Tape and reel	6	CY74FCT821CTQCT	FCT821C
	SOIC – SO	Tube	6	CY74FCT821CTSOC	FCT821C
		Tape and reel	6	CY74FCT821CTSOCT	
	DIP – P	Tube	7.5	CY74FCT821BTPC	CY74FCT821BTPC
	SOIC – SO	Tube	7.5	CY74FCT821BTSOC	FCT821B
		Tape and reel	7.5	CY74FCT821BTSOCT	
	QSOP – Q	Tape and reel	10	CY74FCT821ATQCT	FCT821A
	SOIC – SO	Tube	10	CY74FCT821ATSOC	FCT821A
		Tape and reel	10	CY74FCT821ATSOCT	

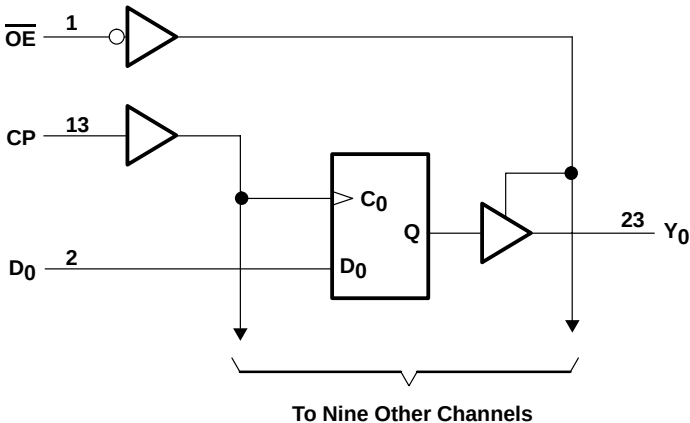
† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS			INTERNAL OUTPUTS		FUNCTION
$\overline{OE}$	D	CP	Q	Y	
H	X	↑	L	Z	Z
H	L	↑	L	Z	Load
H	H	↑	H	Z	
L	L	↑	L	L	
L	H	↑	H	H	

H = High logic level, L = Low logic level, X = Don't care,
↑ = Low-to-high transition, Z = High-impedance state

logic diagram (positive logic)



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SCCS033B— MAY 1994 — REVISED NOVEMBER 2001

absolute maximum rating over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range to ground potential	–0.5 V to 7 V
DC input voltage range	–0.5 V to 7 V
DC output voltage range	–0.5 V to 7 V
DC output current (maximum sink current/pin)	120 mA
Package thermal impedance, θ_{JA} (see Note 1): P package	67°C/W
(see Note 2): Q package	61°C/W
(see Note 2): SO package	46°C/W
Ambient temperature range with power applied, T_A	–65°C to 135°C
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	2			V
V_{IL} Low-level input voltage			0.8	V
I_{OH} High-level output current			–32	mA
I_{OL} Low-level output current			64	mA
T_A Operating free-air temperature	–40		85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation.

CY74FCT821T

10-BIT BUS-INTERFACE REGISTER

WITH 3-STATE OUTPUTS

SCCS033B—MAY 1994 – REVISED NOVEMBER 2001

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	V _{CC} = 4.75 V,	I _{IN} = −18 mA		−0.7	−1.2	V
V _{OH}	V _{CC} = 4.75 V	I _{OH} = −32 mA	2		V	
		I _{OH} = −15 mA	2.4	3.3		
V _{OL}	V _{CC} = 4.75 V,	I _{OL} = 64 mA		0.3	0.55	V
V _{hys}	All inputs			0.2		V
I _I	V _{CC} = 5.25 V,	V _{IN} = V _{CC}			5	μA
I _{IH}	V _{CC} = 5.25 V,	V _{IN} = 2.7 V			±1	μA
I _{IL}	V _{CC} = 5.25 V,	V _{IN} = 0.5 V			±1	μA
I _{OZH}	V _{CC} = 5.25 V,	V _{OUT} = 2.7 V			10	μA
I _{OZL}	V _{CC} = 5.25 V,	V _{OUT} = 0.5 V			−10	μA
I _{OS} ‡	V _{CC} = 5.25 V,	V _{OUT} = 0 V	−60	−120	−225	mA
I _{off}	V _{CC} = 0 V,	V _{OUT} = 4.5 V			±1	μA
I _{CC}	V _{CC} = 5.25 V,	V _{IN} ≤ 0.2 V, V _{IN} ≥ V _{CC} − 0.2 V		0.1	0.2	mA
ΔI _{CC}	V _{CC} = 5.25 V, V _{IN} = 3.4 V [§] , f ₁ = 0, Outputs open			0.5	2	mA
I _{CCD} ¶	V _{CC} = 5.25 V, One bit switching at 50% duty cycle, Outputs open, OE = EN = GND, V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V			0.06	0.12	mA/MHz
I _C [#]	V _{CC} = 5.25 V, Outputs open, OE = EN = GND	One bit switching at f ₁ = 5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V	0.7	1.4	mA
			V _{IN} = 3.4 V or GND	1.2	3.4	
		Eight bits switching at f ₁ = 2.5 MHz at 50% duty cycle	V _{IN} ≤ 0.2 V or V _{IN} ≥ V _{CC} − 0.2 V	1.6	3.2	
			V _{IN} = 3.4 V or GND	3.9	12.2	
C _i				5	10	pF
C _o				9	12	pF

[†] Typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample-and-hold techniques are preferable to minimize internal chip heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output can raise the chip temperature well above normal and cause invalid readings in other parametric tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

[§] Per TTL-driven input ($V_{IN} = 3.4 \text{ V}$); all other inputs at V_{CC} or GND

^{\P} This parameter is derived for use in total power-supply calculations.

^{\#} $I_C = I_{CC} + \Delta I_{CC} \times D_H \times N_T + I_{CCD} (f_0/2 + f_1 \times N_1)$

Where:

I_C = Total supply current

I_{CC} = Power-supply current with CMOS input levels

ΔI_{CC} = Power-supply current for a TTL high input ($V_{IN} = 3.4 \text{ V}$)

D_H = Duty cycle for TTL inputs high

N_T = Number of TTL inputs at D_H

I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)

f_0 = Clock frequency for registered devices, otherwise zero

f_1 = Input signal frequency

N_1 = Number of inputs changing at f_1

All currents are in milliamperes and all frequencies are in megahertz.

|| Values for these conditions are examples of the I_{CC} formula.



CY74FCT821T
10-BIT BUS-INTERFACE REGISTER
WITH 3-STATE OUTPUTS

SCCS033B— MAY 1994 – REVISED NOVEMBER 2001

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER			TEST LOAD	CY74FCT821AT		CY74FCT821BT		CY74FCT821CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_W	Pulse duration	CP	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	7		6		6		ns
t_{su}	Setup time, before $CP \uparrow$	Data	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	4		3		3		ns
t_h	Hold time, after $CP \uparrow$	Data	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$	2		1.5		1.5		ns

switching characteristics over operating free-air temperature range (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST LOAD	CY74FCT821AT		CY74FCT821BT		CY74FCT821CT		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	CP	Y	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$		10		7.5		6	ns
t_{PHL}					10		7.5		6	
t_{PLH}	CP	Y	$C_L = 300 \text{ pF}$, $R_L = 500 \Omega$		20		15		12.5	ns
t_{PHL}					20		15		12.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$		12		8		7	ns
t_{PZL}					12		8		7	
t_{PZH}	$\overline{OE}$	Y	$C_L = 300 \text{ pF}$, $R_L = 500 \Omega$		23		15		12.5	ns
t_{PZL}					23		15		12.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 5 \text{ pF}$, $R_L = 500 \Omega$		7		6.5		6	ns
t_{PLZ}					7		6.5		6	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50 \text{ pF}$, $R_L = 500 \Omega$		8		7.5		6.5	ns
t_{PLZ}					8		7.5		6.5	

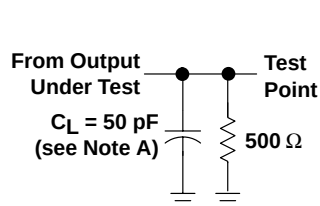
CY74FCT821T

10-BIT BUS-INTERFACE REGISTER

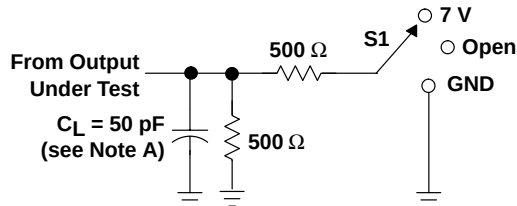
WITH 3-STATE OUTPUTS

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PARAMETER MEASUREMENT INFORMATION

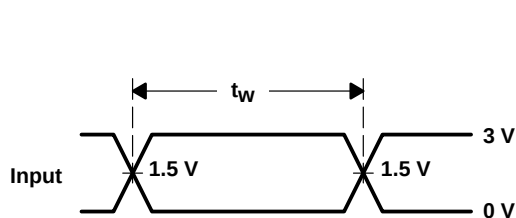


LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

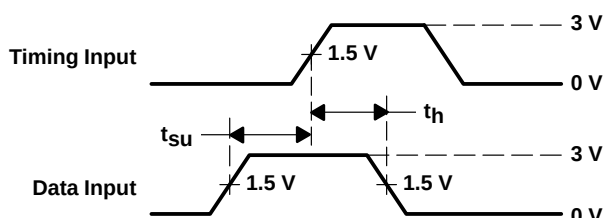


LOAD CIRCUIT FOR
3-STATE OUTPUTS

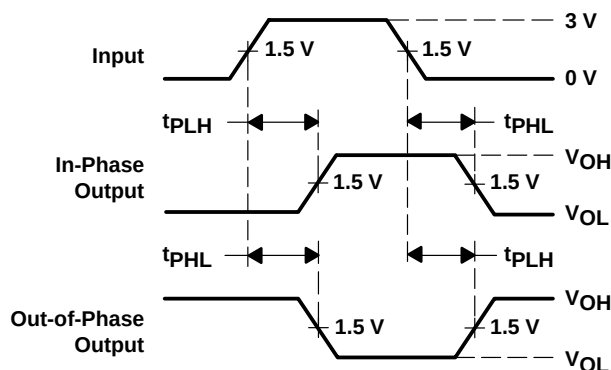
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	Open



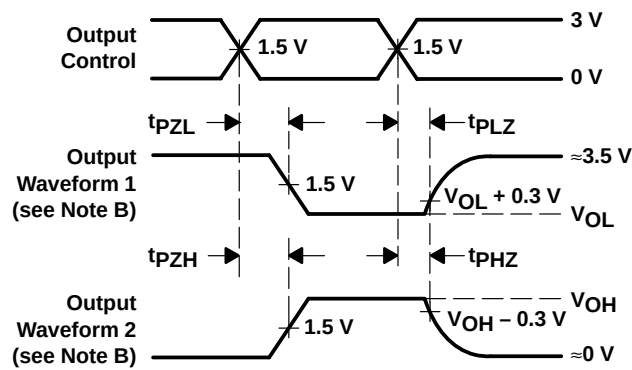
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CY74FCT821ATQCT	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT821ATSOC	ACTIVE	SOIC	DW	24	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT821ATSOCT	ACTIVE	SOIC	DW	24	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT821BTPC	ACTIVE	PDIP	NT	24	15	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
CY74FCT821BTSOC	ACTIVE	SOIC	DW	24	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT821BTSOCT	ACTIVE	SOIC	DW	24	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT821CTQCT	ACTIVE	SSOP/ QSOP	DBQ	24	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-260C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT821CTSOC	ACTIVE	SOIC	DW	24	25	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CY74FCT821CTSOCT	ACTIVE	SOIC	DW	24	2000	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - May not be currently available - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

None: Not yet available Lead (Pb-Free).

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Green (RoHS & no Sb/Br): TI defines "Green" to mean "Pb-Free" and in addition, uses package materials that do not contain halogens, including bromine (Br) or antimony (Sb) above 0.1% of total product weight.

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

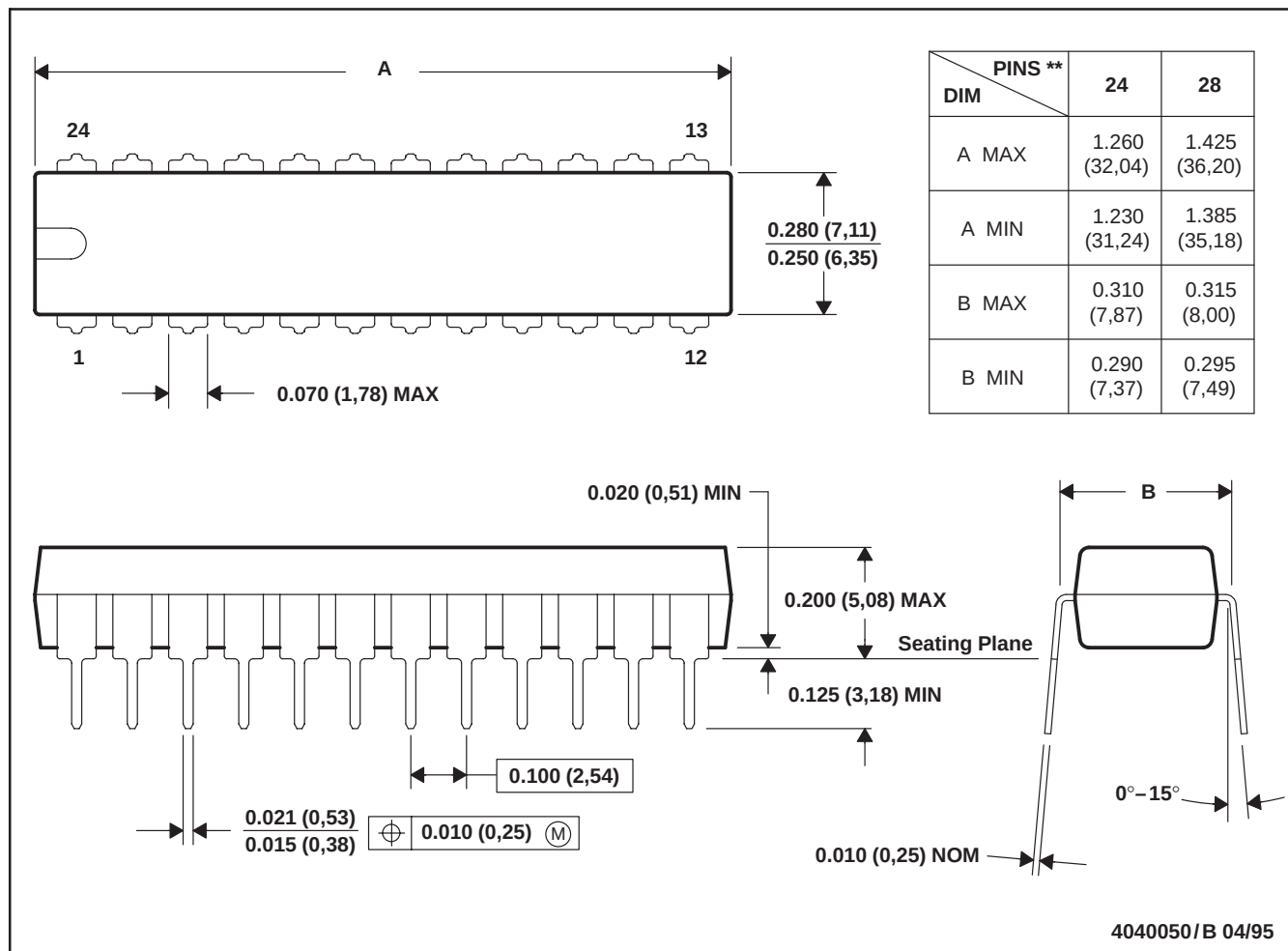
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NT (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

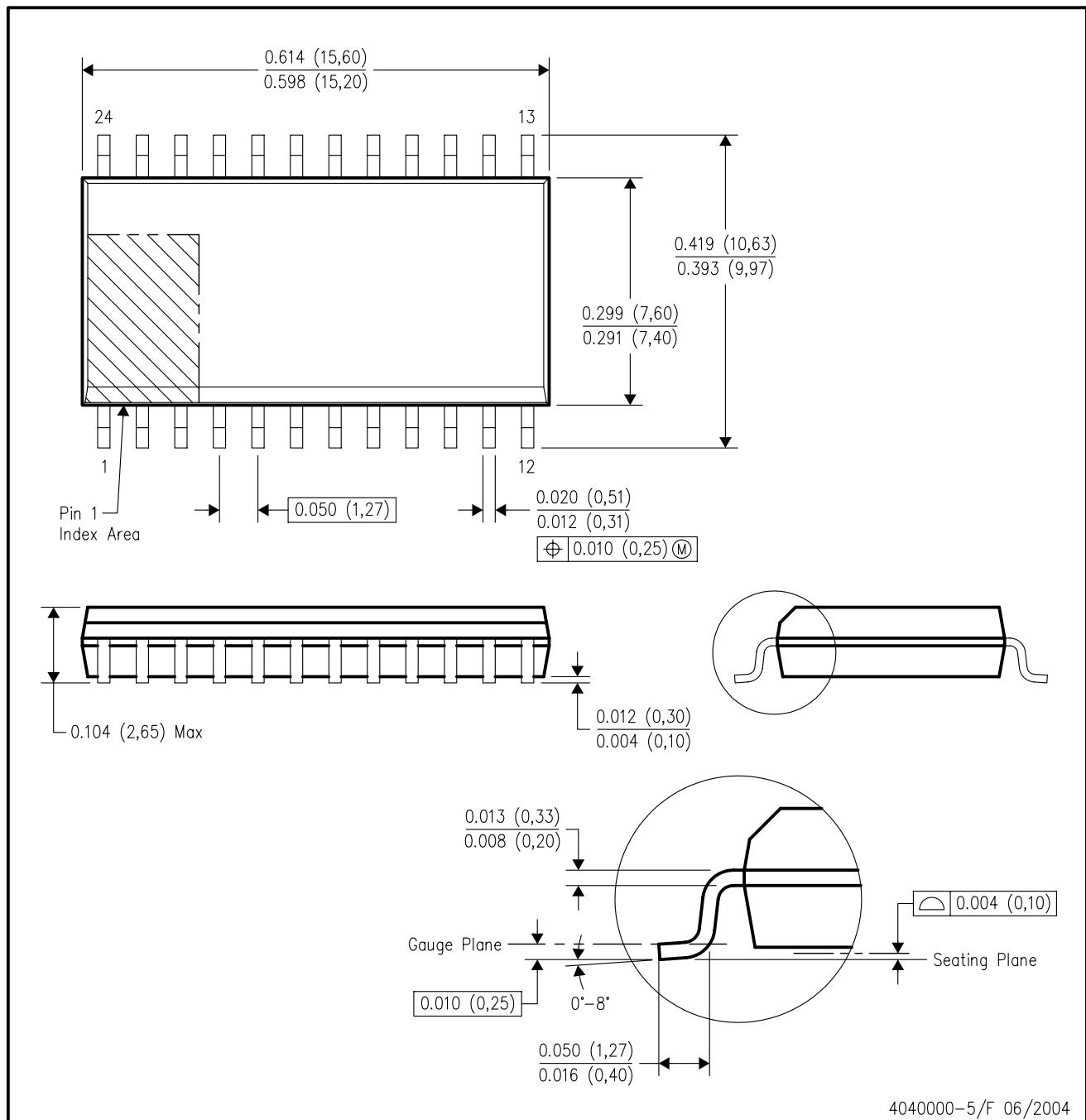
24 PINS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.

DW (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE

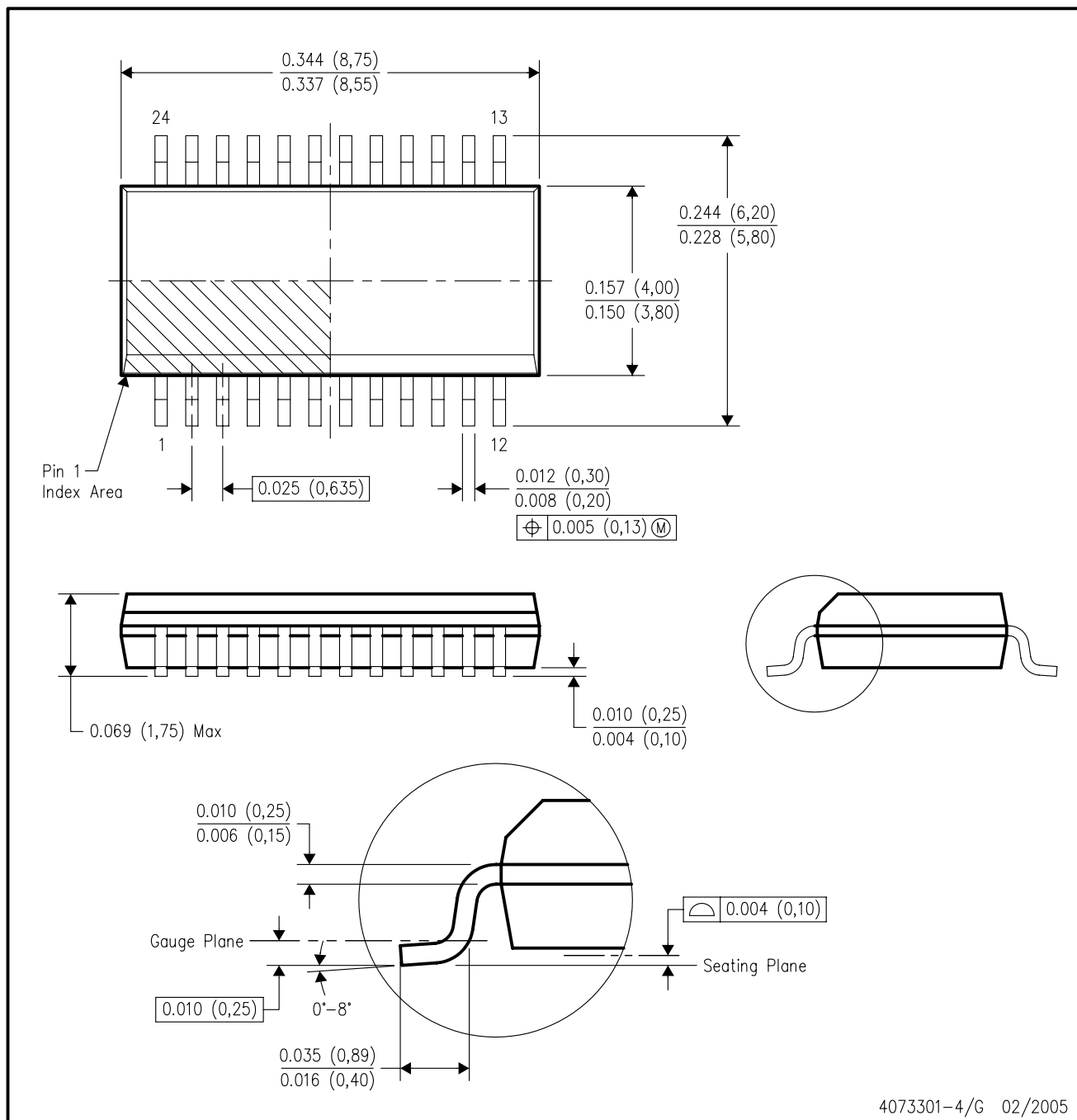


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- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MS-013 variation AD.

DBQ (R-PDSO-G24)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
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 - Falls within JEDEC MO-137 variation AE.

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CY74FCT821ATSOCT - <http://www.ti.com/product/cy74fct821atsoct?HQS=TI-null-null-dscatalog-df-pf-null-ww>

CY74FCT821BTSOC - <http://www.ti.com/product/cy74fct821btsoc?HQS=TI-null-null-dscatalog-df-pf-null-ww>

CY74FCT821T - <http://www.ti.com/product/cy74fct821t?HQS=TI-null-null-dscatalog-df-pf-null-ww>

CY74FCT821CTSOCT - <http://www.ti.com/product/cy74fct821ctsoct?HQS=TI-null-null-dscatalog-df-pf-null-ww>

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CY74FCT821CTSOC - <http://www.ti.com/product/cy74fct821ctsoc?HQS=TI-null-null-dscatalog-df-pf-null-ww>

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