

FSBS3CH60

Smart Power Module

Features

- UL Certified No.E209204(SPM27-BA package)
- 600V-3A 3-phase IGBT inverter bridge including control ICs for gate driving and protection
- Divided negative dc-link terminals for inverter current sensing applications
- Single-grounded power supply due to built-in HVIC
- Isolation rating of 2500Vrms/min.
- Very low leakage current due to using ceramic substrate

Applications

- AC 100V ~ 253V three-phase inverter drive for small power ac motor drives
- Home appliances applications like air conditioner and washing machine.

General Description

It is an advanced smart power module (SPM™) that Fairchild has newly developed and designed to provide very compact and high performance ac motor drives mainly targeting low-power inverter-driven application like air conditioner and washing machine. It combines optimized circuit protection and drive matched to low-loss IGBTs. System reliability is further enhanced by the integrated under-voltage lock-out and short-circuit protection. The high speed built-in HVIC provides optocoupler-less single-supply IGBT gate driving capability that further reduce the overall size of the inverter system design. Each phase current of inverter can be monitored separately due to the divided negative dc terminals.

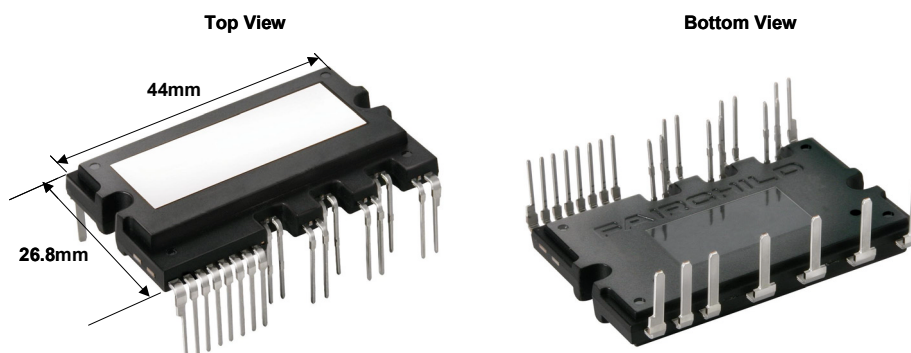


Figure 1.

Integrated Power Functions

- 600V-3A IGBT inverter for three-phase DC/AC power conversion (Please refer to Fig. 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting
Control circuit under-voltage (UV) protection
Note) Available bootstrap circuit example is given in Figs. 10 and 11.
- For inverter low-side IGBTs: Gate drive circuit, Short circuit protection (SC)
Control supply circuit under-voltage (UV) protection
- Fault signaling: Corresponding to a UV fault (Low-side supply)
- Input interface: 3.3/5V CMOS/LSTTL compatible, Schmitt trigger input

Pin Configuration

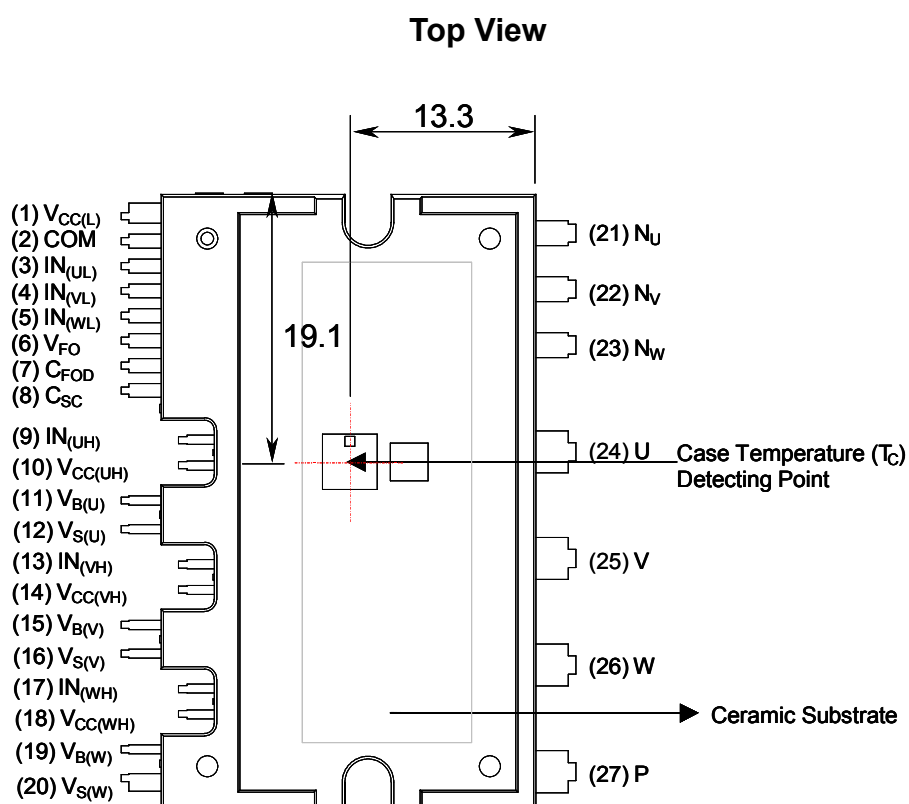
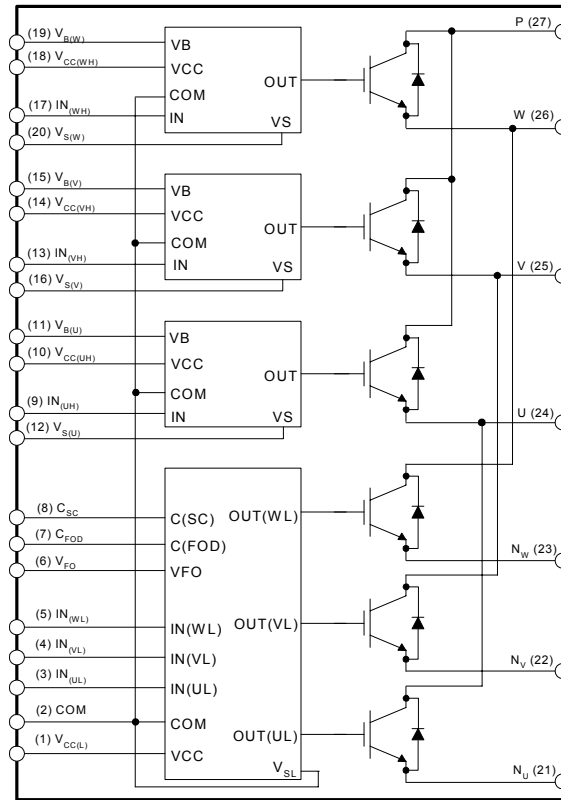


Figure 2.

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and IGBTs Driving
2	COM	Common Supply Ground
3	$IN_{(UL)}$	Signal Input for Low-side U Phase
4	$IN_{(VL)}$	Signal Input for Low-side V Phase
5	$IN_{(WL)}$	Signal Input for Low-side W Phase
6	V_{FO}	Fault Output
7	C_{FOD}	Capacitor for Fault Output Duration Time Selection
8	C_{SC}	Capacitor (Low-pass Filter) for Short-Current Detection Input
9	$IN_{(UH)}$	Signal Input for High-side U Phase
10	$V_{CC(UH)}$	High-side Bias Voltage for U Phase IC
11	$V_{B(U)}$	High-side Bias Voltage for U Phase IGBT Driving
12	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase IGBT Driving
13	$IN_{(VH)}$	Signal Input for High-side V Phase
14	$V_{CC(VH)}$	High-side Bias Voltage for V Phase IC
15	$V_{B(V)}$	High-side Bias Voltage for V Phase IGBT Driving
16	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase IGBT Driving
17	$IN_{(WH)}$	Signal Input for High-side W Phase
18	$V_{CC(WH)}$	High-side Bias Voltage for W Phase IC
19	$V_{B(W)}$	High-side Bias Voltage for W Phase IGBT Driving
20	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase IGBT Driving
21	N_U	Negative DC–Link Input for U Phase
22	N_V	Negative DC–Link Input for V Phase
23	N_W	Negative DC–Link Input for W Phase
24	U	Output for U Phase
25	V	Output for V Phase
26	W	Output for W Phase
27	P	Positive DC–Link Input

Internal Equivalent Circuit and Input/Output Pins



Note:

1. Inverter low-side is composed of three IGBTs including freewheeling diodes for each IGBT and one control IC which has gate driving and protection functions.
2. Inverter power side is composed of four inverter dc-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three IGBTs including freewheeling diodes (FWD) and three drive ICs for each IGBT.

Figure 3.

Absolute Maximum Ratings ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)

Inverter Part

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	Supply Voltage	Applied between P- N_U , N_V , N_W	450	V
$V_{PN(\text{Surge})}$	Supply Voltage (Surge)	Applied between P- N_U , N_V , N_W	500	V
V_{CES}	Collector-emitter Voltage		600	V
$\pm I_C$	Each IGBT Collector Current	$T_C = 25^\circ\text{C}$	3	A
$\pm I_{CP}$	Each IGBT Collector Current (Peak)	$T_C = 25^\circ\text{C}$, Under 1ms Pulse Width	6	A
P_C	Collector Dissipation	$T_C = 25^\circ\text{C}$ per One Chip	23	W
T_J	Operating Junction Temperature	(Note 1)	-20 ~ 125	$^\circ\text{C}$

Note:

1. The maximum junction temperature rating of the power chips integrated within the SPM is 150°C ($@T_C \leq 100^\circ\text{C}$). However, to insure safe operation of the SPM, the average junction temperature should be limited to $T_{J(\text{ave})} \leq 125^\circ\text{C}$ ($@T_C \leq 100^\circ\text{C}$).

Control Part

Symbol	Parameter	Conditions	Rating	Units
V_{CC}	Control Supply Voltage	Applied between $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$, $V_{CC(L)}$ - COM	20	V
V_{BS}	High-side Control Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	20	V
V_{IN}	Input Signal Voltage	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM	-0.3~17	V
V_{FO}	Fault Output Supply Voltage	Applied between V_{FO} - COM	-0.3~ $V_{CC}+0.3$	V
I_{FO}	Fault Output Current	Sink Current at V_{FO} Pin	5	mA
V_{SC}	Current Sensing Input Voltage	Applied between C_{SC} - COM	-0.3~ $V_{CC}+0.3$	V

Total System

Symbol	Parameter	Conditions	Rating	Units
$V_{PN(\text{PROT})}$	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{CC} = V_{BS} = 13.5 \sim 16.5\text{V}$ $T_J = 125^\circ\text{C}$, Non-repetitive, less than 2 μs	400	V
T_C	Module Case Operation Temperature	$-20^\circ\text{C} \leq T_J \leq 125^\circ\text{C}$, See Figure 2	-20 ~ 100	$^\circ\text{C}$
T_{STG}	Storage Temperature		-40 ~ 125	$^\circ\text{C}$
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, AC 1 minute, Connection Pins to ceramic substrate	2500	V_{rms}

Thermal Resistance

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance	Inverter IGBT part (per 1/6 module)	-	-	4.1	$^\circ\text{C/W}$
$R_{th(j-c)F}$		Inverter FWD part (per 1/6 module)	-	-	5.9	$^\circ\text{C/W}$

Note:

2. For the measurement point of case temperature(T_C), please refer to Figure 2.

Electrical Characteristics ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)

Inverter Part

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage	$V_{CC} = V_{BS} = 15\text{V}$ $V_{IN} = 5\text{V}$ $I_C = 3\text{A}$, $T_J = 25^\circ\text{C}$	-	-	2.3	V
V_F	FWD Forward Voltage	$V_{IN} = 0\text{V}$ $I_C = 3\text{A}$, $T_J = 25^\circ\text{C}$	-	-	2.1	V
HS	t_{ON}	$V_{PN} = 300\text{V}$, $V_{CC} = V_{BS} = 15\text{V}$ $I_C = 3\text{A}$ $V_{IN} = 0\text{V} \leftrightarrow 5\text{V}$, Inductive Load (Note 3)	-	0.39	-	us
	$t_{C(ON)}$		-	0.19	-	us
	t_{OFF}		-	0.56	-	us
	$t_{C(OFF)}$		-	0.19	-	us
	t_{rr}		-	0.10	-	us
LS	t_{ON}	$V_{PN} = 300\text{V}$, $V_{CC} = V_{BS} = 15\text{V}$ $I_C = 3\text{A}$ $V_{IN} = 0\text{V} \leftrightarrow 5\text{V}$, Inductive Load (Note 3)	-	0.57	-	us
	$t_{C(ON)}$		-	0.24	-	us
	t_{OFF}		-	0.62	-	us
	$t_{C(OFF)}$		-	0.20	-	us
	t_{rr}		-	0.10	-	us
	I_{CES}	Collector-Emitter Leakage Current	-	-	250	uA

Note:

3. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

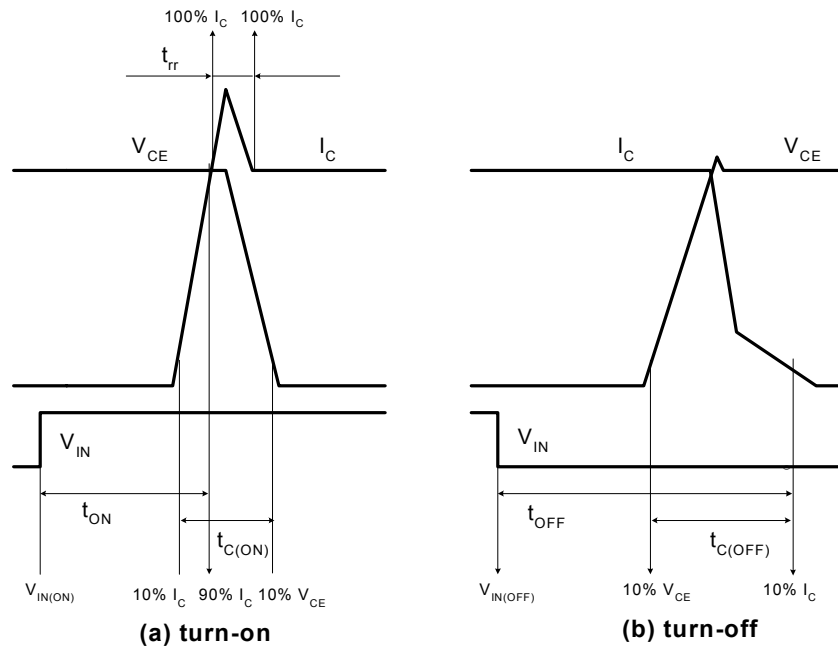


Figure 4. Switching Time Definition

Electrical Characteristics (T_J = 25°C, Unless Otherwise Specified)

Control Part

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
I _{QCCL}	Quiescent V _{CC} Supply Current	V _{CC} = 15V IN _(UL, VL, WL) = 0V	-	-	23	mA
I _{QCCH}		V _{CC} = 15V IN _(UH, VH, WH) = 0V	-	-	100	uA
I _{QBS}	Quiescent V _{BS} Supply Current	V _{BS} = 15V IN _(UH, VH, WH) = 0V	-	-	500	uA
V _{FOH}	Fault Output Voltage	V _{SC} = 0V, V _{FO} Circuit: 4.7kΩ to 5V Pull-up	4.5	-	-	V
V _{FOL}		V _{SC} = 1V, V _{FO} Circuit: 4.7kΩ to 5V Pull-up	-	-	0.8	V
V _{SC(ref)}	Short Circuit Trip Level	V _{CC} = 15V (Note 4)	0.45	0.5	0.55	V
UV _{CCD}	Supply Circuit Under-Voltage Protection	Detection Level	10.7	11.9	13.0	V
UV _{CCR}		Reset Level	11.2	12.4	13.2	V
UV _{BSD}		Detection Level	10.1	11.3	12.5	V
UV _{BSR}		Reset Level	10.5	11.7	12.9	V
t _{FOD}	Fault-out Pulse Width	C _{FOD} = 33nF (Note 5)	1.0	1.8	-	ms
V _{IN(ON)}	ON Threshold Voltage	Applied between IN _(UH) , IN _(VH) , IN _(WH) , IN _(UL) , IN _(VL) , IN _(WL) - COM	3.0	-	-	V
V _{IN(OFF)}	OFF Threshold Voltage		-	-	0.8	V

Note:

4. Short-circuit current protection is functioning only at the low-sides.

5. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : C_{FOD} = 18.3 x 10⁻⁶ x t_{FOD}[F]

Recommended Operating Conditions

Symbol	Parameter	Conditions	Value			Units
			Min.	Typ.	Max.	
V _{PN}	Supply Voltage	Applied between P - N _U , N _V , N _W	-	300	400	V
V _{CC}	Control Supply Voltage	Applied between V _{CC(UH)} , V _{CC(VH)} , V _{CC(WH)} , V _{CC(L)} - COM	13.5	15	16.5	V
V _{BS}	High-side Bias Voltage	Applied between V _{B(U)} - V _{S(U)} , V _{B(V)} - V _{S(V)} , V _{B(W)} - V _{S(W)}	13.0	15	18.5	V
DV _{CC} /Dt, DV _{BS} /Dt	Control supply variation		-1	-	1	V/us
t _{dead}	Blanking Time for Preventing Arm-short	For Each Input Signal	2	-	-	us
f _{PWM}	PWM Input Signal	-20°C ≤ T _C ≤ 100°C, -20°C ≤ T _J ≤ 125°C	-	-	20	kHz
V _{SEN}	Voltage for Current Sensing	Applied between N _U , N _V , N _W - COM (Including surge voltage)	-4		4	V

Mechanical Characteristics and Ratings

Parameter	Conditions		Limits			Units
			Min.	Typ.	Max.	
Mounting Torque	Mounting Screw: - M3	Recommended 0.62N•m	0.51	0.62	0.72	N•m
Device Flatness		Note Figure 5	0	-	+120	um
Weight			-	15.4	-	g

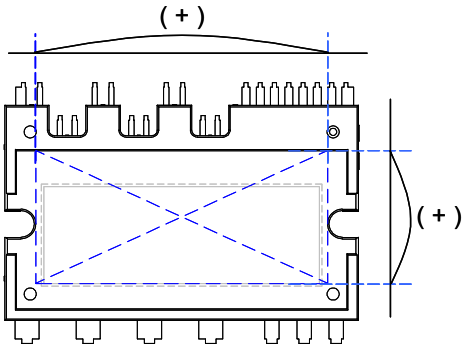
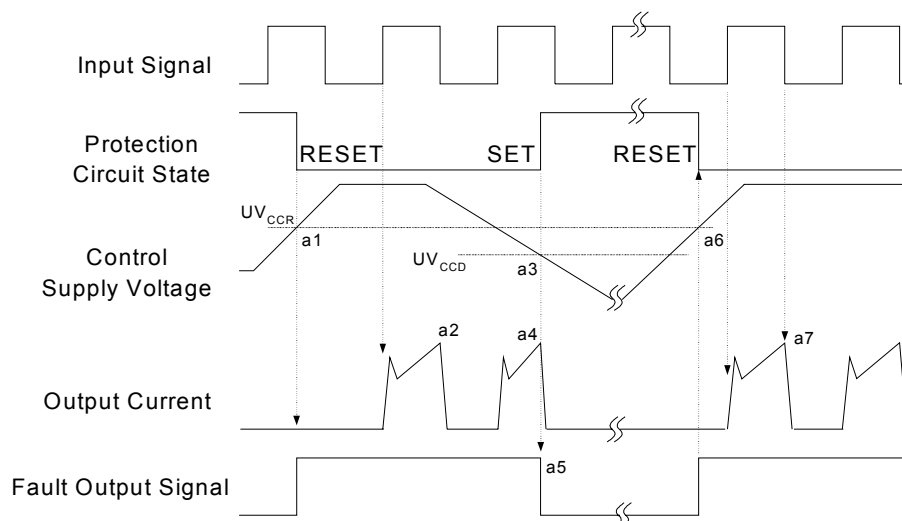


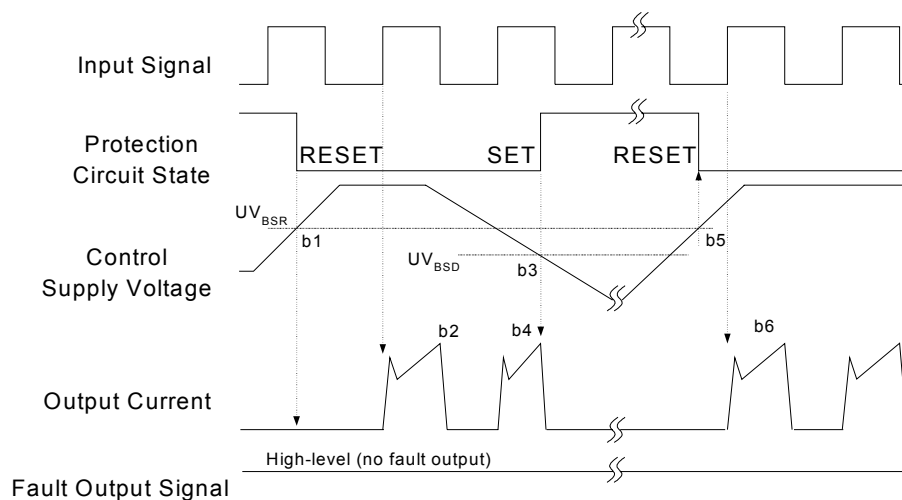
Figure 5. Flatness Measurement Position

Time Charts of SPMs Protective Function



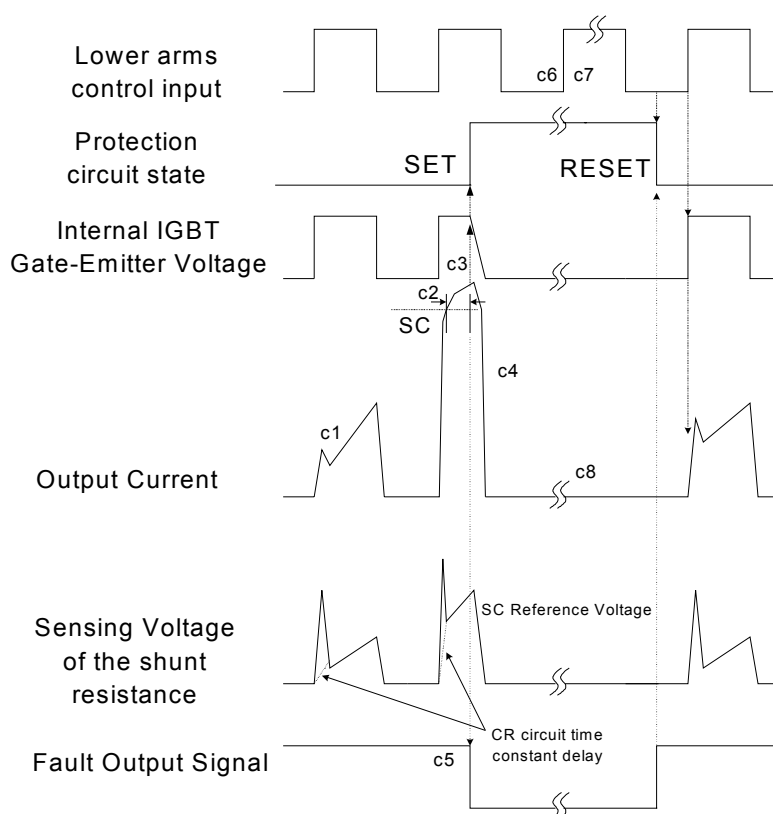
- a1 : Control supply voltage rises: After the voltage rises UV_{CCR} , the circuits start to operate when next input is applied.
- a2 : Normal operation: IGBT ON and carrying current.
- a3 : Under voltage detection (UV_{CCD}).
- a4 : IGBT OFF in spite of control input condition.
- a5 : Fault output operation starts.
- a6 : Under voltage reset (UV_{CCR}).
- a7 : Normal operation: IGBT ON and carrying current.

Figure 6. Under-Voltage Protection (Low-side)



- b1 : Control supply voltage rises: After the voltage reaches UV_{BSR} , the circuits start to operate when next input is applied.
- b2 : Normal operation: IGBT ON and carrying current.
- b3 : Under voltage detection (UV_{BSD}).
- b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5 : Under voltage reset (UV_{BSR})
- b6 : Normal operation: IGBT ON and carrying current

Figure 7. Under-Voltage Protection (High-side)



(with the external shunt resistance and CR connection)

c1 : Normal operation: IGBT ON and carrying current.

c2 : Short circuit current detection (SC trigger).

c3 : Hard IGBT gate interrupt.

c4 : IGBT turns OFF.

c5 : Fault output timer operation starts: The pulse width of the fault output signal is set by the external capacitor C_{FO} .

c6 : Input "L" : IGBT OFF state.

c7 : Input "H": IGBT ON state, but during the active period of fault output the IGBT doesn't turn ON.

c8 : IGBT OFF state

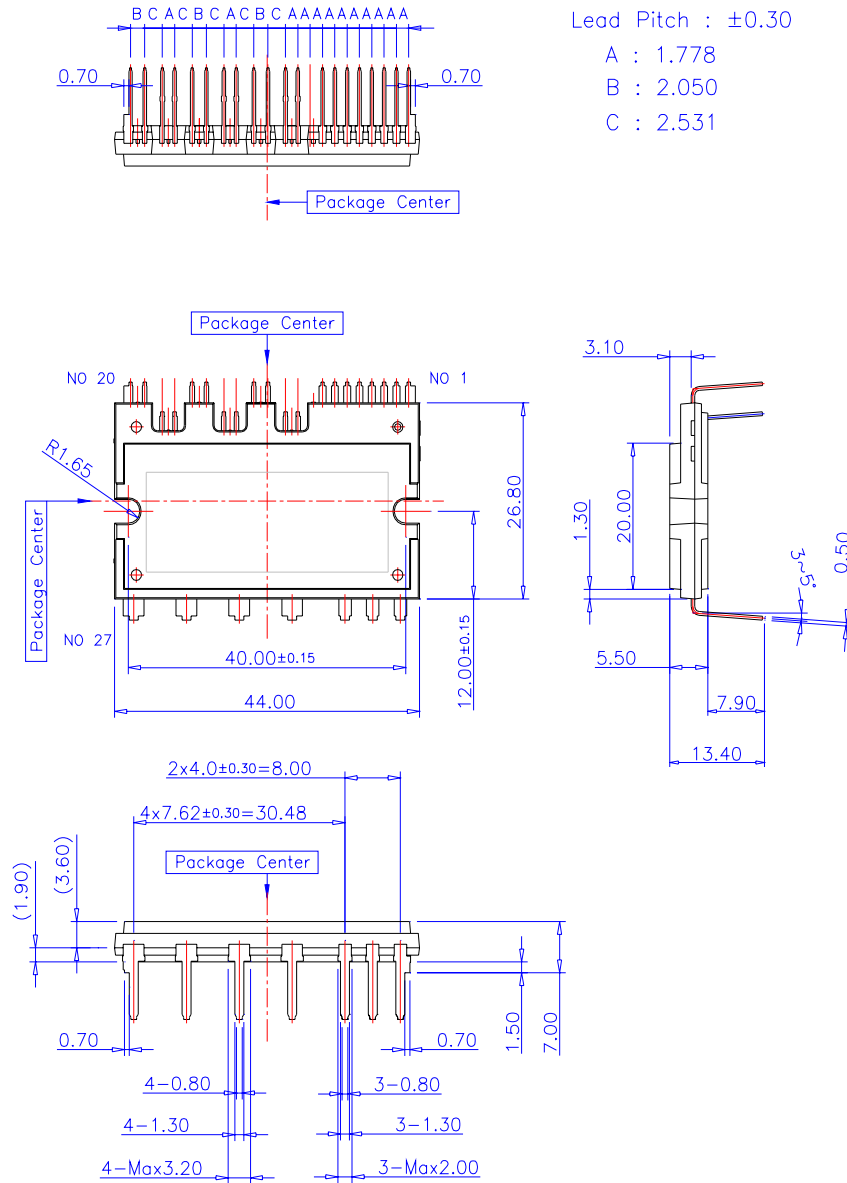
Figure 8. Short-Circuit Current Protection (Low-side Operation only)

1. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The SPM input signal section integrates 3.3k Ω (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.
2. The logic input is compatible with standard CMOS or LSTTL outputs.

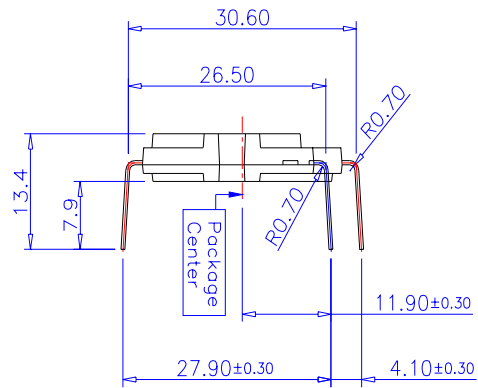
1. It would be recommended that the bootstrap diode, D_{BS} , has soft and fast recovery characteristics.
2. The bootstrap resistor (R_{BS}) should be 3 times greater than $R_{E(H)}$. The recommended value of $R_{E(H)}$ is 5.6Ω , but it can be increased up to 20Ω (maximum) for a slower dv/dt of high-side.
3. The ceramic capacitor placed between V_{CC} -COM should be over $1\mu F$ and mounted as close to the pins of the SPM as possible.

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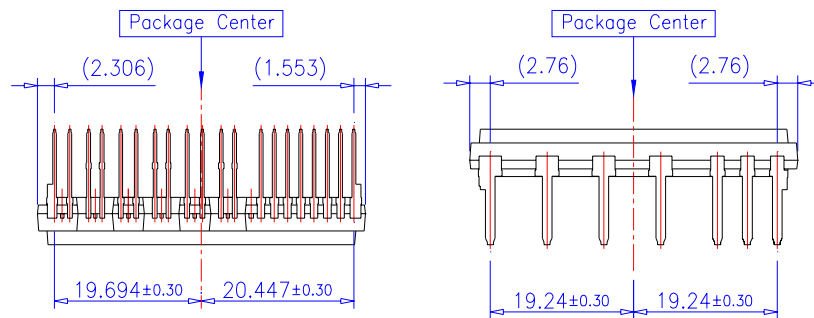
Detailed Package Outline Drawings



Detailed Package Outline Drawings (Continued)

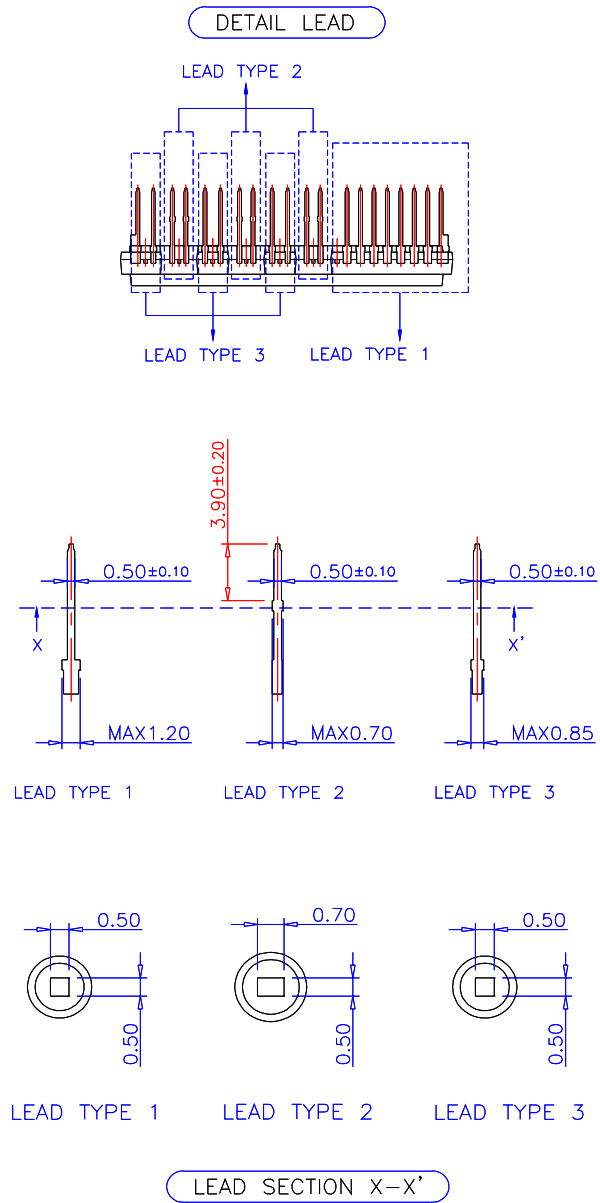


Lead Forming Dimension



PKG Center to Lead Distance

Detailed Package Outline Drawings (Continued)



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