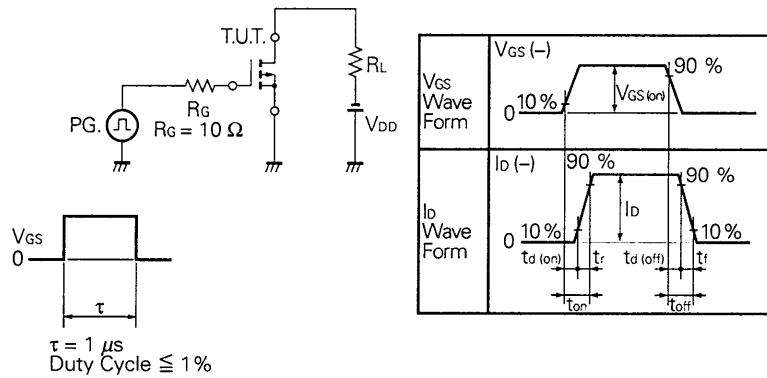


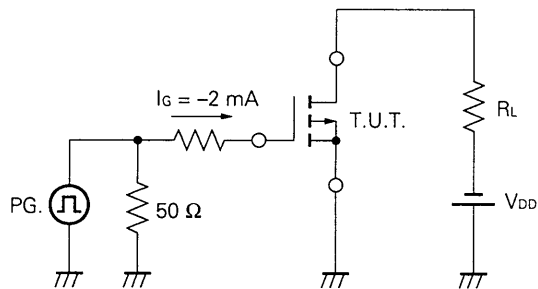
ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Drain to Source On-state Resistance	R _{DS(on)}		47	60	mΩ	V _{GS} = -10 V, I _D = -8 A
Drain to Source On-state Resistance	R _{DS(on)}		80	110	mΩ	V _{GS} = -4 V, I _D = -6 A
Gate to Source Cutoff Voltage	V _{GS(off)}	-1.0	-1.5	-2.0	V	V _{DS} = -10 V, I _D = -1 mA
Forward Transfer Admittance	y _{fs}	8.0	12		S	V _{DS} = -10 V, I _D = -8 A
Drain Leakage Current	I _{DSS}			-10	μA	V _{DS} = -60 V, V _{GS} = 0
Gate to Source Leakage Current	I _{GSS}			±10	μA	V _{GS} = ±16 V, V _{DS} = 0
Input Capacitance	C _{iss}		2 150		pF	V _{DS} = -10 V
Output Capacitance	C _{oss}		1 100		pF	V _{GS} = 0
Reverse Transfer Capacitance	C _{rss}		530		pF	f = 1 MHz
Turn-On Delay Time	t _{d(on)}		35		ns	V _{GS(on)} = -10 V V _{DD} = -30 V I _D = -8 A, R _G = 10 Ω R _L = 3.8 Ω
Rise Time	t _r		150		ns	
Turn-Off Delay Time	t _{d(off)}		260		ns	
Fall Time	t _f		230		ns	
Total Gate Charge	Q _G		80		nC	V _{GS} = -10 V I _D = -15 A V _{DD} = -48 V
Gate to Source Charge	Q _{GS}		6		nC	
Gate to Drain Charge	Q _{GD}		35		nC	
Diode Forward Voltage	V _{SD}		1.0		V	I _F = 15 A, V _{GS} = 0
Reverse Recovery Time	t _{rr}		120		ns	I _F = 15 A, V _{GS} = 0
Reverse Recovery Charge	Q _{rr}		260		nC	di/dt = 50 A/μs

Test Circuit 1: Switching Time

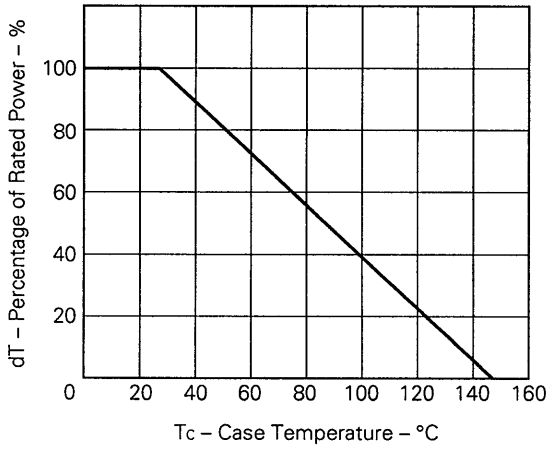


Test Circuit 2: Gate Charge

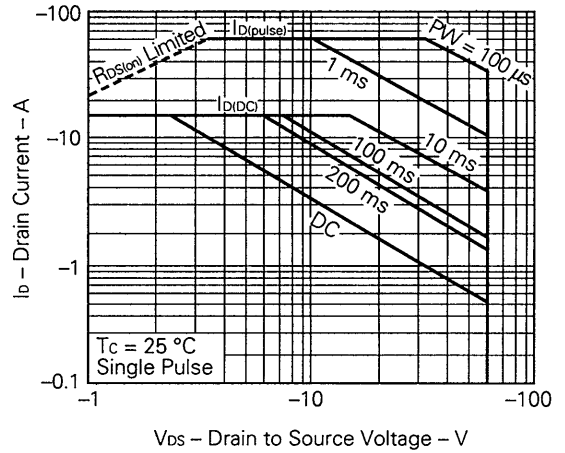


ELECTRICAL CHARACTERISTICS (T_a = 25 °C)

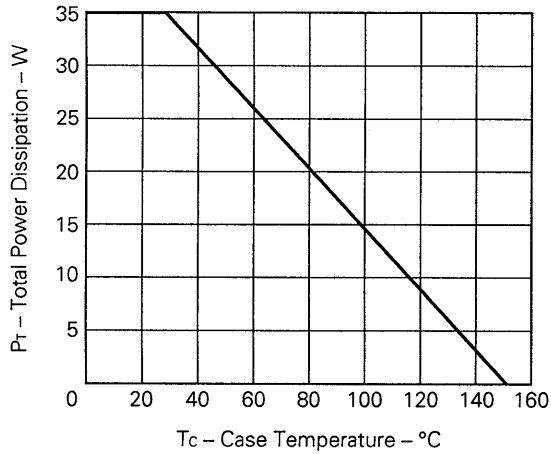
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



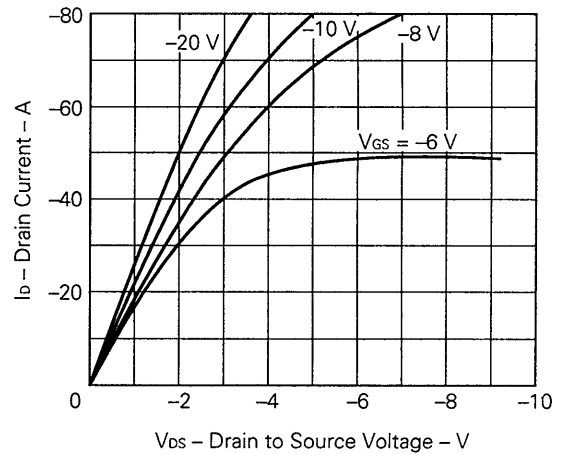
FORWARD BIAS SAFE OPERATING AREA



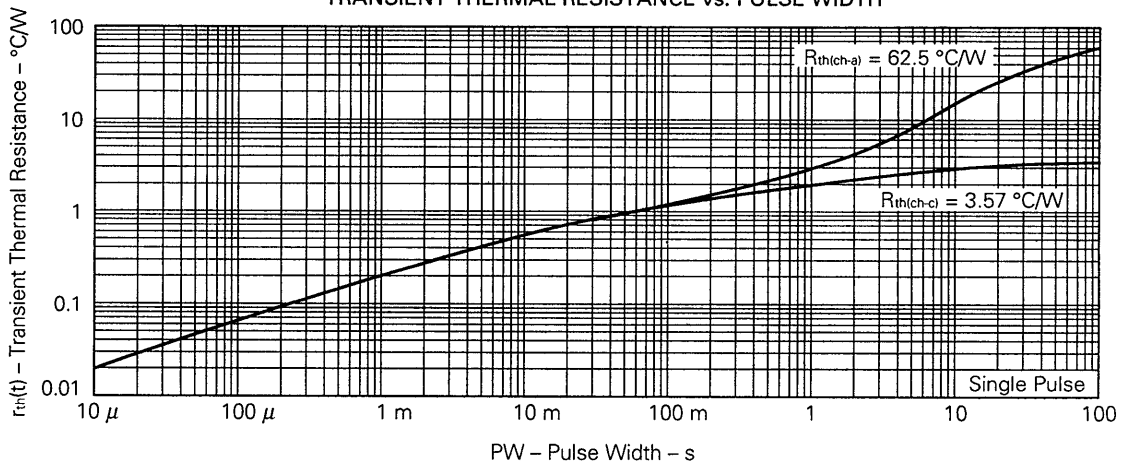
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



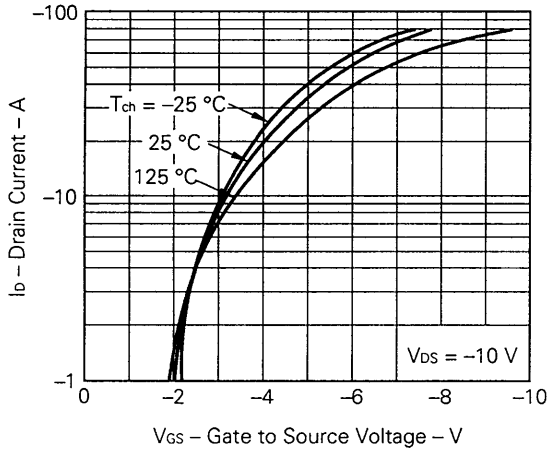
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



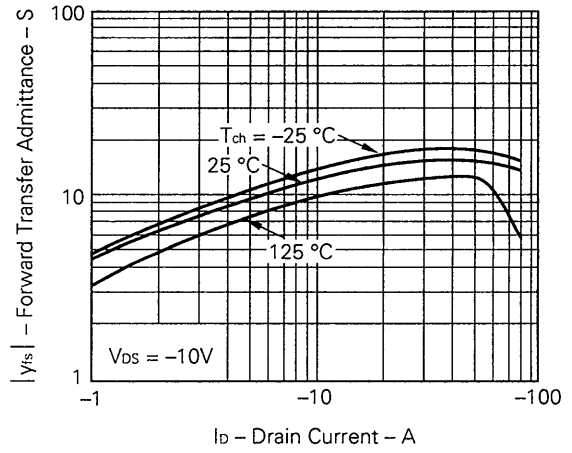
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



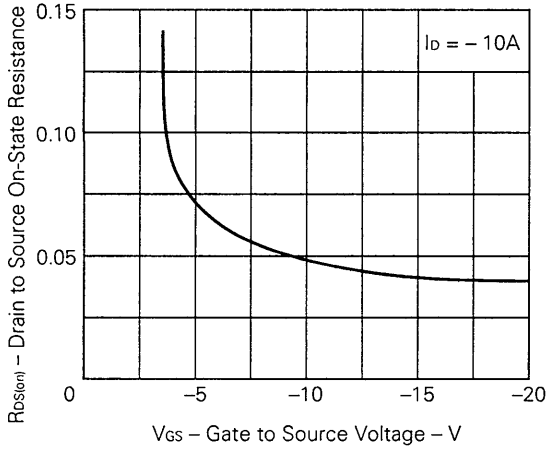
TRANSFER CHARACTERISTICS



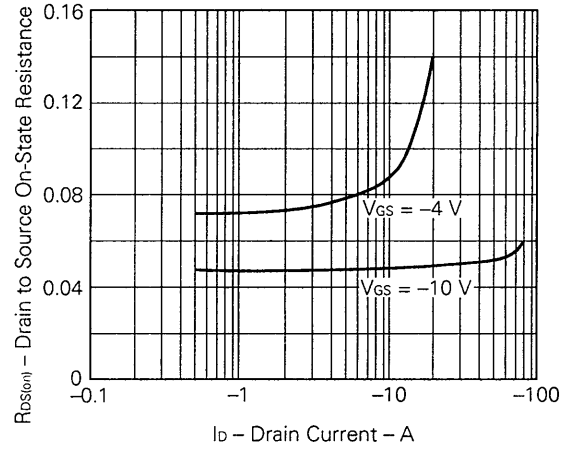
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



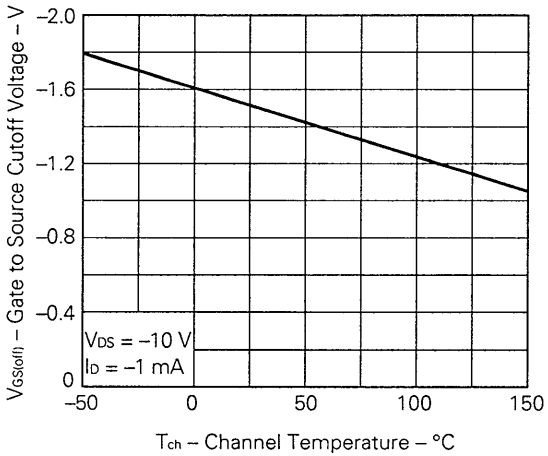
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



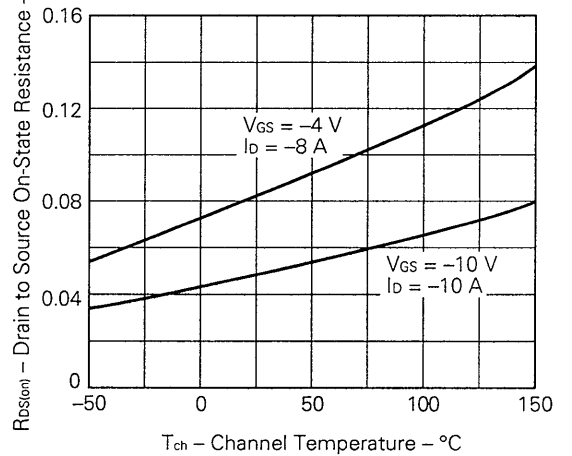
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

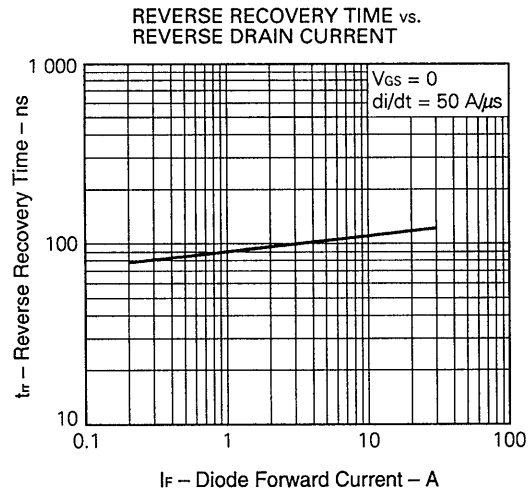
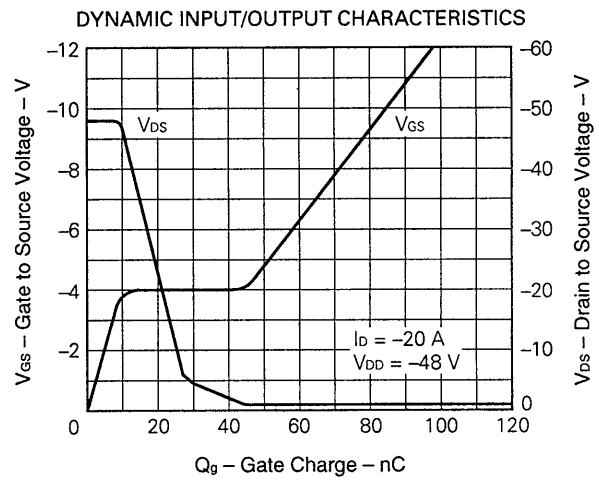
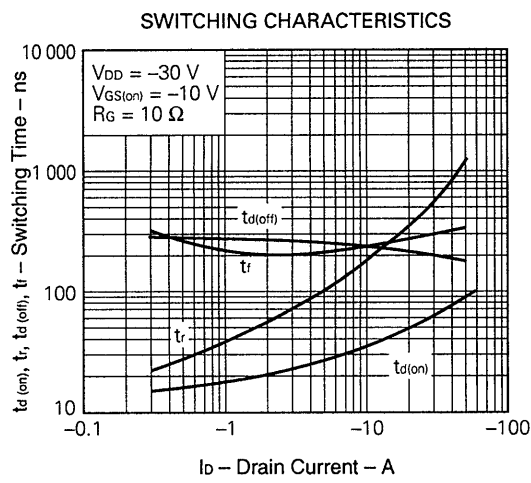
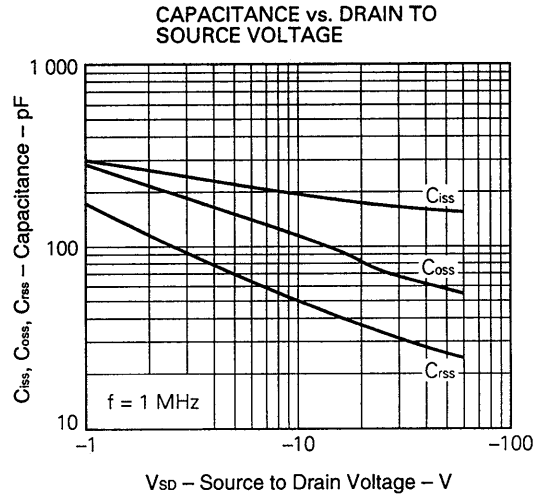
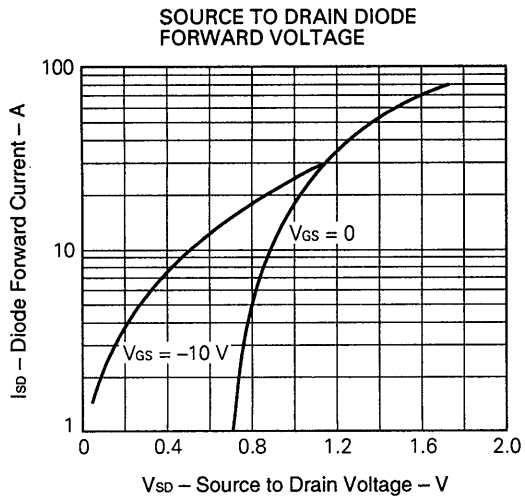


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE





Reference

Application note name	No.
Safe operating area of Power MOS FET.	TEA-1034
Application circuit using Power MOS FET.	TEA-1035
Quality control of NEC semiconductors devices.	TEI-1202
Quality control guide of semiconductors devices.	MEI-1202
Assembly manual of semiconductors devices.	IEI-1207

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