

## Dual P-Channel 30-V (D-S) MOSFET

### ■ Features

- Low  $r_{DS(on)}$  Provides Higher Efficiency and Extends Battery Life
- Miniature SO-8 Surface Mount Package Saves Board Space
- High power and current handling capability
- Extended  $V_{GS}$  range ( $\pm 25$ ) for battery pack applications

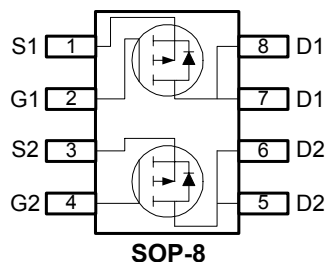
### ■ General Description

These miniature surface mount MOSFETs utilize High Cell Density process. Low  $r_{DS(on)}$  assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

### ■ Product Summary

$V_{DS}$ (V)	$r_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
-30	52@ $V_{GS}=-10V$	-5.2
	89@ $V_{GS}=-4.5V$	-4.0

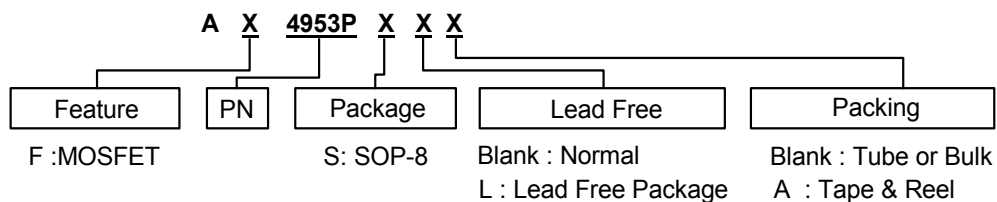
### ■ Pin Assignments



### ■ Pin Descriptions

Pin Name	Description
S1/2	Channel 1/2 Source
G1/2	Channel 1/2 Gate
D1/2	Channel 1/2 Drain

### ■ Ordering information





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### ■ Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	-30	V
$V_{GS}$	Gate-Source Voltage	$\pm 25$	V
$I_D$	Continuous Drain Current (Note 1)	$T_A=25^\circ\text{C}$	$\pm 5.2$
		$T_A=70^\circ\text{C}$	$\pm 4.2$
$I_{DM}$	Pulsed Drain Current (Note 2)	$\pm 30$	A
$I_S$	Continuous Source Current (Diode Conduction) (Note 1)	-1.6	A
$P_D$	Power Dissipation (Note 1)	$T_A=25^\circ\text{C}$	2.1
		$T_A=70^\circ\text{C}$	1.3
$T_J, T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$

### ■ Thermal Resistance Ratings

Symbol	Parameter	Maximum	Units
$R_{\theta JC}$	Maximum Junction-to-Case (Note 1)	40	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Junction-to-Ambient (Note 1)	60	$^\circ\text{C/W}$

Note 1: surface Mounted on 1"x 1" FR4 Board.

Note 2: Pulse width limited by maximum junction temperature

### ■ Specifications ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Limits			Unit
			Min.	Typ.	Max.	
<b>Static</b>						
$V_{(BR)DSS}$	Drain-Source breakdown Voltage	$V_{GS}=0V, I_D=-250\mu\text{A}$	-30	-	-	V
$V_{GS(th)}$	Gate-Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1	-1.6	-3	V
$I_{GSS}$	Gate-Body Leakage	$V_{DS}=0V, V_{GS}=\pm 25V$	-	-	$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=-24V, V_{GS}=0V$	-	-	-1	uA
		$V_{DS}=-24V, V_{GS}=0V, T_J=55^\circ\text{C}$	-	-	-5	
$I_{D(on)}$	On-State Drain Current (Note 3)	$V_{DS}=-5V, V_{GS}=-10V$	-30	-	-	A
$r_{DS(on)}$	Drain-Source On-Resistance (Note 3)	$V_{GS}=-10V, I_D=-5.2A$	-	40	52	m $\Omega$
		$V_{GS}=-4.5V, I_D=-4.0A$	-	67	89	
		$V_{GS}=-10V, I_D=-5.2A, T_J=55^\circ\text{C}$	-	44	57	
$g_{fs}$	Forward Transconductance (Note 3)	$V_{DS}=-15V, I_D=-5.2A$	-	19	-	S
$V_{SD}$	Diode Forward Voltage	$I_S=-2.1A, V_{GS}=0V$	-	-0.7	-1.2	V
<b>Dynamic (Note 4)</b>						
$Q_g$	Total Gate Charge	$V_{DS}=-15V, V_{GS}=-10V, I_D=-5.2A$	-	15	19	nC
$Q_{gs}$	Gate-Source Charge		-	2.2	-	
$Q_{gd}$	Gate-Drain Charge		-	1.7	-	
<b>Switching</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD}=-15, R_L=15\Omega, I_D=-1A, V_{GEN}=-10V, R_G=6\Omega$	-	7	14	nS
$t_r$	Rise Time		-	13	24	
$t_{d(off)}$	Turn-Off Delay Time		-	14	25	
$t_f$	Fall-Time		-	9	17	

Note 3: Pulse test:  $PW \leq 300\mu\text{s}$  duty cycle  $\leq 2\%$ .

Note 4: Guaranteed by design, not subject to production testing.

## Dual P-Channel 30-V (D-S) MOSFET

### Typical Performance Characteristics

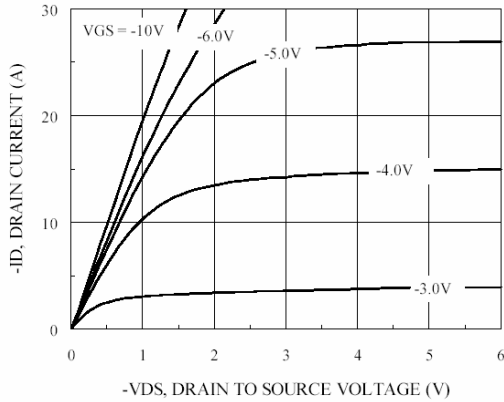


Figure 1. On-Region Characteristics

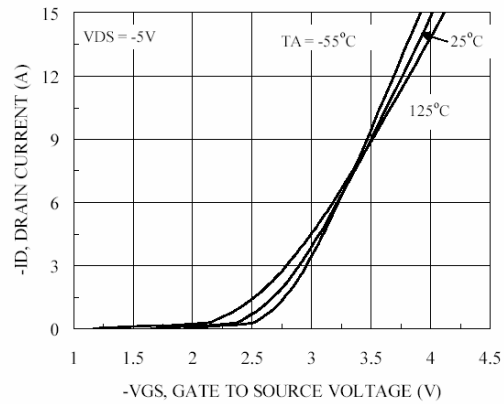


Figure 2. Body Diode Forward Voltage Variation with Source Current and Temperature

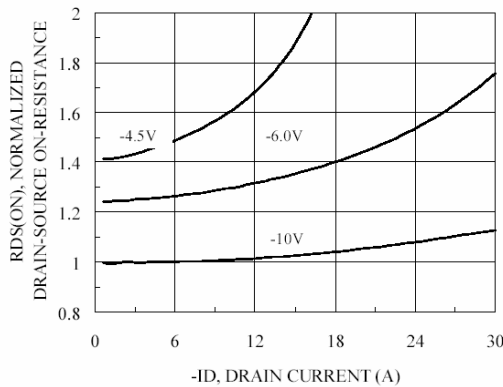


Figure 3. On Resistance Vs Vgs Voltage

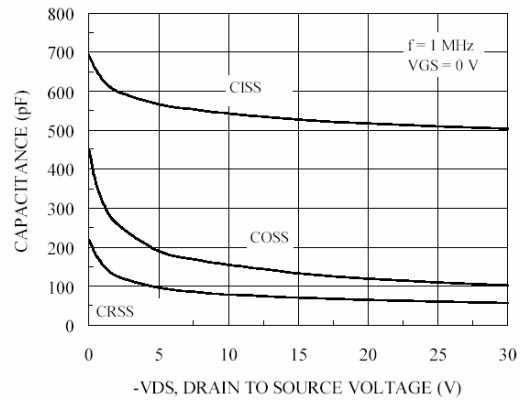


Figure 4. Capacitance Characteristics

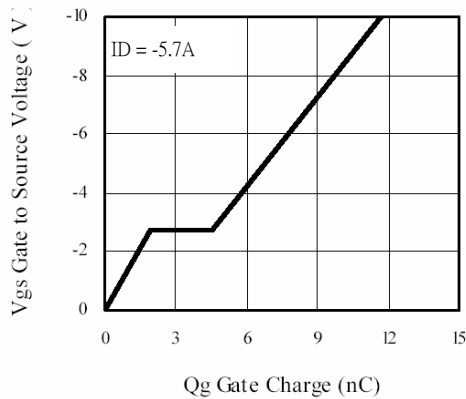


Figure 5. Gate Charge Characteristics

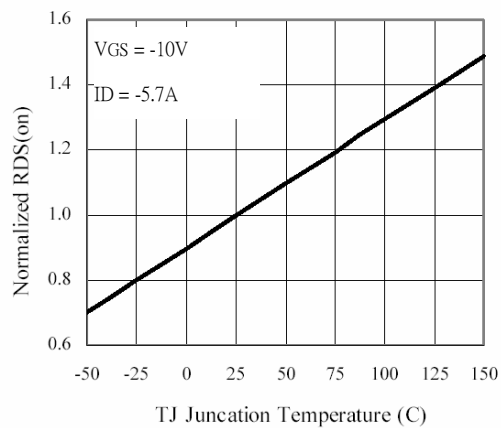


Figure 6. On-Resistance Variation with Temperature

## Dual P-Channel 30-V (D-S) MOSFET

### Typical Performance Characteristics (Continued)

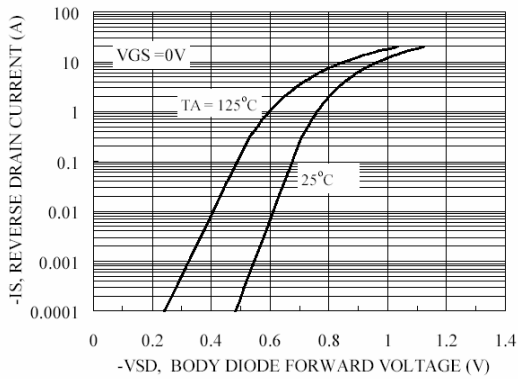


Figure 7. Transfer Characteristics

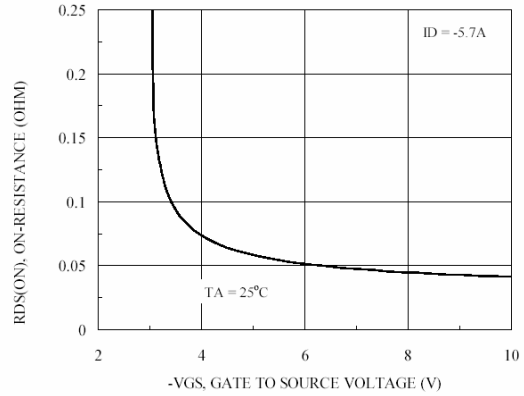


Figure 8. On-Resistance with Gate to Source Voltage

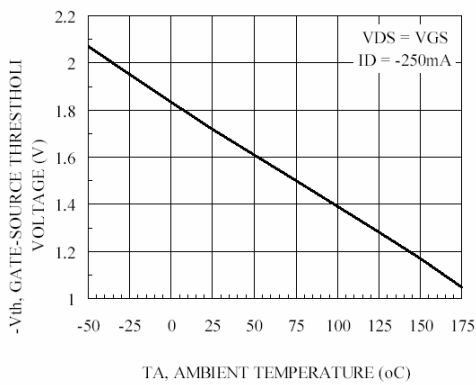


Figure 9. Vth Gate to Source Voltage Vs Temperature

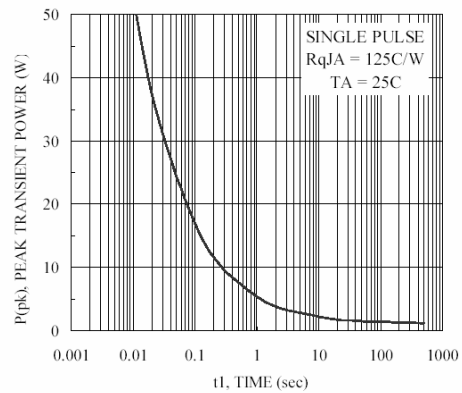


Figure 10. Single Pulse Maximum Power Dissipation

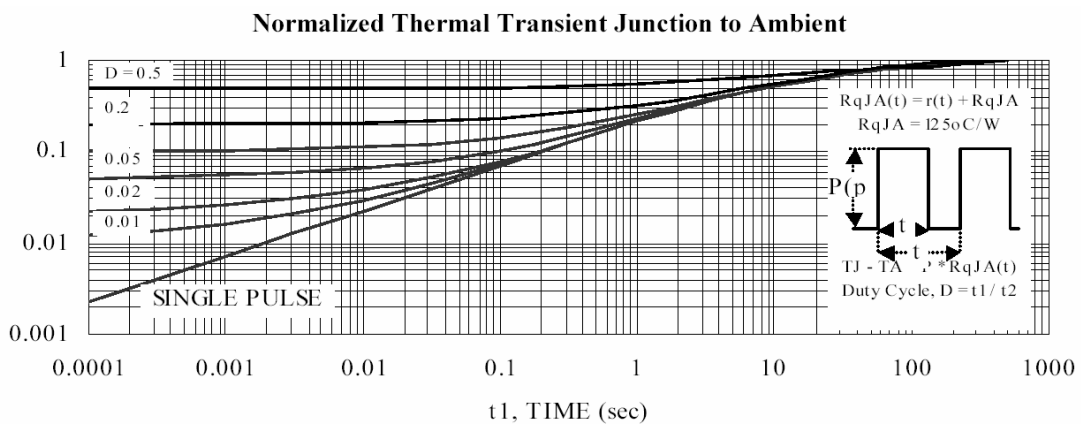
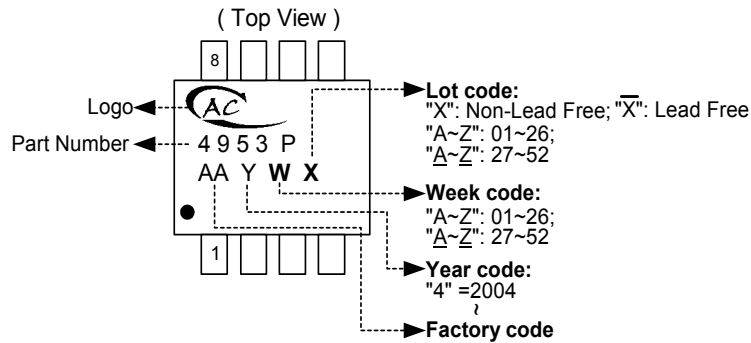


Figure 11. Transient Thermal Response Curve

## Dual P-Channel 30-V (D-S) MOSFET

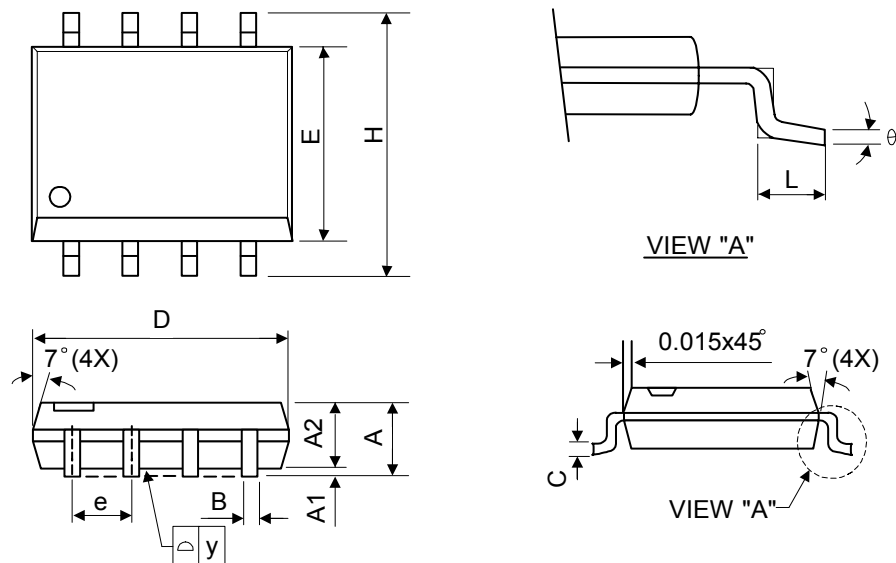
### ■ Marking Information

SOP-8L



### ■ Package Information

Package Type: SOP-8L



Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	1.40	1.60	1.75	0.055	0.063	0.069
A1	0.10	-	0.25	0.040	-	0.100
A2	1.30	1.45	1.50	0.051	0.057	0.059
B	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.010
D	4.80	5.05	5.30	0.189	0.199	0.209
E	3.70	3.90	4.10	0.146	0.154	0.161
e	-	1.27	-	-	0.050	-
H	5.79	5.99	6.20	0.228	0.236	0.244
L	0.38	0.71	1.27	0.015	0.028	0.050
y	-	-	0.10	-	-	0.004
θ	0°	-	8°	0°	-	8°



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