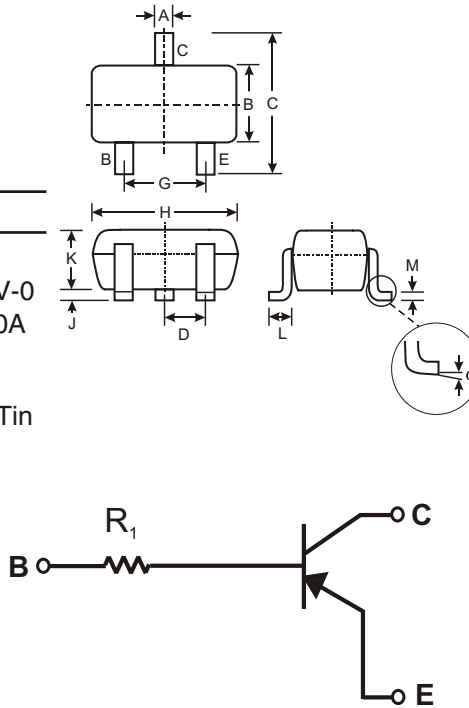


### Features

- Epitaxial Planar Die Construction
- Complementary NPN Types Available (DDTC)
- Built-In Biasing Resistor, R1 only
- Also Available in Lead Free Version

### Mechanical Data

- Case: SC-59, Molded Plastic
- Case material - UL Flammability Rating 94V-0
- Moisture sensitivity: Level 1 per J-STD-020A
- Terminals: Solderable per MIL-STD-202, Method 208
- Also Available in Lead Free Plating (Matte Tin Finish). Please see Ordering Information, Note 3, on Page 2
- Terminal Connections: See Diagram
- Marking: Date Code and Marking Code (See Diagrams & Page 2)
- Weight: 0.008 grams (approx.)
- Ordering Information (See Page 2)



SC-59		
Dim	Min	Max
A	0.35	0.50
B	1.50	1.70
C	2.70	3.00
D	0.95	
G	1.90	
H	2.90	3.10
J	0.013	0.10
K	1.00	1.30
L	0.35	0.55
M	0.10	0.20
$\alpha$	0°	8°
All Dimensions in mm		

P/N	R1 (NOM)	MARKING
DDTA113TKA	1K $\Omega$	P01
DDTA123TKA	2.2K $\Omega$	P03
DDTA143TKA	4.7K $\Omega$	P07
DDTA114TKA	10K $\Omega$	P12
DDTA124TKA	22K $\Omega$	P16
DDTA144TKA	47K $\Omega$	P19
DDTA115TKA	100K $\Omega$	P23
DDTA125TKA	200K $\Omega$	P25

SCHMATIC DIAGRAM

### Maximum Ratings @ T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Value	Unit
Collector-Base Voltage	V <sub>CBO</sub>	-50	V
Collector-Emitter Voltage	V <sub>CEO</sub>	-50	V
Emitter-Base Voltage	V <sub>EBO</sub>	-5	V
Collector Current	I <sub>C</sub> (Max)	-100	mA
Power Dissipation	P <sub>d</sub>	200	mW
Thermal Resistance, Junction to Ambient Air (Note 1)	R <sub>θJA</sub>	625	°C/W
Operating and Storage and Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

Note: 1. Mounted on FR4 PC Board with recommended pad layout at <http://www.diodes.com/datasheets/ap02001.pdf>.

## Electrical Characteristics @ T<sub>A</sub> = 25°C unless otherwise specified

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
Collector-Base Breakdown Voltage	BV <sub>CBO</sub>	-50	—	—	V	I <sub>C</sub> = -50μA
Collector-Emitter Breakdown Voltage	BV <sub>CEO</sub>	-50	—	—	V	I <sub>C</sub> = -1mA
Emitter-Base Breakdown Voltage	BV <sub>EBO</sub>	-5	—	—	V	I <sub>E</sub> = -50μA
Collector Cutoff Current	I <sub>CBO</sub>	—	—	-0.5	μA	V <sub>CB</sub> = -50V
Emitter Cutoff Current	I <sub>EBO</sub>	—	—	-0.5	μA	V <sub>EB</sub> = -4V
Collector-Emitter Saturation Voltage	V <sub>CE(sat)</sub>	—	—	-0.3	V	I <sub>C</sub> /I <sub>B</sub> = -10mA/-1mA DDTA113TKA I <sub>C</sub> /I <sub>B</sub> = -5mA/-0.5mA DDTA123TKA I <sub>C</sub> /I <sub>B</sub> = -2.5mA/-0.25mA DDTA143TKA I <sub>C</sub> /I <sub>B</sub> = -1mA/-0.1mA DDTA114TKA I <sub>C</sub> /I <sub>B</sub> = -5mA/-0.5mA DDTA124TKA I <sub>C</sub> /I <sub>B</sub> = -2.5mA/-0.25mA DDTA144TKA I <sub>C</sub> /I <sub>B</sub> = -1mA/-0.1mA DDTA115TKA I <sub>C</sub> /I <sub>B</sub> = -0.5mA/-0.05mA DDTA125TKA
DC Current Transfer Ratio	h <sub>FE</sub>	100	250	600	—	I <sub>C</sub> = -1mA, V <sub>CE</sub> = -5V
Input Resistor (R <sub>1</sub> ) Tolerance	DR <sub>1</sub>	-30	—	+30	%	—
Gain-Bandwidth Product*	f <sub>T</sub>	—	250	—	MHz	V <sub>CE</sub> = -10V, I <sub>E</sub> = 5mA, f = 100MHz

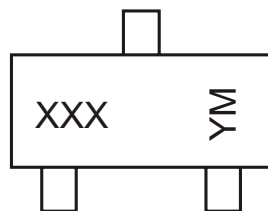
\* Transistor - For Reference Only

## Ordering Information (Note 2)

Device	Packaging	Shipping
DDTA113TKA-7	SC-59	3000/Tape & Reel
DDTA123TKA-7	SC-59	3000/Tape & Reel
DDTA143TKA-7	SC-59	3000/Tape & Reel
DDTA114TKA-7	SC-59	3000/Tape & Reel
DDTA124TKA-7	SC-59	3000/Tape & Reel
DDTA144TKA-7	SC-59	3000/Tape & Reel
DDTA115TKA-7	SC-59	3000/Tape & Reel
DDTA125TKA-7	SC-59	3000/Tape & Reel

- Notes:
- For Packaging Details, go to our website at <http://www.diodes.com/datasheets/ap02007.pdf>.
  - For Lead Free version (with Lead Free terminal finish) part number, please add "-F" suffix to part number above.  
Example: DDTA125TKA-7-F.

## Marking Information



XXX = Product Type Marking Code  
See Sheet 1 Diagrams  
YM = Date Code Marking  
Y = Year ex: N = 2002  
M = Month ex: 9 = September

Date Code Key

Year	2002	2003	2004	2005	2006	2007	2008	2009
Code	N	P	R	S	T	U	V	W

Month	Jan	Feb	March	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

**TYPICAL CURVES - DDTA114TKA**

**NEW PRODUCT**

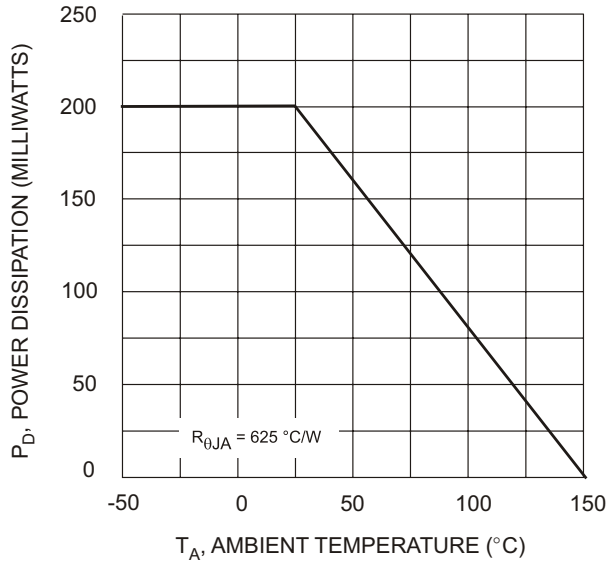


Fig. 1 Derating Curve

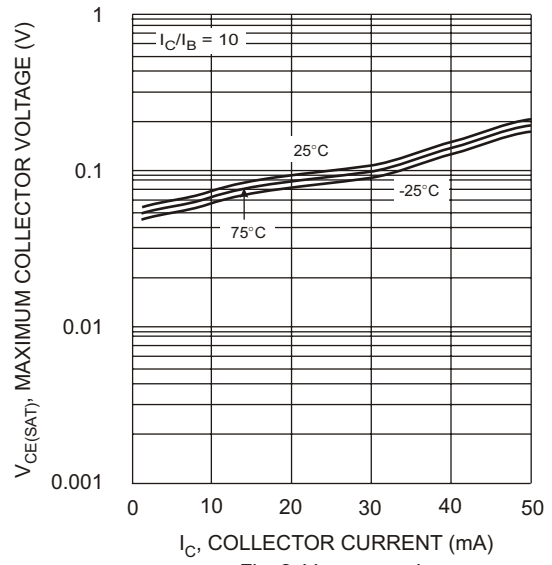


Fig. 2  $V_{CE(SAT)}$  vs.  $I_C$

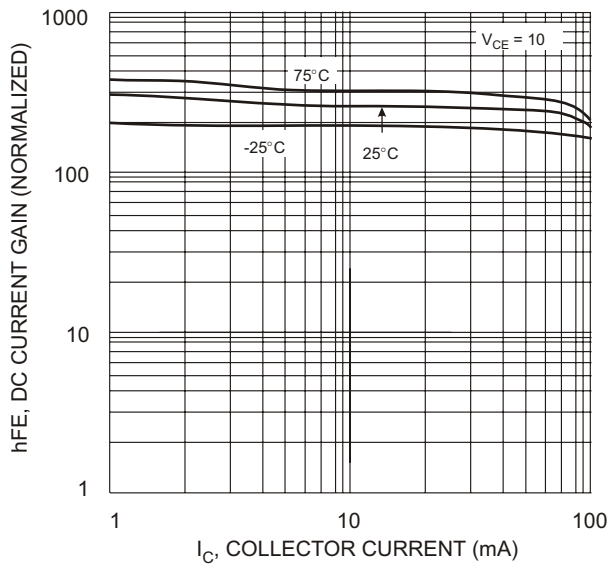


Fig. 3 DC Current Gain

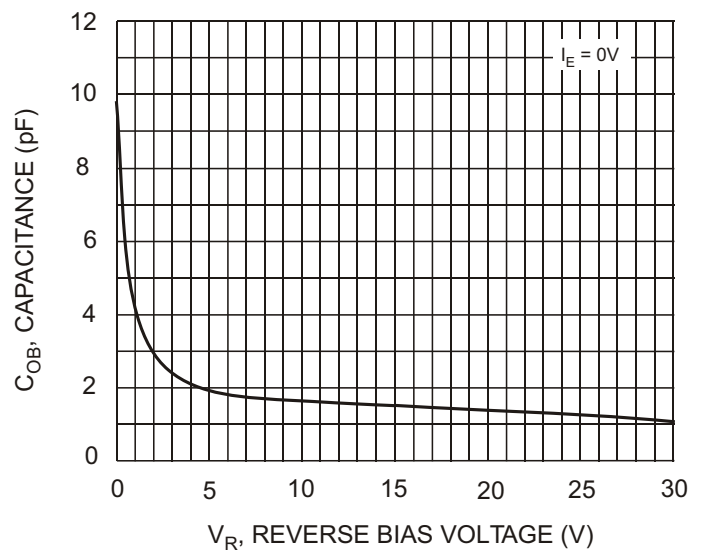


Fig. 4 Output Capacitance

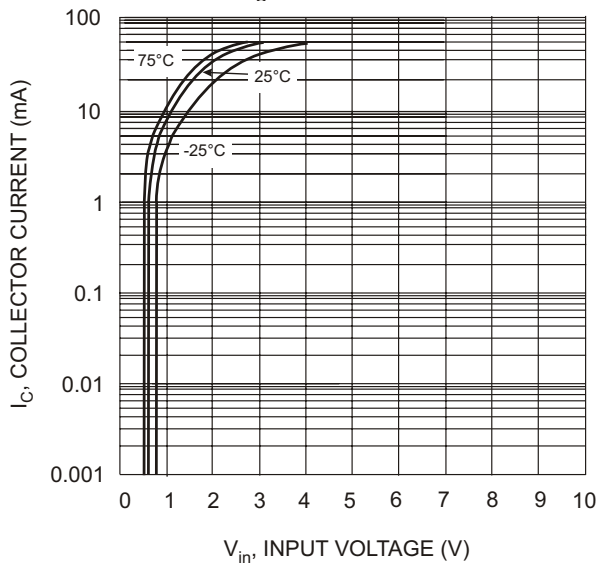


Fig. 5 Collector Current Vs. Input Voltage

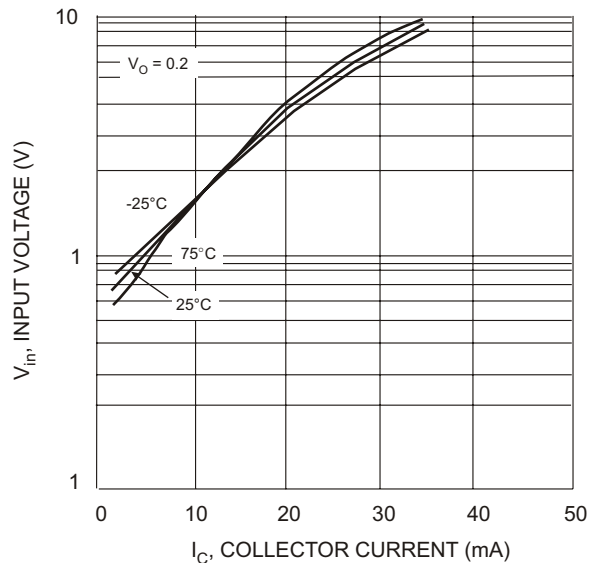


Fig. 6 Input Voltage vs. Collector Current



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