

Product Summary

$V_{(BR)DSS}$	$R_{DS(on)}$ max	I_D max $T_A = +25^\circ\text{C}$
30V	16m Ω @ $V_{GS} = 10\text{V}$	9.8A
	22m Ω @ $V_{GS} = 4.5\text{V}$	8.4A

Description

This MOSFET has been designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

Applications

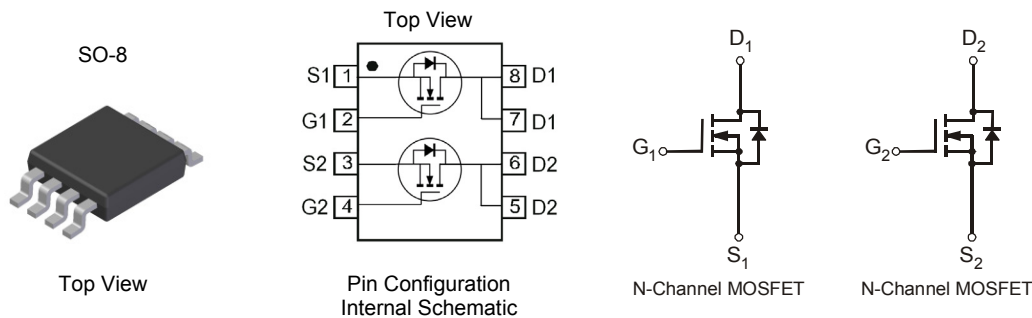
- Backlighting
- Power Management Functions
- DC-DC Converters

Features and Benefits

- 100% avalanche rated part
- Low $R_{DS(on)}$ - minimizes conduction losses
- Low Q_g - minimizes switching losses
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 standards for High Reliability**

Mechanical Data

- Case: SO-8
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Connections Indicator: See diagram
- Terminals: Finish — Matte Tin annealed over Copper leadframe. Solderable per MIL-STD-202, Method 208 $\text{\textcircled{3}}$
- Weight: 0.076 grams (approximate)

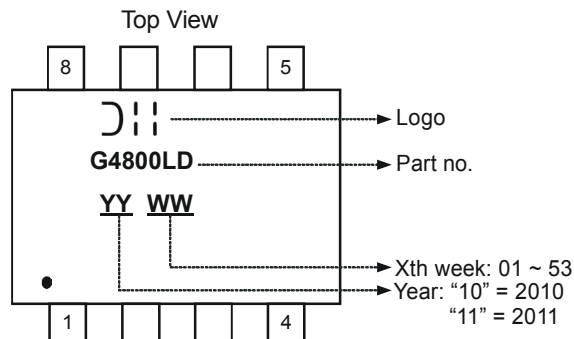


Ordering Information (Note 4)

Part Number	Compliance	Case	Packaging
DMG4800LSD-13	Standard	SO-8	2500 / Tape & Reel
DMG4800LSDQ-13	Automotive	SO-8	2500 / Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 4. For packaging details, go to our website at <http://www.diodes.com/products/packages.html>.

Marking Information



Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	30	V
Gate-Source Voltage			V_{GSS}	± 25	V
Continuous Drain Current (Note 6) $V_{GS} = 10\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	7.5 6.0	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	9.8 7.7	A
Continuous Drain Current (Note 6) $V_{GS} = 4.5\text{V}$	Steady State	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	6.4 5.0	A
	$t < 10\text{s}$	$T_A = +25^\circ\text{C}$ $T_A = +70^\circ\text{C}$	I_D	8.4 6.6	A
Maximum Continuous Body Diode Forward Current (Note 6)			I_S	2	A
Pulsed Drain Current (10 μs pulse, duty cycle = 1%)			I_{DM}	42	A
Avalanche Current (Notes 7 & 8) $L = 0.1\text{mH}$			I_{AR}	17	A
Repetitive Avalanche Energy (Notes 7 & 8) $L = 0.1\text{mH}$			E_{AR}	14	mJ

Thermal Characteristics

Characteristic			Symbol	Value	Units
Total Power Dissipation (Note 5)			P_D	1.17	W
Thermal Resistance, Junction to Ambient (Note 5)	Steady State		$R_{\theta JA}$	107	$^\circ\text{C/W}$
	$t < 10\text{s}$			61	
Total Power Dissipation (Note 6)			P_D	1.5	W
Thermal Resistance, Junction to Ambient (Note 6)	Steady State		$R_{\theta JA}$	83	$^\circ\text{C/W}$
	$t < 10\text{s}$			49	
Thermal Resistance, Junction to Case			$R_{\theta JC}$	14.5	
Operating and Storage Temperature Range			T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 9)						
Drain-Source Breakdown Voltage	BV_{DSS}	30	-	-	V	$V_{GS} = 0\text{V}, I_D = 250\mu\text{A}$
Zero Gate Voltage Drain Current $T_J = +25^\circ\text{C}$	I_{DSS}	-	-	1.0	μA	$V_{DS} = 30\text{V}, V_{GS} = 0\text{V}$
Gate-Source Leakage	I_{GSS}	-	-	± 100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$
ON CHARACTERISTICS (Note 9)						
Gate Threshold Voltage	$V_{GS(th)}$	0.8	-	1.6	V	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$
Static Drain-Source On-Resistance	$R_{DS(on)}$	-	12	16	m Ω	$V_{GS} = 10\text{V}, I_D = 9\text{A}$
		-	16	22		$V_{GS} = 4.5\text{V}, I_D = 7\text{A}$
Forward Transfer Admittance	$ Y_{fs} $	-	8	-	S	$V_{DS} = 10\text{V}, I_D = 9\text{A}$
Diode Forward Voltage	V_{SD}	-	0.72	0.94	V	$V_{GS} = 0\text{V}, I_S = 1\text{A}$
DYNAMIC CHARACTERISTICS (Note 10)						
Input Capacitance	C_{iss}	-	798	-	pF	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V},$ $f = 1.0\text{MHz}$
Output Capacitance	C_{oss}	-	128	-	pF	
Reverse Transfer Capacitance	C_{rss}	-	122	-	pF	
Gate Resistance	R_g	-	1.37	-	Ω	$V_{DS} = 0\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$
Total Gate Charge	Q_g	-	8.56	-	nC	$V_{GS} = 5\text{V}, V_{DS} = 15\text{V},$ $I_D = 9\text{A}$
Gate-Source Charge	Q_{gs}	-	1.8	-	nC	
Gate-Drain Charge	Q_{gd}	-	2.5	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	5.03	-	ns	$V_{DD} = 15\text{V}, V_{GEN} = 10\text{V},$ $R_L = 15\Omega, R_G = 6\Omega, I_D = 1\text{A}$
Turn-On Rise Time	t_r	-	4.50	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	26.33	-	ns	
Turn-Off Fall Time	t_f	-	8.55	-	ns	

- Notes:
- Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 - Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.
 - I_{AR} and E_{AR} rating are based on low frequency and duty cycles to keep $T_J = +25^\circ\text{C}$.
 - Applicable to products manufactured with Data Code "1146" (Nov, 2011) and newer.
 - Short duration pulse test used to minimize self-heating effect.
 - Guaranteed by design. Not subject to product testing.

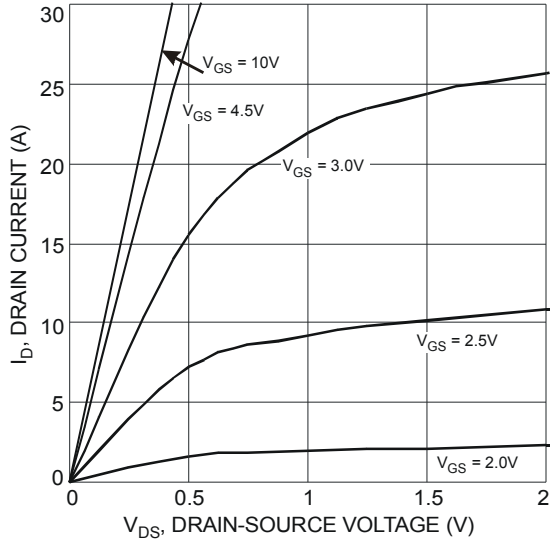


Fig. 1 Typical Output Characteristic

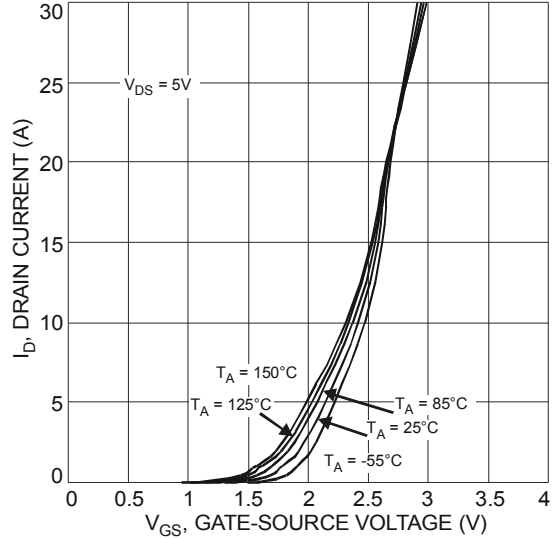


Fig. 2 Typical Transfer Characteristic

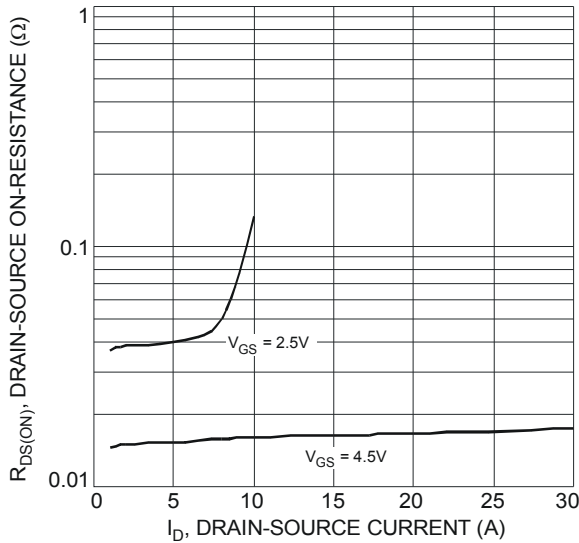


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

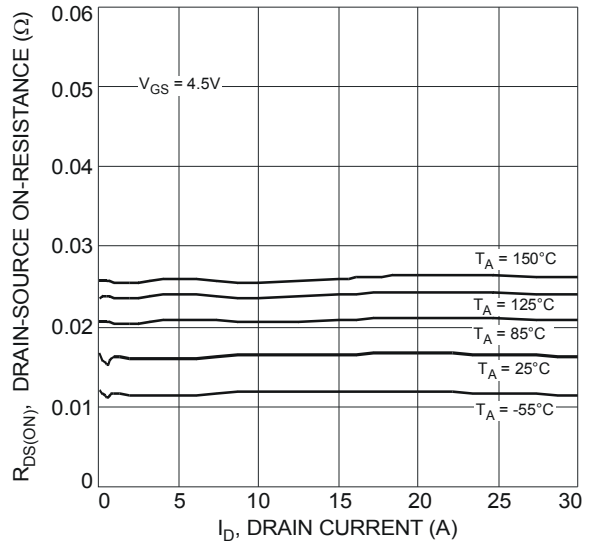


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

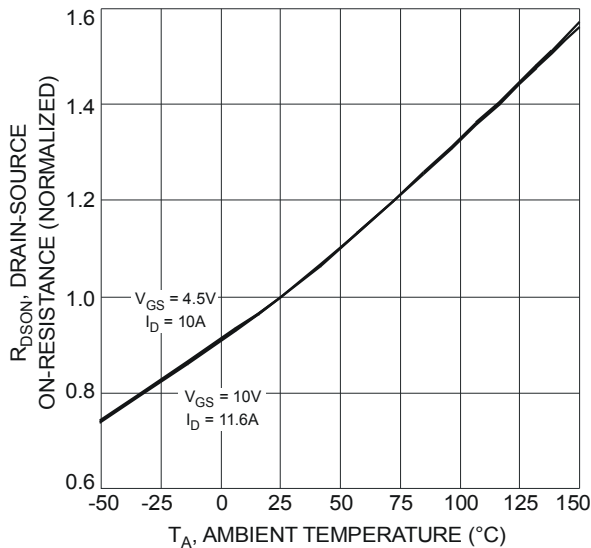


Fig. 5 On-Resistance Variation with Temperature

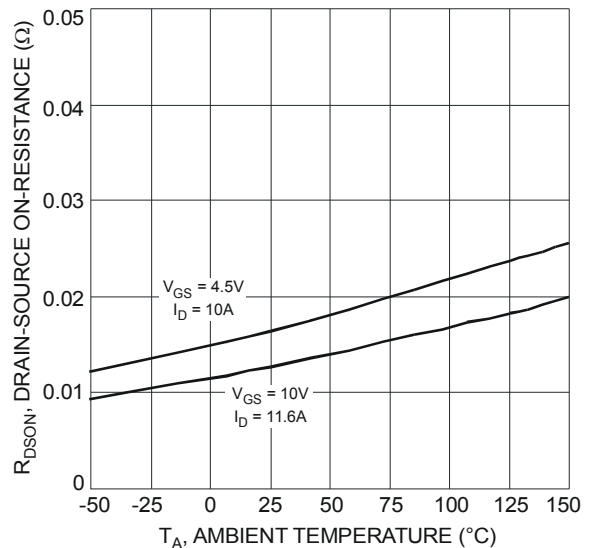


Fig. 6 On-Resistance Variation with Temperature

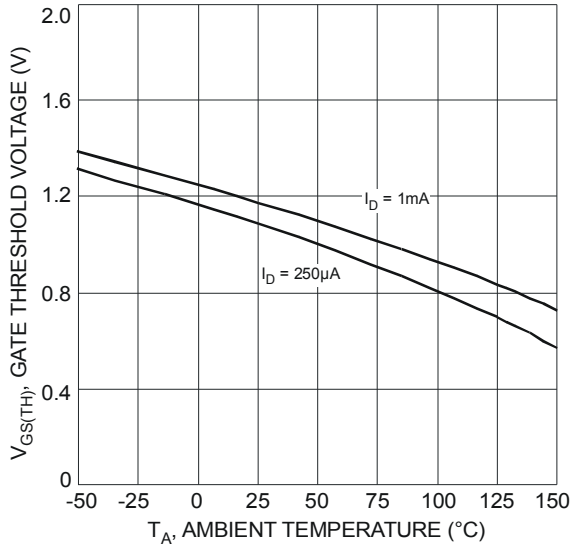


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

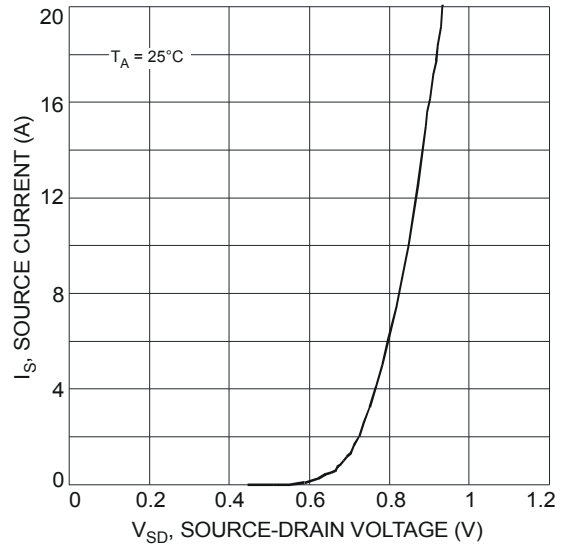


Fig. 8 Diode Forward Voltage vs. Current

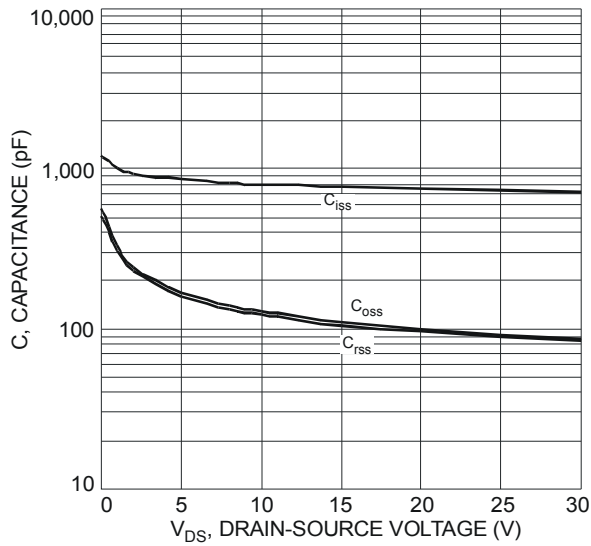


Fig. 9 Typical Total Capacitance

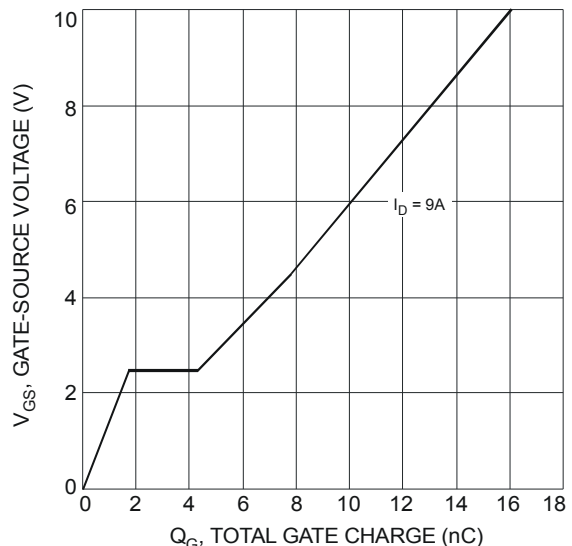


Fig. 10 Total Gate Charge

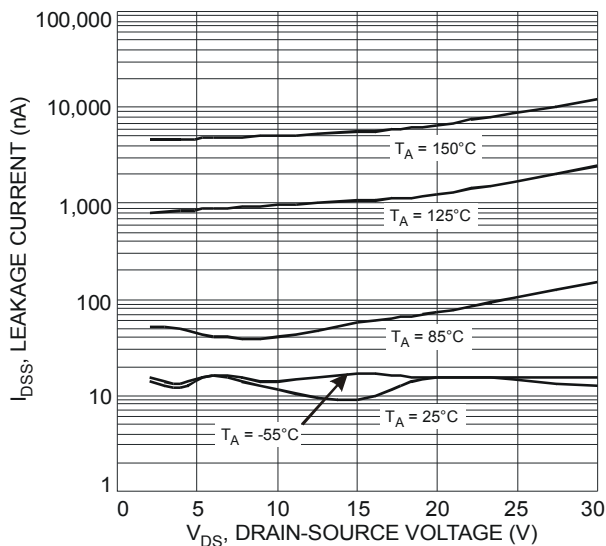


Fig. 11 Typical Leakage Current vs. Drain-Source Voltage

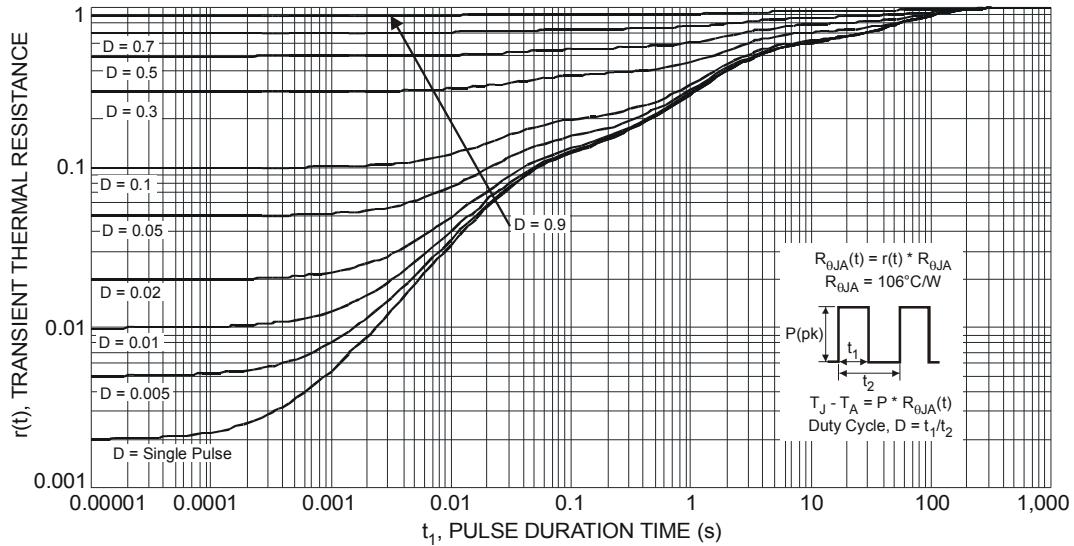
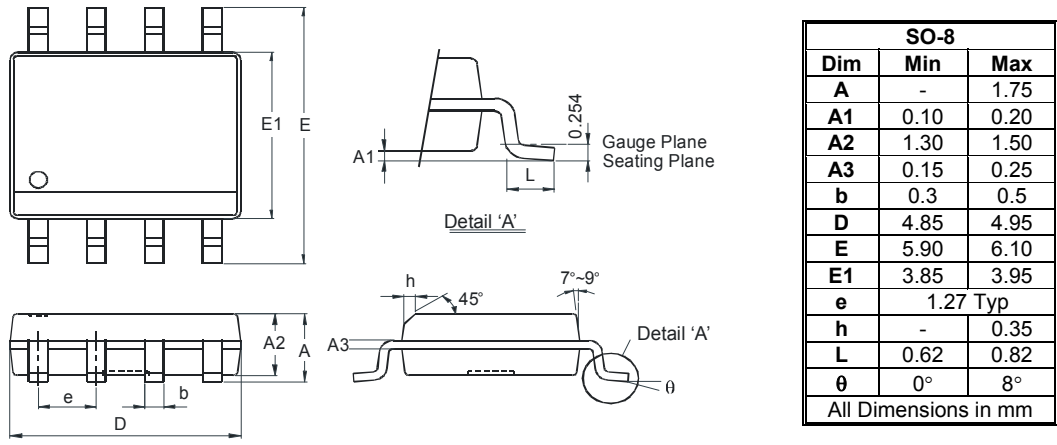
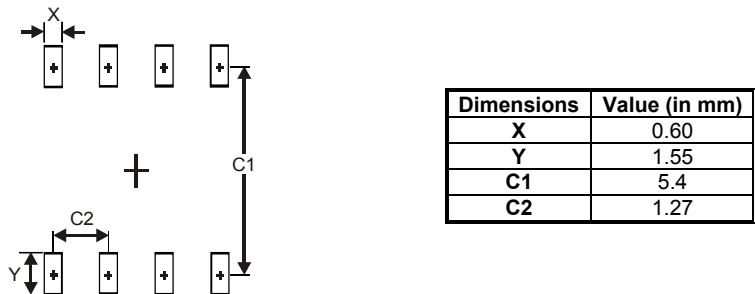


Fig. 12 Transient Thermal Response

Package Outline Dimensions



Suggested Pad Layout



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