

FDP8878

N-Channel Logic Level PowerTrench® MOSFET

30V, 40A, 15mΩ

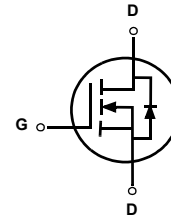
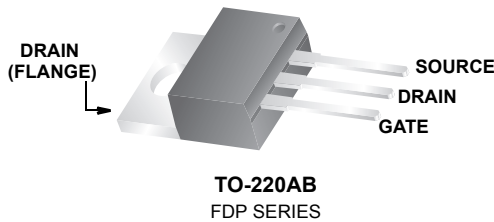
General Descriptions

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(ON)}$ and fast switching speed.



Features

- $r_{DS(ON)} = 15m\Omega$, $V_{GS} = 10V$, $I_D = 40A$
- $r_{DS(ON)} = 19m\Omega$, $V_{GS} = 4.5V$, $I_D = 36A$
- High performance trench technology for extremely low $r_{DS(ON)}$
- Low gate charge
- High power and current handling capability
- RoHS Compliant



MOSFET Maximum Ratings $T_A = 25^\circ C$ unless otherwise noted

Symbol	Parameter	Ratings	Units	
V_{DSS}	Drain to Source Voltage	30	V	
V_{GS}	Gate to Source Voltage	± 20	V	
I_D	Drain Current			
	Continuous ($T_C = 25^\circ C$, $V_{GS} = 10V$)	40	A	
	Continuous ($T_C = 25^\circ C$, $V_{GS} = 4.5V$)	36	A	
	Pulsed (Note 4)	141	A	
E_{AS}	Single Pulse Avalanche Energy (Note 1)	$L = 1mH, I_{AS} = 11A$	60	mJ
		$L = 43\mu H, I_{AS} = 32A$	22	
P_D	Power dissipation	40.5	W	
T_J, T_{STG}	Operating and Storage Temperature	-55 to 175	$^\circ C$	

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 2)	3.7	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient at 1000 seconds (Note 3)	43	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP8878	FDP8878	TO-220	Tube	n/a	45 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

B_{VDSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$	30	-	-	V
$\frac{\Delta B_{VDSS}}{\Delta T_J}$	Breakdown Voltage Temp. Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C		21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{V}$ $V_{GS} = 0\text{V}$ $T_A = 150^\circ\text{C}$	-	-	1 250	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(TH)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	1.2	1.7	2.5	V
$\frac{\Delta V_{GS(TH)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C		-5		mV/°C
$r_{DS(ON)}$	Drain to Source On Resistance	$I_D = 40\text{A}, V_{GS} = 10\text{V}$	-	12	15	m Ω
		$I_D = 36\text{A}, V_{GS} = 4.5\text{V}$	-	16	19	
		$I_D = 40\text{A}, V_{GS} = 10\text{V}$, $T_A = 175^\circ\text{C}$	-	20	25	

Dynamic Characteristics

C_{ISS}	Input Capacitance	$V_{DS} = 15\text{V}, V_{GS} = 0\text{V}$, $f = 1\text{MHz}$	-	927	1235	pF	
C_{OSS}	Output Capacitance		-	188	250	pF	
C_{RSS}	Reverse Transfer Capacitance		-	1130	175	pF	
R_G	Gate Resistance	$f = 1\text{MHz}$		3.0		Ω	
$Q_{g(TOT)}$	Total Gate Charge at 10V	$V_{GS} = 0\text{V}$ to 10V	$V_{DD} = 15\text{V}$ $I_D = 40\text{A}$ $I_g = 1.0\text{mA}$	-	17.1	23	nC
$Q_{g(5)}$	Total Gate Charge at 5V	$V_{GS} = 0\text{V}$ to 5V		-	9.2	12	nC
Q_{gs}	Gate to Source Gate Charge			-	2.6	-	nC
Q_{gs2}	Gate Charge Threshold to Plateau			-	1.7	-	nC
Q_{gd}	Gate to Drain "Miller" Charge			-	3.7	-	nC

Switching Characteristics ($V_{GS} = 10\text{V}$)

t_{ON}	Turn-On Time	$V_{DD} = 15\text{V}, I_D = 40\text{A}$ $V_{GS} = 10\text{V}, R_{GS} = 16\Omega$	-	255	383	ns
$t_{d(ON)}$	Turn-On Delay Time		-	11.1		ns
t_r	Rise Time		-	244		ns
$t_{d(OFF)}$	Turn-Off Delay Time		-	14.8		ns
t_f	Fall Time		-	35.3		ns
t_{OFF}	Turn-Off Time		-	50	75	ns

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Voltage	$I_{SD} = 40\text{A}$	-	1.1	1.25	V
		$I_{SD} = 3.2\text{A}$	-	0.85	1.2	V
t_{rr}	Reverse Recovery Time	$I_{SD} = 40\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	14.4	18.8	ns
Q_{RR}	Reverse Recovered Charge	$I_{SD} = 40\text{A}, dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	5.1	6.7	nC

Notes:

- 1: Starting $T_J = 25^\circ\text{C}$, $V_{DD} = 30\text{V}$, $V_{GS} = 10\text{V}$
- 2: $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.
- 3: $R_{\theta JA}$ is measured with 1.0 in² copper on FR-4 board
- 4: Pulse Test: Pulse Width < 300 μs , Duty Cycle < 2.0%

Typical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

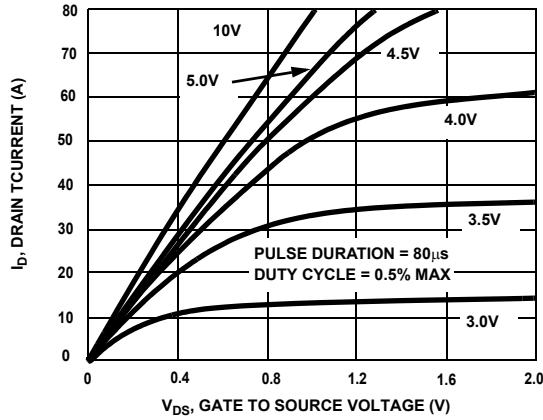


Figure 1. On Region Characteristics

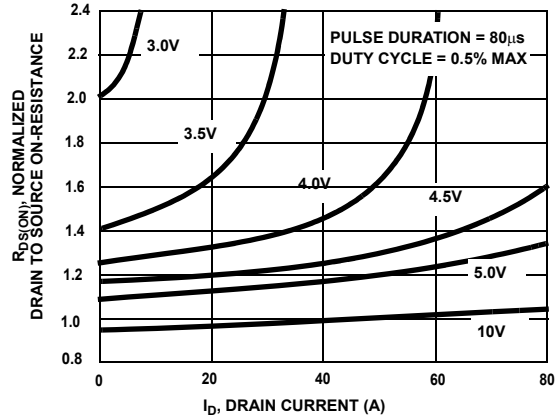


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

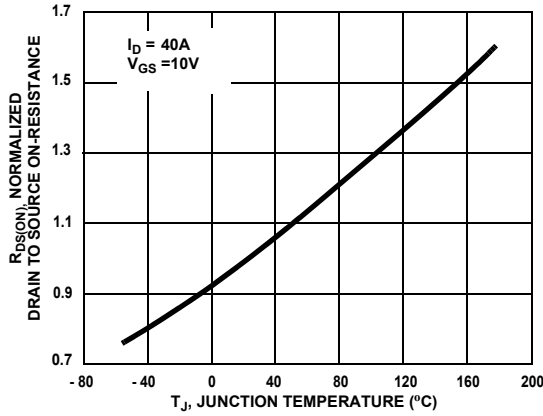


Figure 3. On Resistance Variation with Temperature

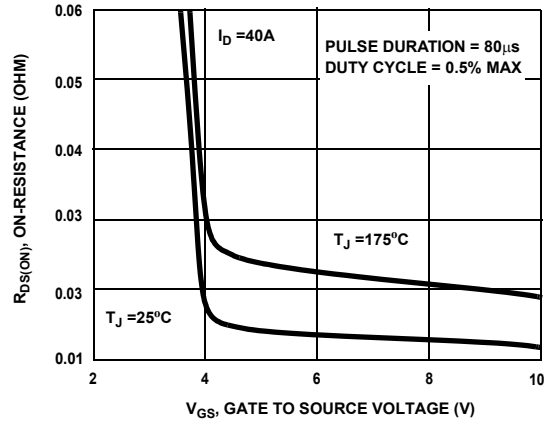


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

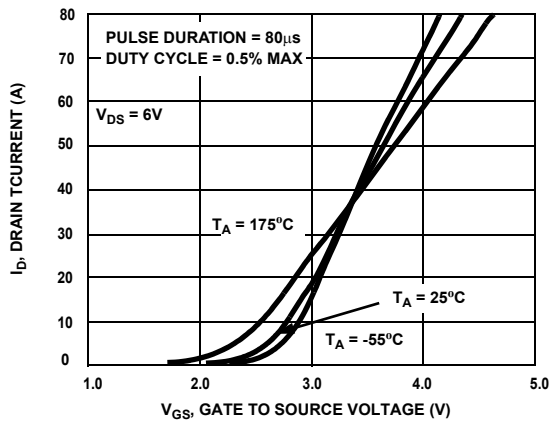


Figure 5. Transfer Characteristics

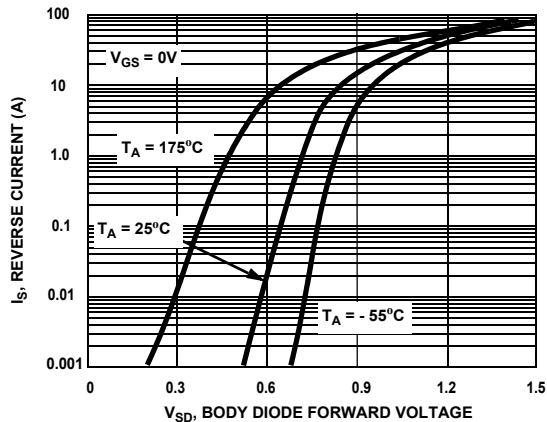


Figure 6. Body Diode Forward Voltage Variation With Source Current and Temperature

Typical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

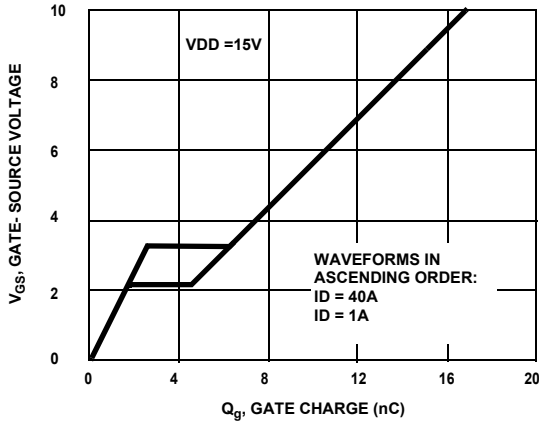


Figure 7. Gate Charge Characteristics

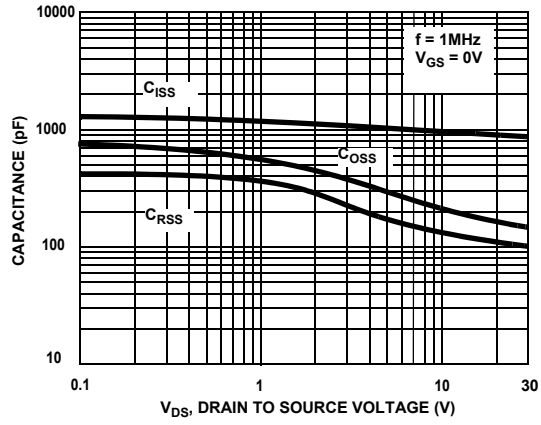


Figure 8. Capacitance Characteristics

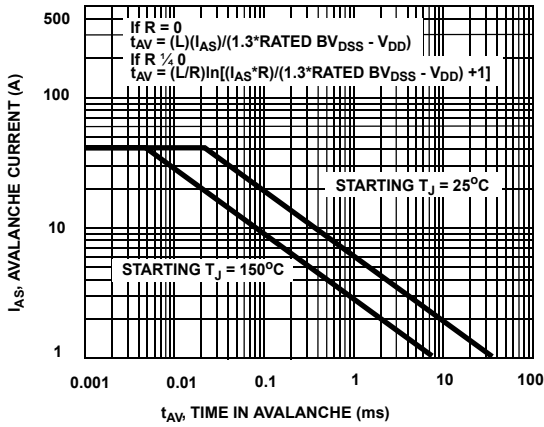


Figure 9. Unclamped Inductive Switching Capability

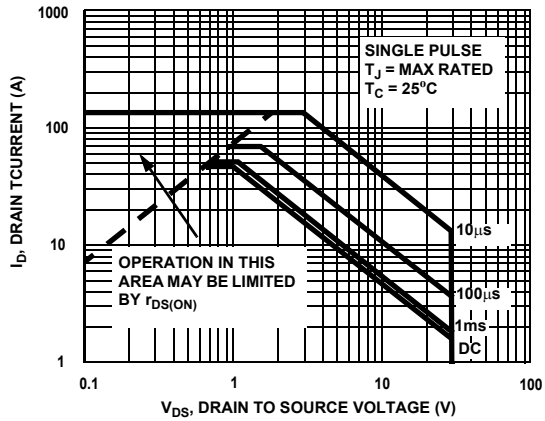


Figure 10. Safe Operating Area

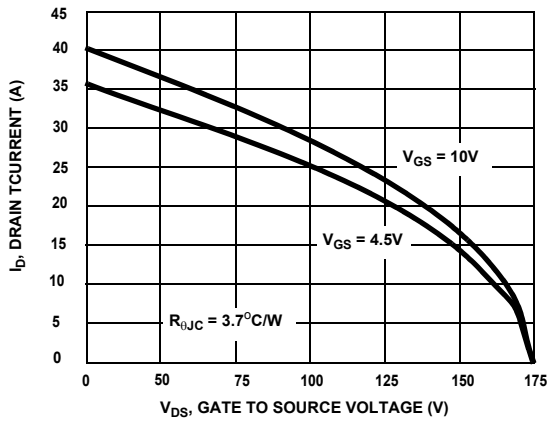


Figure 11. Maximum Continuous Drain Current vs Case Temperature

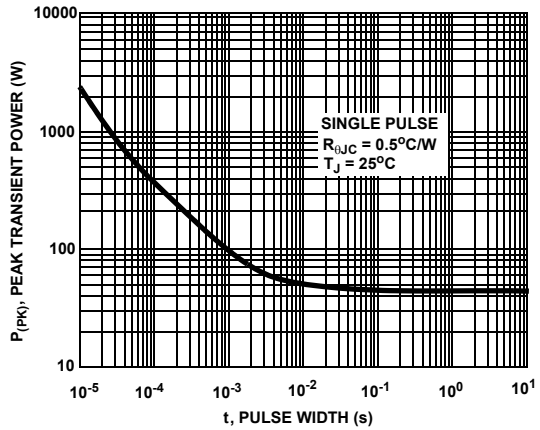


Figure 12. Single Pulse Maximum Power Dissipation

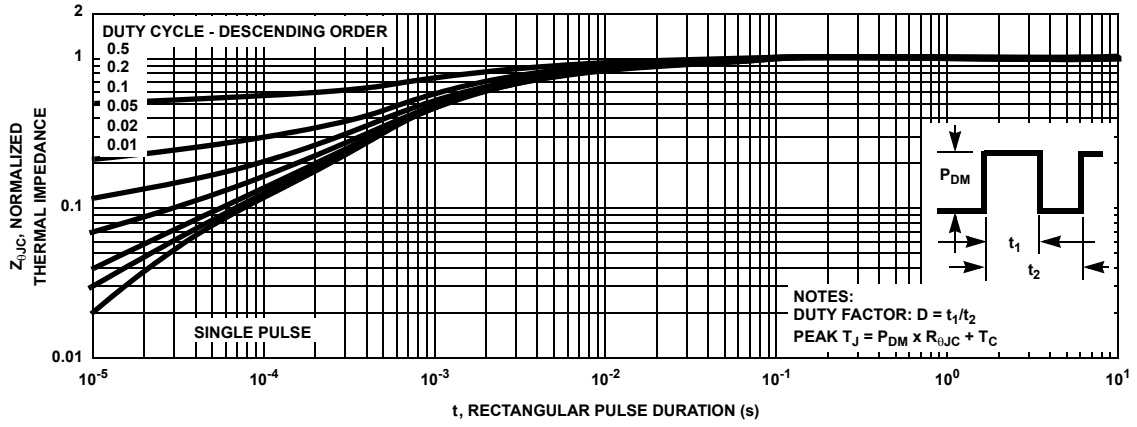


Figure 13. Transient Thermal Response Curve

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