

# FDR836P

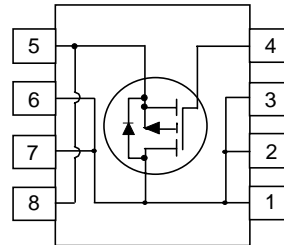
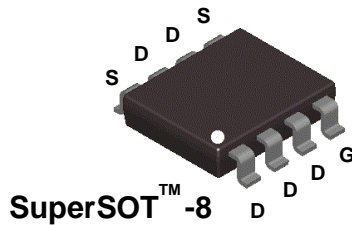
## P-Channel 2.5V Specified MOSFET

### General Description

SuperSOT™ -8 P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as battery powered circuits or portable electronics where low in-line power loss, fast switching and resistance to transients are needed.

### Features

- -6.1 A, -20 V.  $R_{DS(ON)} = 0.030 \Omega @ V_{GS} = -4.5 \text{ V}$   
 $R_{DS(ON)} = 0.040 \Omega @ V_{GS} = -2.5 \text{ V}$
- High density cell design for extremely low  $R_{DS(ON)}$ .
- Small footprint (38% smaller than a standard SO-8); low profile package (1 mm thick); power handling capability similar to SO-8.



### Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	-20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 8$	V
$I_D$	Drain Current - Continuous (Note 1a) - Pulsed	-6.1	A
		-18	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	1.8	W
		1.0	
		0.9	
$T_J, T_{stg}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	70	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	20	$^\circ\text{C/W}$

### Package Outlines and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
.836P	FDR836P	13"	12mm	3000 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-24		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 8\text{ V}, V_{DS} = 0\text{ V}$			100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -8\text{ V}, V_{DS} = 0\text{ V}$			-100	nA

## On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.6	-1	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}, I_D = -6.1\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -6.1\text{ A}, T_J = 125^\circ\text{C}$ $V_{GS} = -2.5\text{ V}, I_D = -5\text{ A}$		0.022 0.031 0.029	0.030 0.048 0.040	$\Omega$
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -4.5\text{ V}, V_{DS} = -5\text{ V}$	-9			A
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -6.1\text{ A}$		22		S

## Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2200		pF
$C_{oss}$	Output Capacitance			570		pF
$C_{rss}$	Reverse Transfer Capacitance			140		pF

## Switching Characteristics (Note 2)

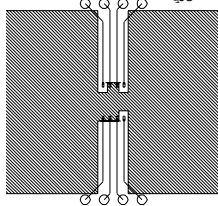
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$		10	18	ns
$t_r$	Turn-On Rise Time			14	25	ns
$t_{d(off)}$	Turn-Off Delay Time			225	360	ns
$t_f$	Turn-Off Fall Time			85	135	ns
$Q_g$	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -6.1\text{ A},$ $V_{GS} = -4.5\text{ V}$		32	44	nC
$Q_{gs}$	Gate-Source Charge			3.2		nC
$Q_{gd}$	Gate-Drain Charge			8.1		nC

## Drain-Source Diode Characteristics and Maximum Ratings

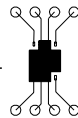
$I_S$	Maximum Continuous Drain-Source Diode Forward Current			-1.5		A
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.5\text{ A}$ (Note 2)		-0.65	-1.2	V

### Notes:

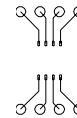
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $70^\circ\text{C/W}$  when mounted on a  $1.0\text{ in}^2$  pad of 2 oz. copper.



b)  $125^\circ\text{C/W}$  when mounted on a  $0.026\text{ in}^2$  pad of 2oz. copper.



c)  $135^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $\leq 300\text{ ms}$ , Duty Cycle  $\leq 2.0\%$

Typical Characteristics

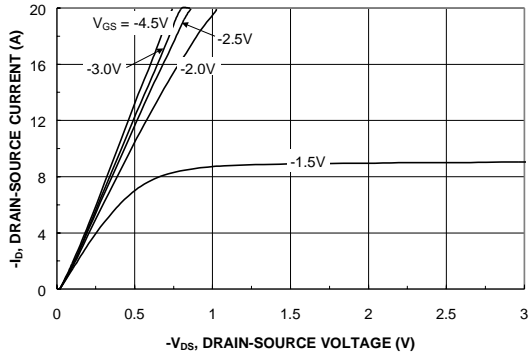


Figure 1. On-Region Characteristics.

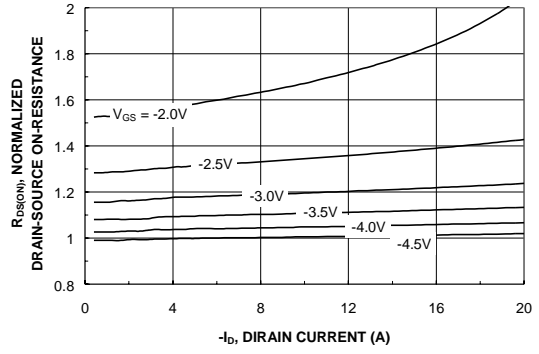


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

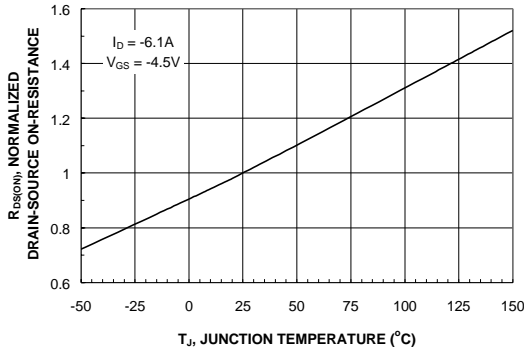


Figure 3. On-Resistance Variation with Temperature.

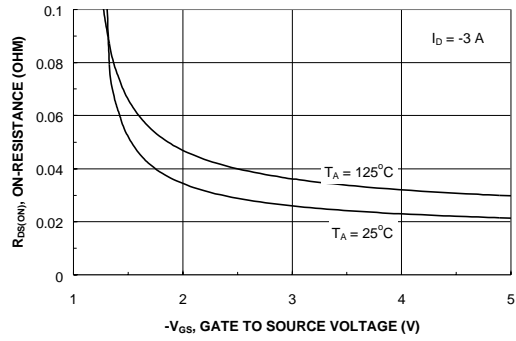


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

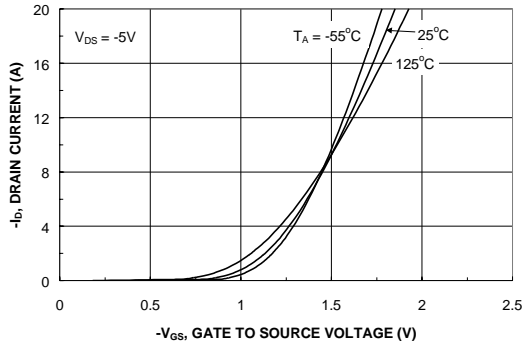


Figure 5. Transfer Characteristics.

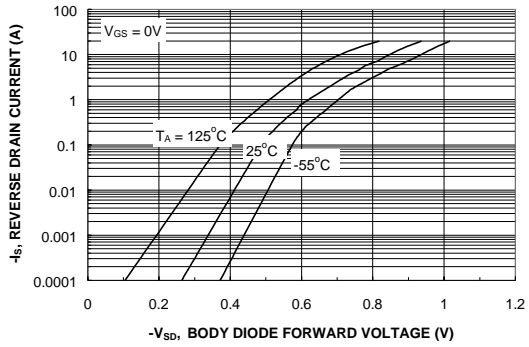


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics (continued)

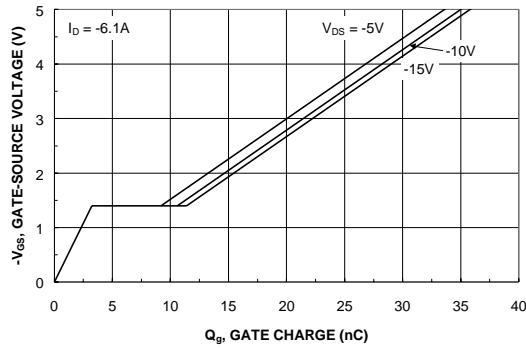


Figure 7. Gate-Charge Characteristics.

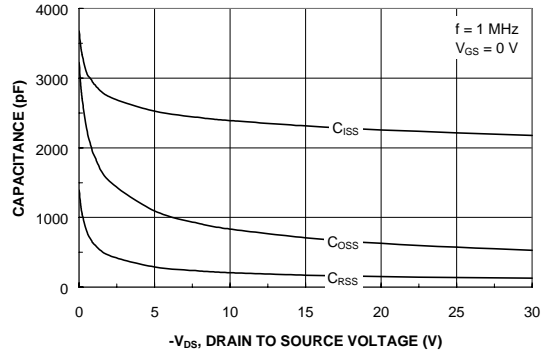


Figure 8. Capacitance Characteristics.

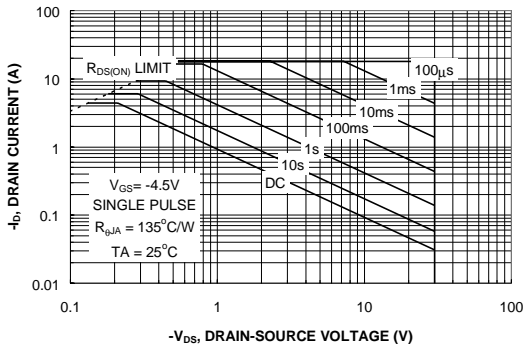


Figure 9. Maximum Safe Operating Area.

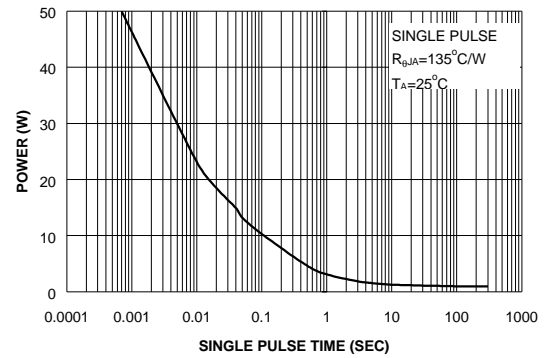


Figure 10. Single Pulse Maximum Power Dissipation.

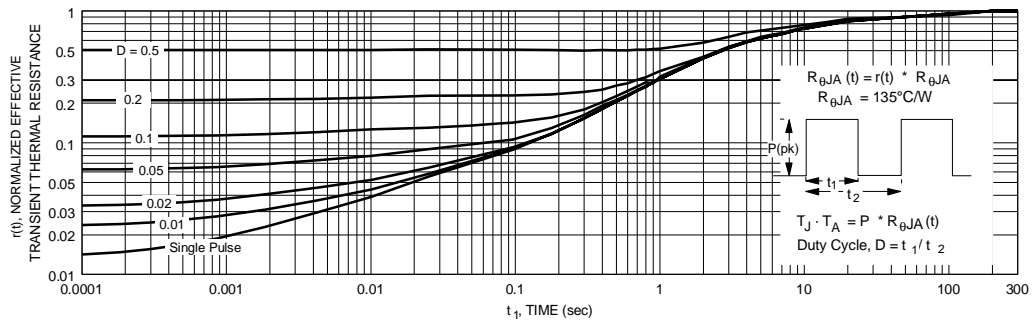


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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