

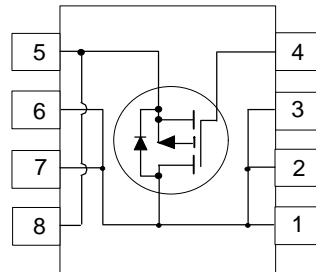
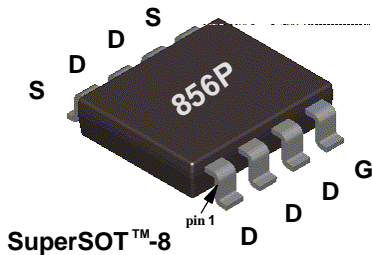
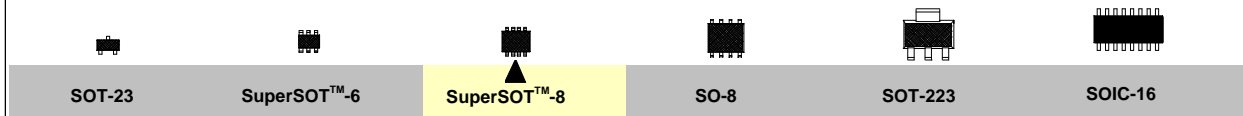
FDR856P P-Channel Logic Level Enhancement Mode Field Effect Transistor

General Description

SuperSOT™-8 P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as battery powered circuits or portable electronics where low in-line power loss, fast switching and resistance to transients are needed.

Features

- 6.3 A, -30 V, $R_{DS(ON)} = 0.025 \Omega @ V_{GS} = -10 \text{ V}$
 $R_{DS(ON)} = 0.040 \Omega @ V_{GS} = -4.5 \text{ V}$.
- SuperSOT™-8 package:
small footprint (40% less than SO-8); low profile (1mm thick); maximum power comparable to SO-8.
- High density cell design for extremely low $R_{DS(ON)}$.



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

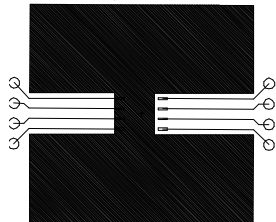
Symbol	Parameter	FDR856P	Units
V_{DSS}	Drain-Source Voltage	-30	V
V_{GSS}	Gate-Source Voltage - Continuous	± 20	V
I_D	Maximum Drain Current - Continuous (Note 1a)	-5.1	A
	- Pulsed	-50	
P_D	Maximum Power Dissipation (Note 1a)	1.8	W
	(Note 1b)	1	
	(Note 1c)	0.9	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
THERMAL CHARACTERISTICS			
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

Electrical Characteristics ($T_A = 25\text{ }^\circ\text{C}$ unless otherwise noted)

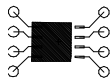
Symbol	Parameter	Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-30			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$		-15		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	μA
		$T_J = 55\text{ }^\circ\text{C}$			-10	μA
I_{GSSF}	Gate - Body Leakage, Forward	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
I_{GSSR}	Gate - Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$			-100	nA
ON CHARACTERISTICS (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\text{ }\mu\text{A}$	-1	-1.5	-3	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Temp. Coefficient	$I_D = -250\text{ }\mu\text{A}$, Referenced to $25\text{ }^\circ\text{C}$		3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -6.3\text{ A}$		0.022	0.025	Ω
		$T_J = 125\text{ }^\circ\text{C}$		0.03	0.042	
		$V_{GS} = -4.5\text{ V}, I_D = -5\text{ A}$		0.033	0.04	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	-50			A
g_{FS}	Forward Transconductance	$V_{DS} = -10\text{ V}, I_D = -6.3\text{ A}$		15		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		1370		pF
C_{oss}	Output Capacitance			740		pF
C_{rss}	Reverse Transfer Capacitance			220		pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{D(on)}$	Turn - On Delay Time	$V_{DS} = -15\text{ V}, I_D = -1\text{ A}$ $V_{GS} = -10\text{ V}, R_G = 6\text{ }\Omega$		7	14	ns
t_r	Turn - On Rise Time			12	19	
$t_{D(off)}$	Turn - Off Delay Time			80	100	
t_f	Turn - Off Fall Time			130	160	
Q_g	Total Gate Charge	$V_{DS} = -15\text{ V}, I_D = -6.3\text{ A},$ $V_{GS} = -10\text{ V}$		22	31	nC
Q_{gs}	Gate-Source Charge			3.8		
Q_{gd}	Gate-Drain Charge			8.7		
DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain-Source Diode Forward Current				-1.3	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2)		-0.73	-1.2	V

Notes:

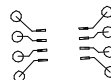
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50\text{ }^\circ\text{C/W}$ on a 0.5 in^2 pad of 2oz copper.



b. $105\text{ }^\circ\text{C/W}$ on a 0.02 in^2 pad of 2oz copper.



c. $125\text{ }^\circ\text{C/W}$ on a 0.003 in^2 pad of 2oz copper.

Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2.0\%$.

Typical Electrical Characteristics

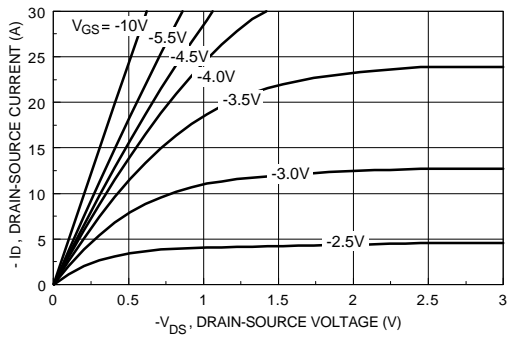


Figure 1. On-Region Characteristics.

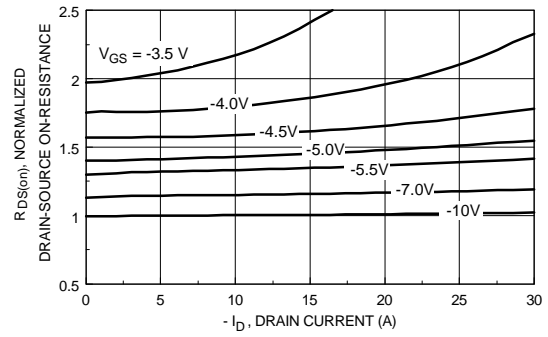


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

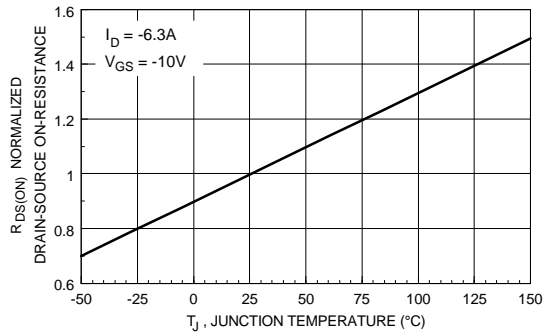


Figure 3. On-Resistance Variation with Temperature.

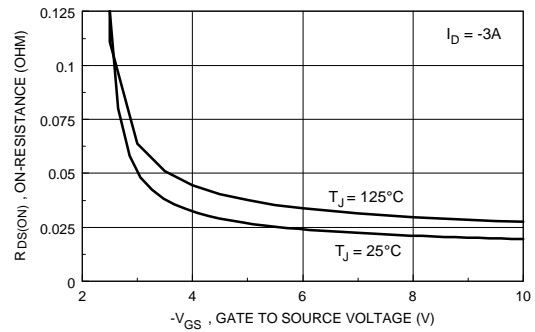


Figure 4. On Resistance Variation with Gate-to-Source Voltage.

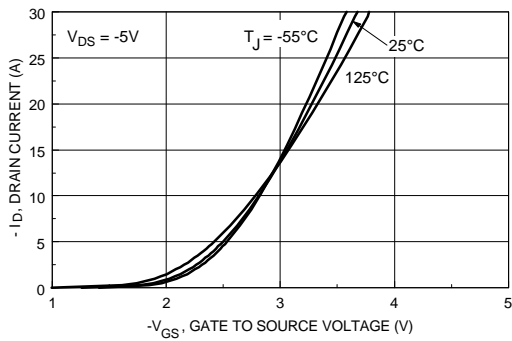


Figure 5. Transfer Characteristics.

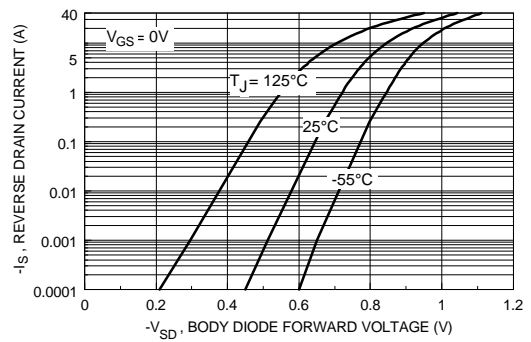


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Electrical Characteristics (continued)

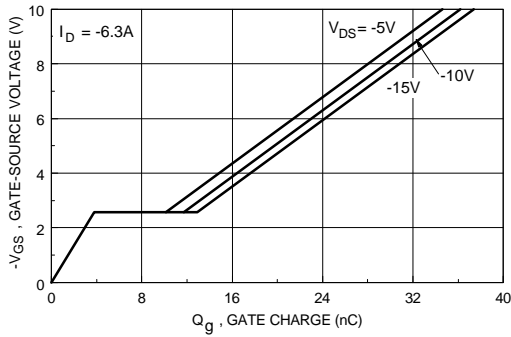


Figure 7. Gate Charge Characteristics.

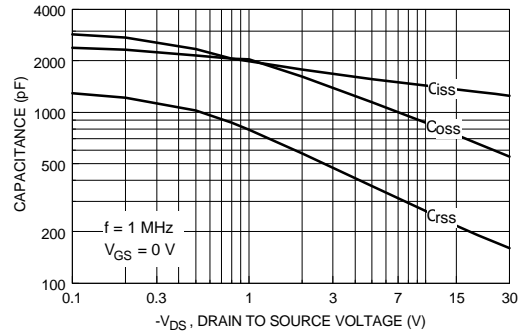


Figure 8. Capacitance Characteristics.

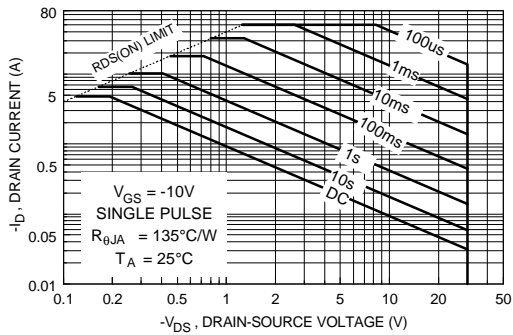


Figure 9. Maximum Safe Operating Area.

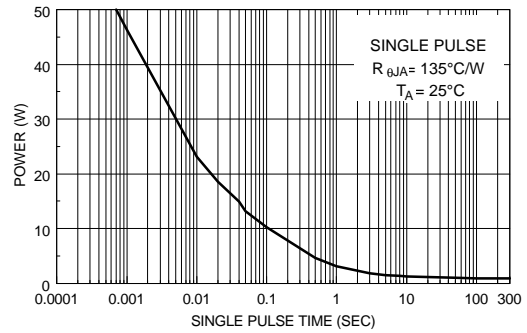


Figure 10. Single Pulse Maximum Power Dissipation.

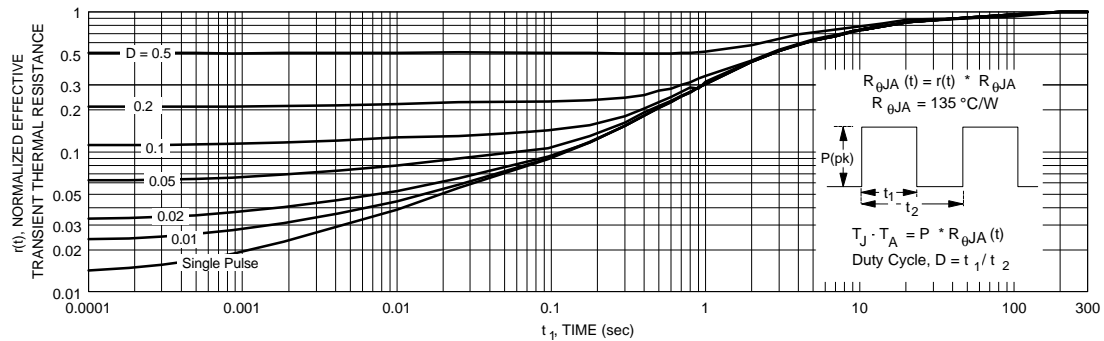


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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