

# FDS4141

## P-Channel PowerTrench® MOSFET

-40V, -10.8A, 13.0mΩ

### Features

- Max  $r_{DS(on)}$  = 13.0mΩ at  $V_{GS} = -10V$ ,  $I_D = -10.5A$
- Max  $r_{DS(on)}$  = 19.0mΩ at  $V_{GS} = -4.5V$ ,  $I_D = -8.4A$
- High performance trench technology for extremely low  $r_{DS(on)}$
- RoHS Compliant

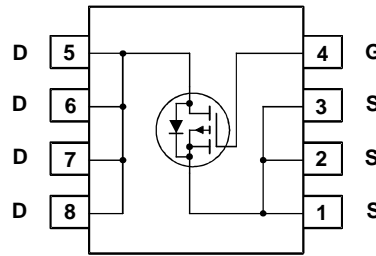
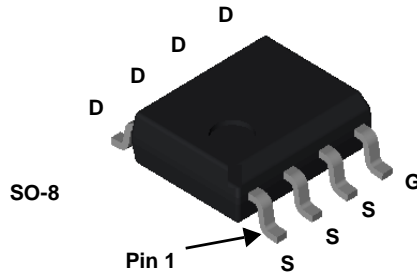


### General Description

This P-Channel MOSFET has been produced using Fairchild Semiconductor's proprietary PowerTrench® technology to deliver low  $r_{DS(on)}$  and optimized  $BV_{DSS}$  capability to offer superior performance benefit in the applications and optimized switching performance capability reducing power dissipation losses in converter/inverter applications.

### Applications

- Control switch in synchronous & non-synchronous buck
- Load switch
- Inverter



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	-40	V
$V_{GS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current -Continuous	-10.8	A
	-Pulsed	-36	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	294	mJ
$P_D$	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	5	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1b)	2.5	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS4141	FDS4141	SO-8	13"	12mm	2500units

## Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		-33		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -32\text{V}$ ,			-1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1.0	-1.6	-3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$ , referenced to $25^\circ\text{C}$		5.3		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{V}, I_D = -10.5\text{A}$		11.0	13.0	m $\Omega$
		$V_{GS} = -4.5\text{V}, I_D = -8.4\text{A}$		15.2	19.0	
		$V_{GS} = -10\text{V}, I_D = -10.5\text{A}, T_J = 125^\circ\text{C}$		16.8	19.9	
$g_{FS}$	Forward Transconductance	$V_{DD} = -5\text{V}, I_D = -10.5\text{A}$		37		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V},$ $f = 1\text{MHz}$		2005	2670	pF
$C_{oss}$	Output Capacitance			355	475	pF
$C_{rss}$	Reverse Transfer Capacitance			190	285	pF
$R_g$	Gate Resistance		$f = 1\text{MHz}$	5		$\Omega$

### Switching Characteristics

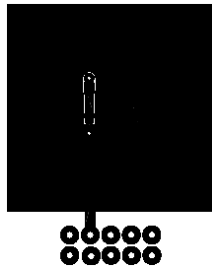
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -20\text{V}, I_D = -10.5\text{A},$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$		10	20	ns	
$t_r$	Rise Time			5	10	ns	
$t_{d(off)}$	Turn-Off Delay Time			42	68	ns	
$t_f$	Fall Time			12	22	ns	
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{V to } -10\text{V}$		35	49	nC
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{V to } -5\text{V}$	$V_{DD} = -20\text{V},$ $I_D = -10.5\text{A}$	19	27	nC
$Q_{gs}$	Gate to Source Charge			6		nC	
$Q_{gd}$	Gate to Drain "Miller" Charge			7		nC	

### Drain-Source Diode Characteristics

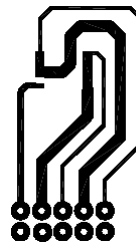
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -10.5\text{A}$ (Note 2)		-0.8	-1.3	V
		$V_{GS} = 0\text{V}, I_S = -2.1\text{A}$ (Note 2)		-0.7	-1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = -10.5\text{A}, di/dt = 100\text{A}/\mu\text{s}$		26	42	ns
$Q_{rr}$	Reverse Recovery Charge			14	26	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a  $1\text{in}^2$  pad 2 oz copper pad on a  $1.5 \times 1.5\text{in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  when mounted on a  $1\text{in}^2$  pad of 2 oz copper.

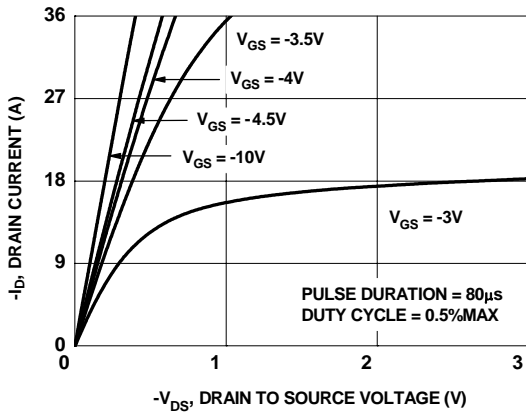


b)  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

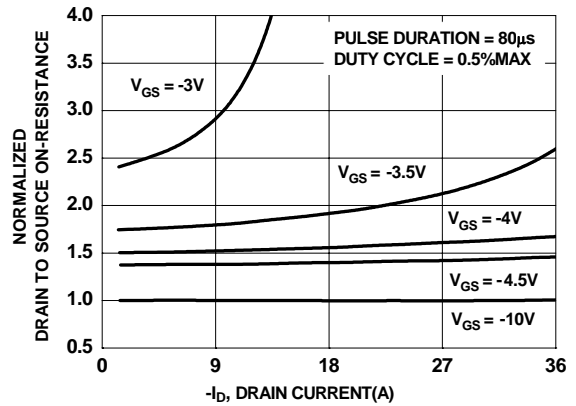
2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty cycle < 2.0%.

3. UIL condition: Starting  $T_J = 25^\circ\text{C}$ ,  $L = 3\text{mH}$ ,  $I_{AS} = -14\text{A}$ ,  $V_{DD} = -40\text{V}$ ,  $V_{GS} = -10\text{V}$ .

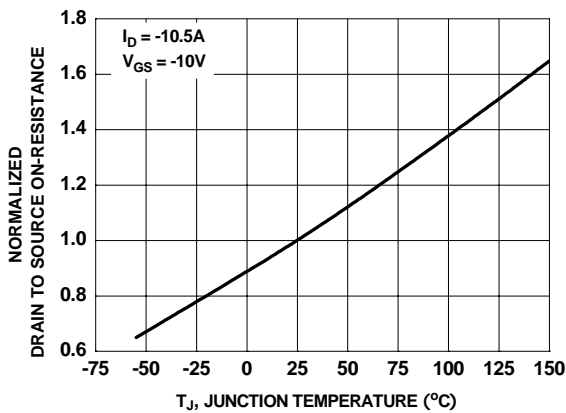
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



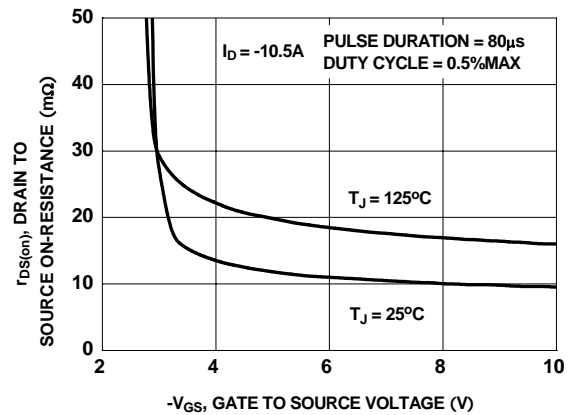
**Figure 1. On-Region Characteristics**



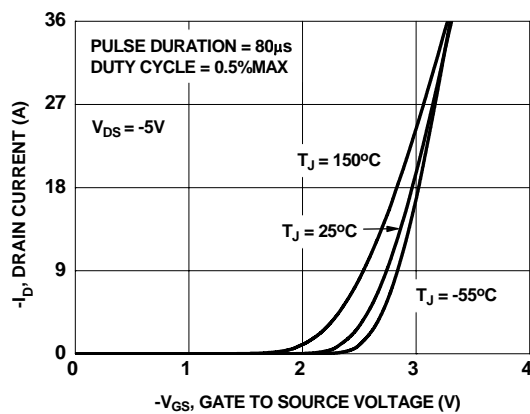
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



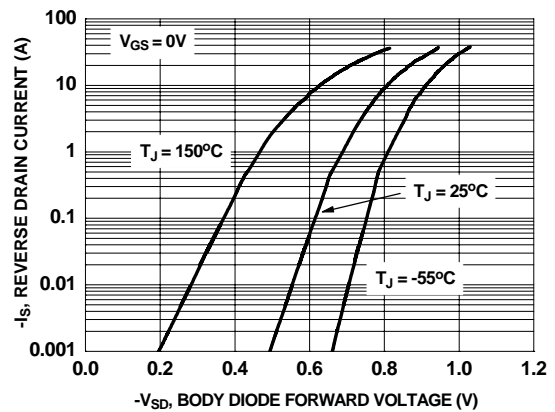
**Figure 3. Normalized On-Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

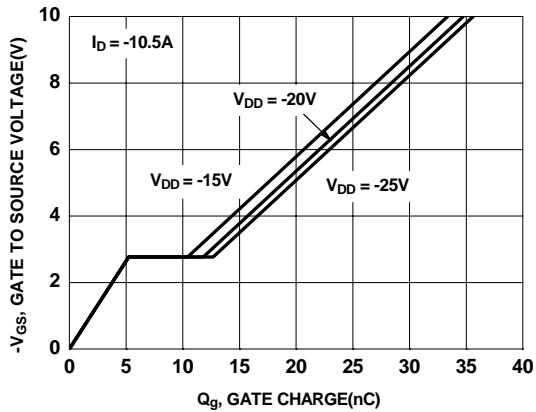


**Figure 5. Transfer Characteristics**

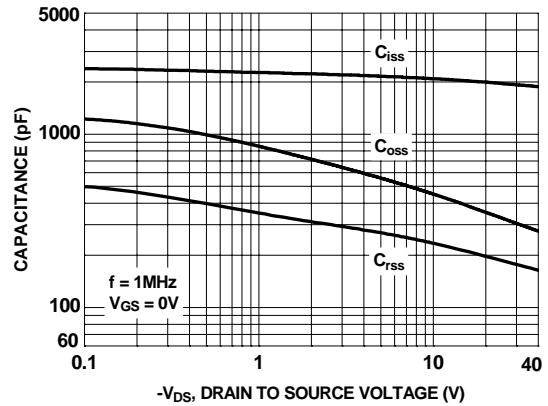


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

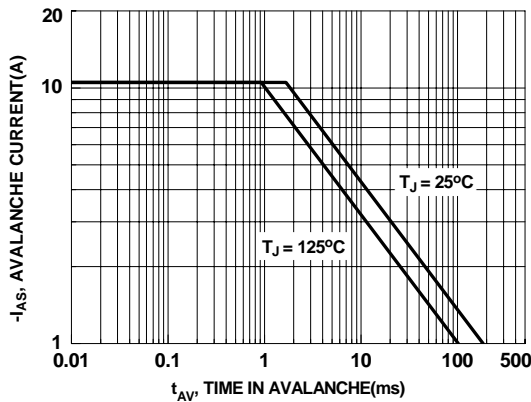
**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



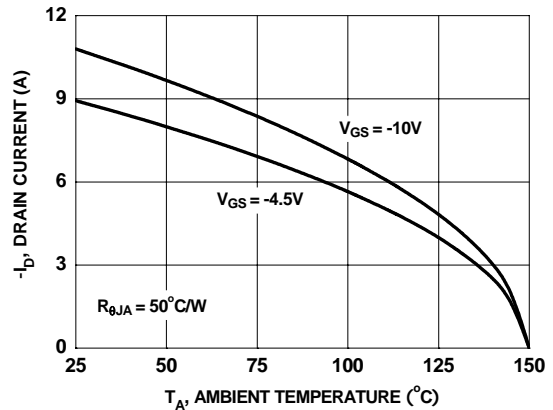
**Figure 7. Gate Charge Characteristics**



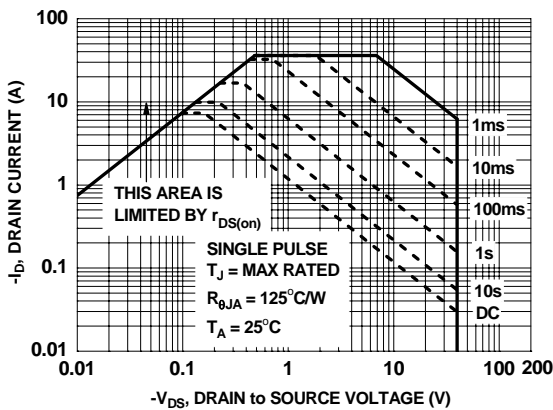
**Figure 8. Capacitance vs Drain to Source Voltage**



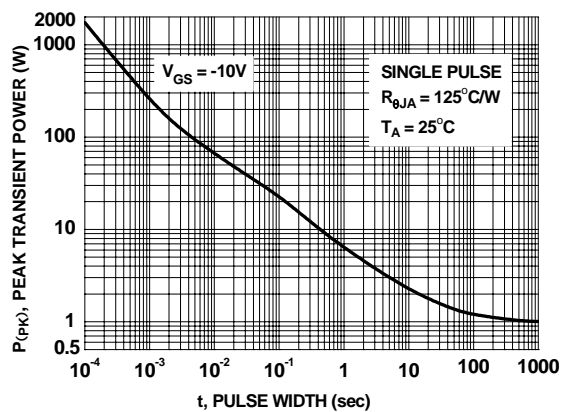
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

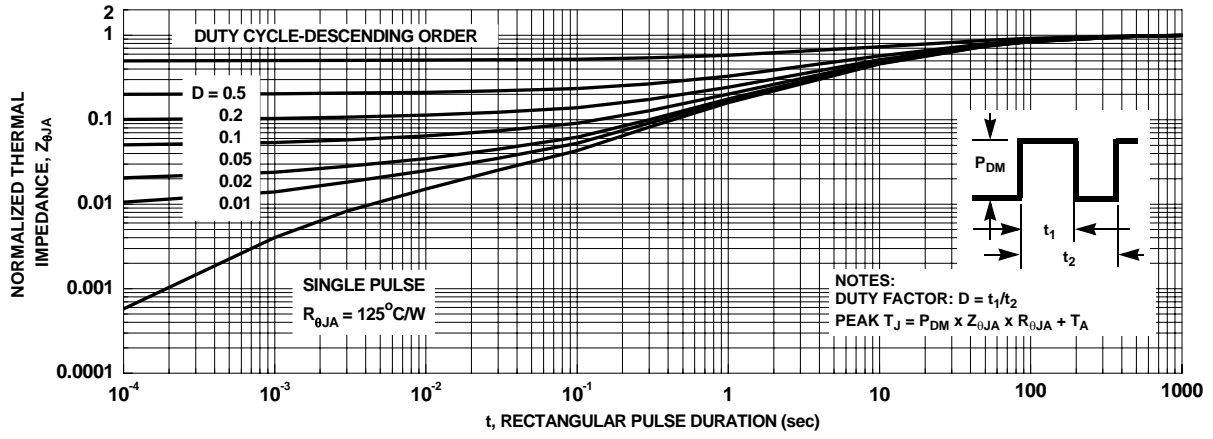


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25^\circ\text{C}$  unless otherwise noted



**Figure 13. Transient Thermal Response Curve**



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