

# FDC6333C

## 30V N & P-Channel PowerTrench<sup>®</sup> MOSFETs

### General Description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

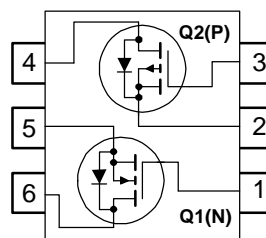
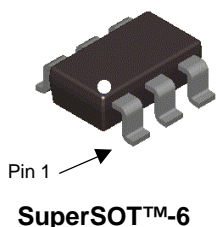
These devices have been designed to offer exceptional power dissipation in a very small footprint for applications where the bigger more expensive SO-8 and TSSOP-8 packages are impractical.

### Applications

- DC/DC converter
- Load switch
- LCD display inverter

### Features

- **Q1** 2.5 A, 30V.  $R_{DS(ON)} = 95\text{ m}\Omega @ V_{GS} = 10\text{ V}$   
 $R_{DS(ON)} = 150\text{ m}\Omega @ V_{GS} = 4.5\text{ V}$
- **Q2** -2.0 A, 30V.  $R_{DS(ON)} = 150\text{ m}\Omega @ V_{GS} = -10\text{ V}$   
 $R_{DS(ON)} = 220\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- Low gate charge
- High performance trench technology for extremely low  $R_{DS(ON)}$ .
- SuperSOT -6 package: small footprint (72% smaller than SO-8); low profile (1mm thick).



### Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V <sub>DSS</sub>	Drain-Source Voltage	30	-30	V
V <sub>GSS</sub>	Gate-Source Voltage	±16	±25	V
I <sub>D</sub>	Drain Current – Continuous (Note 1a)	2.5	-2.0	A
	– Pulsed	8	-8	
P <sub>D</sub>	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	0.96		W
		0.9		
		0.7		
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range	-55 to +150		°C

### Thermal Characteristics

R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient (Note 1a)	130	°C/W
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case (Note 1)	60	°C/W

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.333	FDC6333C	7"	8mm	3000 units

## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ $V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	<b>Q1</b> <b>Q2</b>	30 –30		V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$ $I_D = -250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$	<b>Q1</b> <b>Q2</b>		27 –22	mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	<b>Q1</b> <b>Q2</b>		1 –1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 16\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	<b>Q1</b> <b>Q2</b>		100 100	nA
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -16\text{ V}, V_{DS} = 0\text{ V}$ $V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	<b>Q1</b> <b>Q2</b>		–100 –100	nA

### On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	<b>Q1</b>	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1	1.8	3	V
		<b>Q2</b>	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	–1	–1.8	–3	
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	<b>Q1</b>	$I_D = 250\ \mu\text{A}, \text{Ref. To } 25^\circ\text{C}$		4		mV/°C
		<b>Q2</b>	$I_D = -250\ \mu\text{A}, \text{Ref. to } 25^\circ\text{C}$		–4		
$R_{DS(on)}$	Static Drain–Source On–Resistance	<b>Q1</b>	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 2.0\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}, T_J = 125^\circ\text{C}$		73 90 106	95 150 148	m $\Omega$
		<b>Q2</b>	$V_{GS} = -10\text{ V}, I_D = -2.0\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -1.7\text{ A}$ $V_{GS} = 10\text{ V}, I_D = -2.0\text{ A}, T_J = 125^\circ\text{C}$		95 142 149	130 220 216	
$I_{D(on)}$	On–State Drain Current	<b>Q1</b>	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	8			A
		<b>Q2</b>	$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	–8			
$g_{FS}$	Forward Transconductance	<b>Q1</b>	$V_{DS} = 5\text{ V}, I_D = 2.5\text{ A}$		7		S
		<b>Q2</b>	$V_{DS} = -5\text{ V}, I_D = -2.0\text{ A}$		3		

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	<b>Q1</b>	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{MHz}$		282		pF
		<b>Q2</b>	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{MHz}$		185		
$C_{oss}$	Output Capacitance	<b>Q1</b>	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{MHz}$		49		pF
		<b>Q2</b>	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{MHz}$		56		
$C_{riss}$	Reverse Transfer Capacitance	<b>Q1</b>	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{MHz}$		20		pF
		<b>Q2</b>	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{MHz}$		26		

### Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	<b>Q1</b>	For <b>Q1</b> : $V_{DS} = 15\text{ V}, I_{DS} = 1\text{ A}$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		4.5	9	ns
		<b>Q2</b>			4.5	9	
$t_r$	Turn–On Rise Time	<b>Q1</b>	For <b>Q2</b> : $V_{DS} = -15\text{ V}, I_{DS} = -1\text{ A}$ $V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		6	12	ns
		<b>Q2</b>			13	23	
$t_{d(off)}$	Turn–Off Delay Time	<b>Q1</b>			19	34	ns
		<b>Q2</b>			11	20	
$t_f$	Turn–Off Fall Time	<b>Q1</b>			1.5	3	ns
		<b>Q2</b>			2	4	
$Q_g$	Total Gate Charge	<b>Q1</b>	For <b>Q1</b> : $V_{DS} = 15\text{ V}, I_{DS} = 2.5\text{ A}$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$		4.7	6.6	nC
		<b>Q2</b>			4.1	5.7	
$Q_{gs}$	Gate–Source Charge	<b>Q1</b>	For <b>Q2</b> : $V_{DS} = -15\text{ V}, I_{DS} = -2.0\text{ A}$ $V_{GS} = -10\text{ V}$		0.9		nC
		<b>Q2</b>			0.8		
$Q_{gd}$	Gate–Drain Charge	<b>Q1</b>			0.6		nC
		<b>Q2</b>			0.4		

### Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

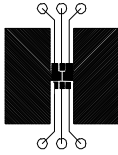
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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#### Drain–Source Diode Characteristics and Maximum Ratings

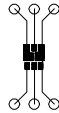
$I_S$	Maximum Continuous Drain–Source Diode Forward Current	Q1			0.8	A	
		Q2			-0.8		
$V_{SD}$	Drain–Source Diode Forward Voltage	Q1	$V_{GS} = 0\text{ V}, I_S = 0.8\text{ A}$	(Note 2)	0.8	1.2	V
		Q2	$V_{GS} = 0\text{ V}, I_S = 0.8\text{ A}$	(Note 2)	0.8	-1.2	

**Notes:**

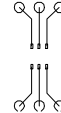
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a)  $130^\circ\text{C/W}$  when mounted on a  $0.125\text{ in}^2$  pad of 2 oz. copper.



- b)  $140^\circ\text{C/W}$  when mounted on a  $.004\text{ in}^2$  pad of 2 oz copper



- c)  $180^\circ\text{C/W}$  when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

## Typical Characteristics: N-Channel

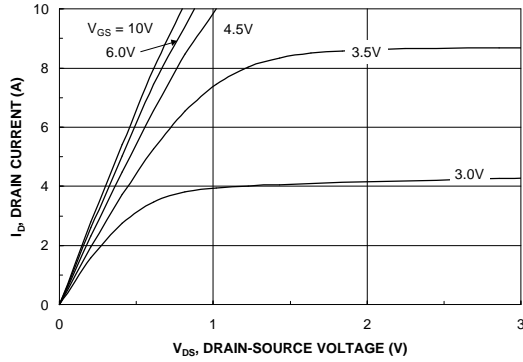


Figure 1. On-Region Characteristics.

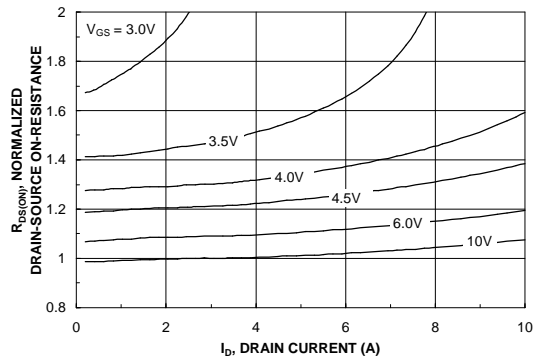


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

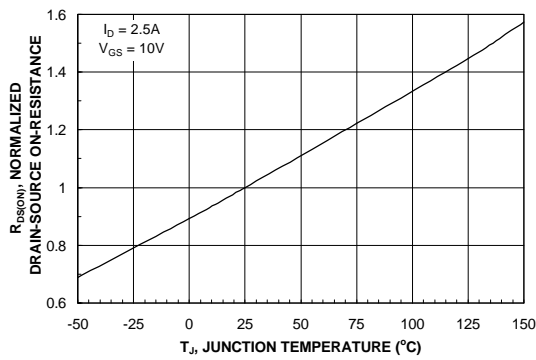


Figure 3. On-Resistance Variation with Temperature.

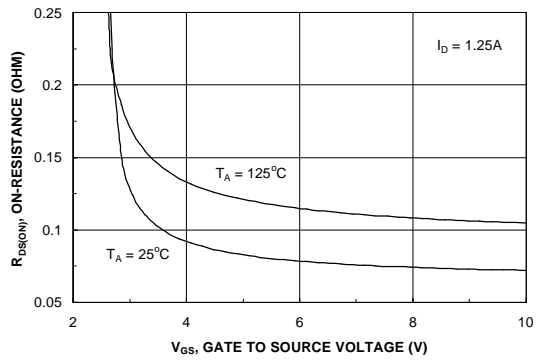


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

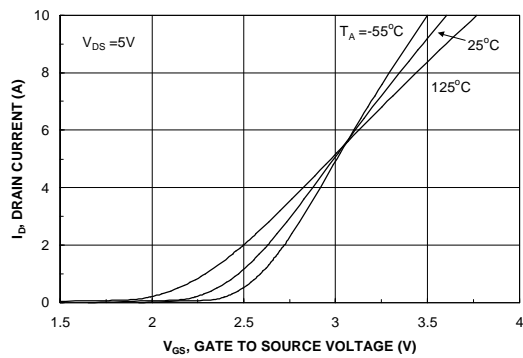


Figure 5. Transfer Characteristics.

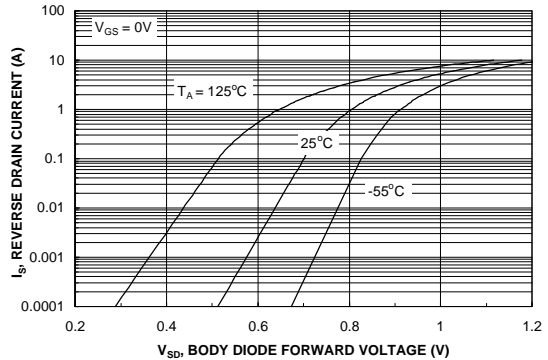


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics: N-Channel (continued)

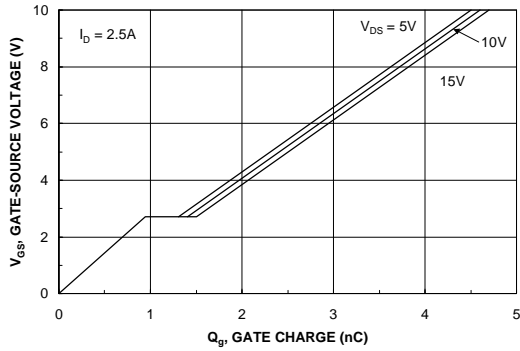


Figure 7. Gate Charge Characteristics.

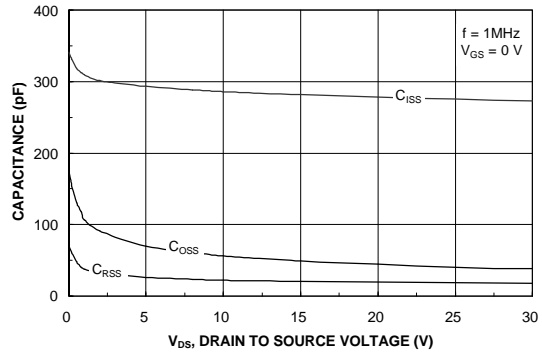


Figure 8. Capacitance Characteristics.

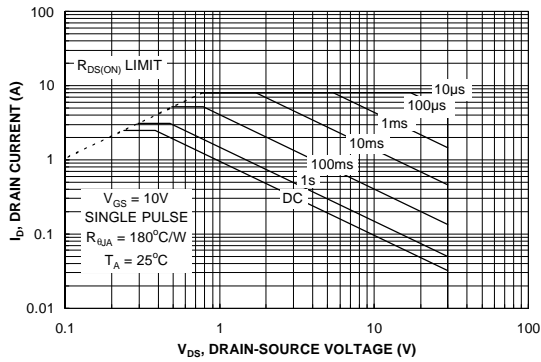


Figure 9. Maximum Safe Operating Area.

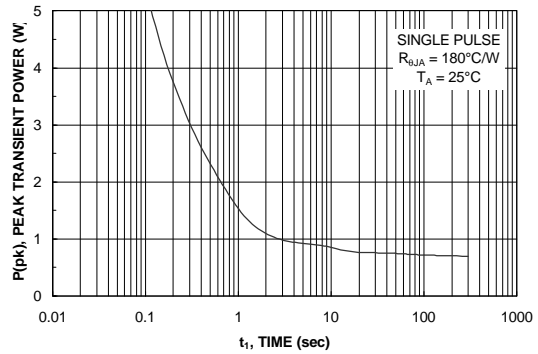


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics: P-Channel

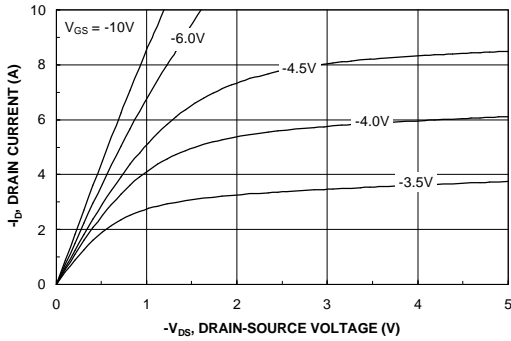


Figure 11. On-Region Characteristics.

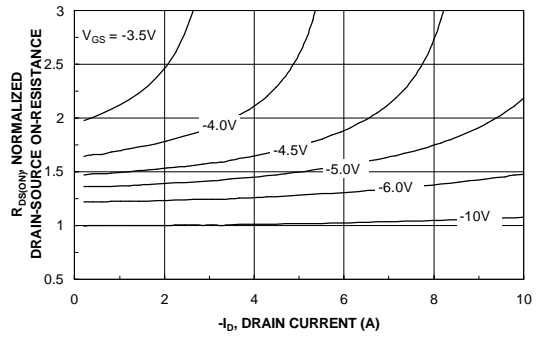


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

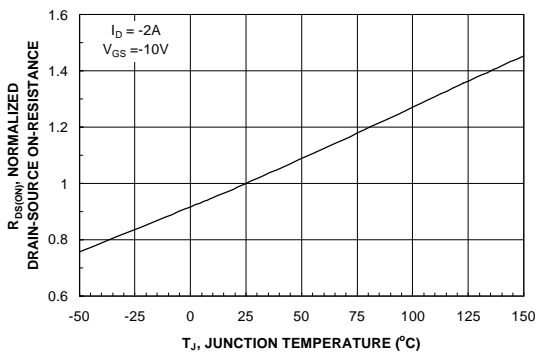


Figure 13. On-Resistance Variation with Temperature.

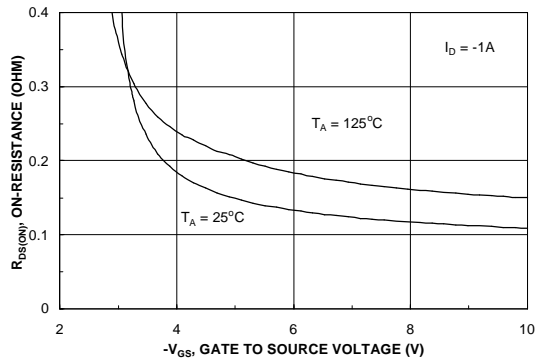


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

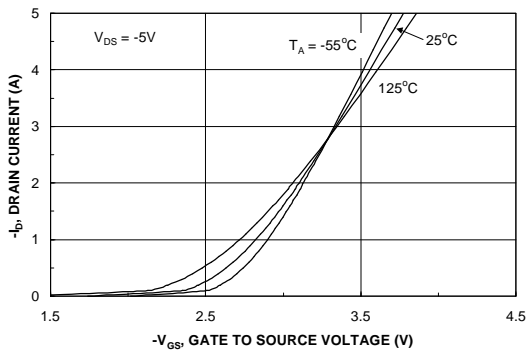


Figure 15. Transfer Characteristics.

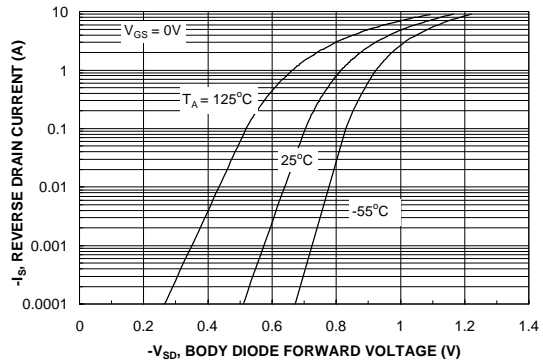
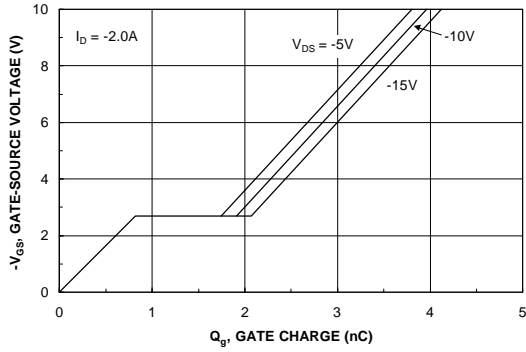
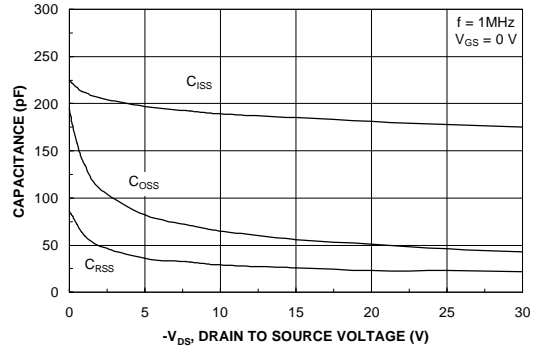


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

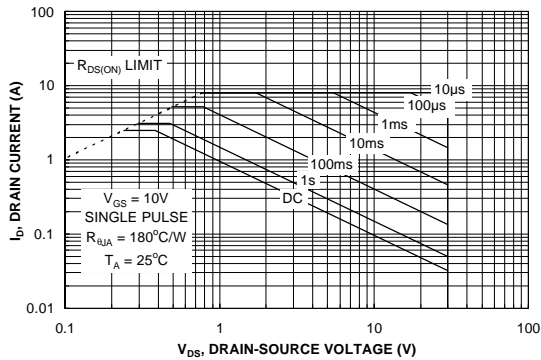
**Typical Characteristics: P-Channel** (continued)



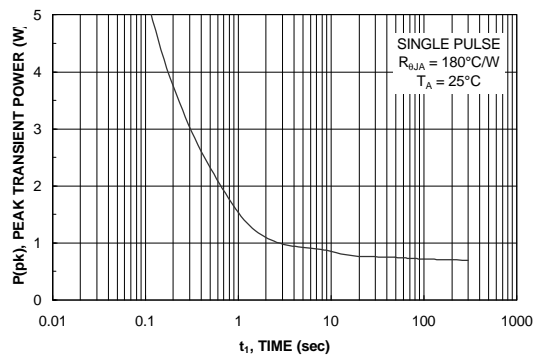
**Figure 17. Gate Charge Characteristics.**



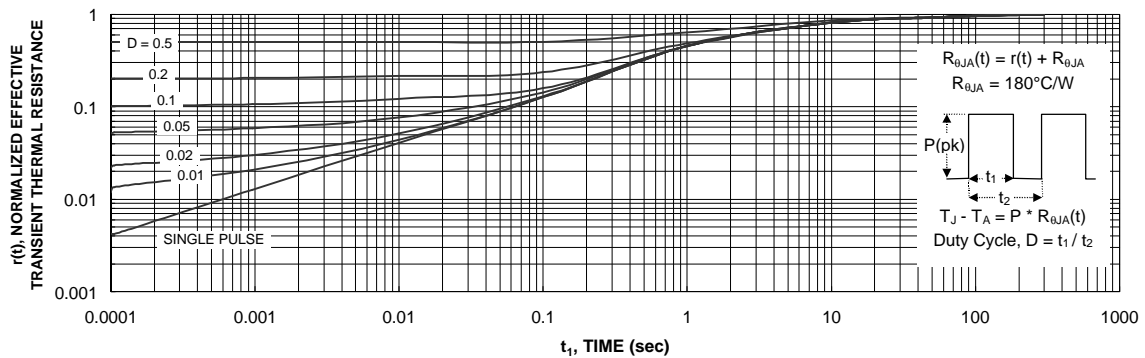
**Figure 18. Capacitance Characteristics.**



**Figure 19. Maximum Safe Operating Area.**



**Figure 20. Single Pulse Maximum Power Dissipation.**



**Figure 21. Transient Thermal Response Curve.**

Thermal characterization performed using the conditions described in Note 1c.  
Transient thermal response will change depending on the circuit board design.

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