

FDJ1032C

Complementary PowerTrench® MOSFET

General Description

These N & P-Channel MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

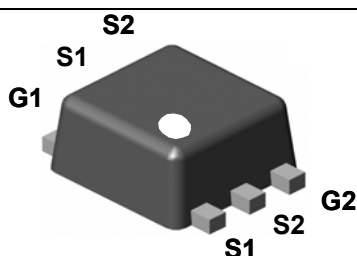
These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Applications

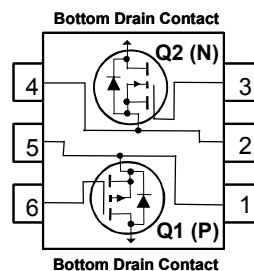
- DC/DC converter
- Load switch
- Motor Driving

Features

- **Q1** -2.8 A, -20 V. $R_{DS(ON)} = 160 \text{ m}\Omega @ V_{GS} = -4.5 \text{ V}$
 $R_{DS(ON)} = 230 \text{ m}\Omega @ V_{GS} = -2.5 \text{ V}$
 $R_{DS(ON)} = 390 \text{ m}\Omega @ V_{GS} = -1.8 \text{ V}$
- **Q2** 3.2 A, 20 V. $R_{DS(ON)} = 90 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
 $R_{DS(ON)} = 130 \text{ m}\Omega @ V_{GS} = 2.5 \text{ V}$
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$.
- FLMP SC75 package: Enhanced thermal performance in industry-standard package size



SC75 DUAL FLMP



Absolute Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DSS}	Drain-Source Voltage	-20	20	V
V_{GSS}	Gate-Source Voltage	± 8	± 12	V
I_D	Drain Current - Continuous (Note 1a) - Pulsed	-2.8 -12	3.2 12	A
P_D	Power Dissipation for single Operation (Note 1a) (Note 1b)	1.5 0.9		W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	80	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1a)	5	

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.H	FDJ1032C	7"	8mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}$, $V_{GS} = 0\text{ V}$, $I_D = -250\ \mu\text{A}$ $I_D = 250\ \mu\text{A}$	Q1 Q2	-20 20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C $I_D = 250\ \mu\text{A}$, Referenced to 25°C	Q1 Q2		-13 13		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}$, $V_{DS} = 16\text{ V}$, $V_{GS} = 0\text{ V}$ $V_{GS} = 0\text{ V}$	Q1 Q2			-1 1	μA
I_{GSS}	Gate-Body Leakage	$V_{GS} = +8\text{ V}$, $V_{GS} = +12\text{ V}$, $V_{DS} = 0\text{ V}$ $V_{DS} = 0\text{ V}$	Q1 Q2			± 100 ± 100	nA
On Characteristics (Note 2)							
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $V_{DS} = V_{GS}$, $I_D = -250\ \mu\text{A}$ $I_D = 250\ \mu\text{A}$	Q1 Q2	-0.4 0.6	-0.8 1.0	-1.5 1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C $I_D = 250\ \mu\text{A}$, Referenced to 25°C	Q1 Q2		3 -3		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -4.5\text{ V}$, $V_{GS} = -2.5\text{ V}$, $V_{GS} = -1.8\text{ V}$, $V_{GS} = -4.5\text{ V}$, $V_{GS} = 4.5\text{ V}$, $V_{GS} = 2.5\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = -2.8\text{ A}$, $I_D = -2.2\text{ A}$, $I_D = -1.7\text{ A}$, $I_D = 2.8\text{ A}$, $I_D = 3.2\text{ A}$, $I_D = 2.7\text{ A}$, $I_D = 3.2\text{ A}$, $T_J = 125^\circ\text{C}$	Q1 Q2		108 163 283 150 70 100 83	160 230 390 238 90 130 132	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}$, $V_{DS} = 5\text{ V}$, $I_D = -2.8\text{ A}$ $I_D = 3.2\text{ A}$	Q1 Q2		5 7.5		S
Dynamic Characteristics							
C_{iss}	Input Capacitance	Q1: $V_{DS} = -10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$	Q1 Q2		290 200		pF
C_{oss}	Output Capacitance	Q2: $V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$	Q1 Q2		55 50		pF
C_{riss}	Reverse Transfer Capacitance	$V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1.0\text{ MHz}$	Q1 Q2		29 30		pF
R_G	Gate Resistance	$V_{GS} = 15\text{ mV}$, $f = 1.0\text{ MHz}$	Q1 Q2		18 10		Ω
Switching Characteristics							
$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = -10\text{ V}$, $I_D = -1\text{ A}$, $R_{GEN} = 6\ \Omega$	Q1 Q2		8 7	16 14	ns
t_r	Turn-On Rise Time	$V_{GS} = -4.5\text{ V}$, Q2: $V_{DD} = 10\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 1\text{ A}$, $R_{GEN} = 6\ \Omega$	Q1 Q2		13 8	23 16	ns
$t_{d(off)}$	Turn-Off Delay Time	$V_{DD} = 10\text{ V}$, $V_{GS} = 4.5\text{ V}$, $I_D = 1\text{ A}$, $R_{GEN} = 6\ \Omega$	Q1 Q2		13 11	23 20	ns
t_f	Turn-Off Fall Time		Q1 Q2		18 2	32 4	ns
Q_g	Total Gate Charge	Q1: $V_{DS} = -10\text{ V}$, $I_D = -2.8\text{ A}$, $V_{GS} = -4.5\text{ V}$	Q1 Q2		3 2	4 3	nC
Q_{gs}	Gate-Source Charge	Q2: $V_{DS} = 10\text{ V}$, $I_D = 3.2\text{ A}$, $V_{GS} = 4.5\text{ V}$	Q1 Q2		0.65 0.4		nC
Q_{gd}	Gate-Drain Charge	$V_{DS} = 10\text{ V}$, $I_D = 3.2\text{ A}$, $V_{GS} = 4.5\text{ V}$	Q1 Q2		0.75 1.0		nC

Electrical Characteristics (continued) $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Drain-Source Diode Characteristics and Maximum Ratings							
I_S	Maximum Continuous Drain-Source Diode Forward Current		Q1 Q2			-1.25 1.25	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -1.3\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)	Q1 Q2		-0.8 0.8	-1.2 1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = -4.2\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$ $I_F = 5.9\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$	Q1 Q2		14 11		nS
Q_{rr}	Diode Reverse Recovery Charge	$I_F = -4.2\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$ $I_F = 5.9\text{ A}, d_I/d_t = 100\text{ A}/\mu\text{s}$	Q1 Q2		4 2.5		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) $80^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper (Single Operation).



- b) $140^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper (Single Operation).

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu\text{s}$, Duty Cycle < 2.0%

Typical Characteristics : Q1

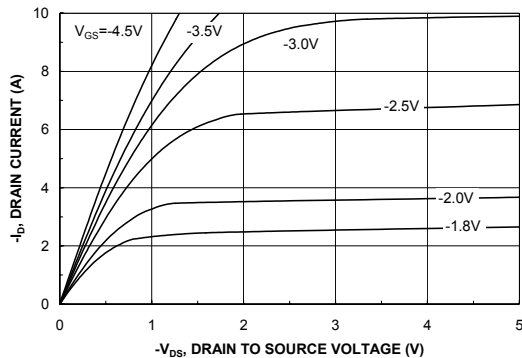


Figure 1. On-Region Characteristics.

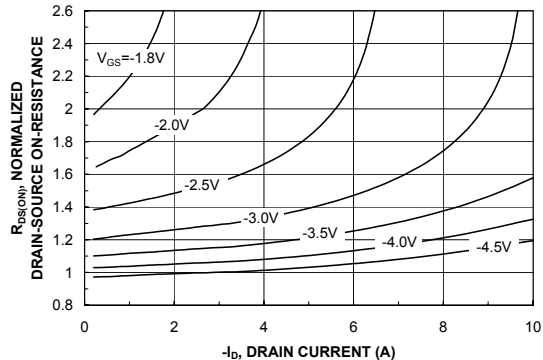


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

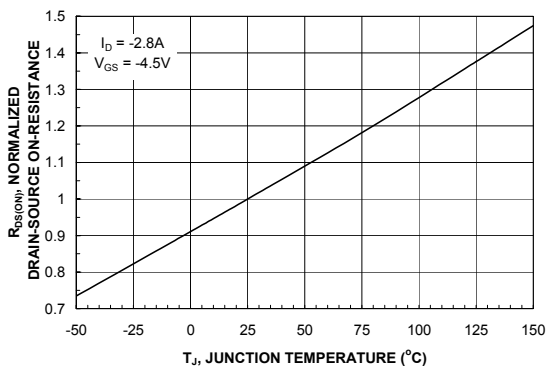


Figure 3. On-Resistance Variation with Temperature.

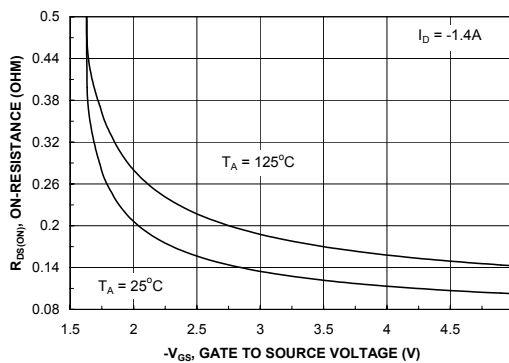


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

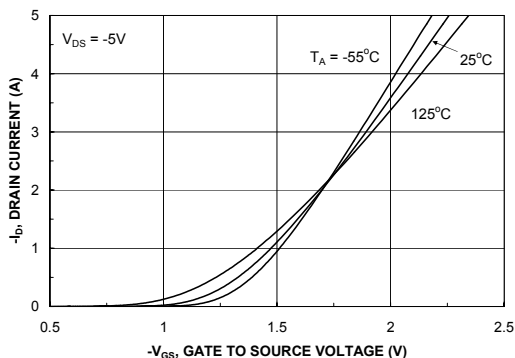


Figure 5. Transfer Characteristics.

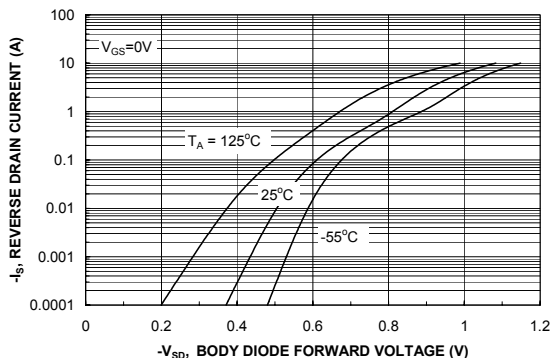


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q1

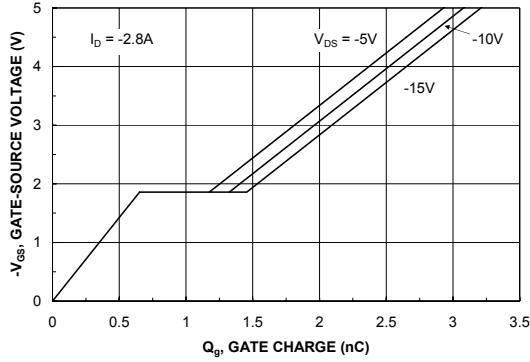


Figure 7. Gate Charge Characteristics.

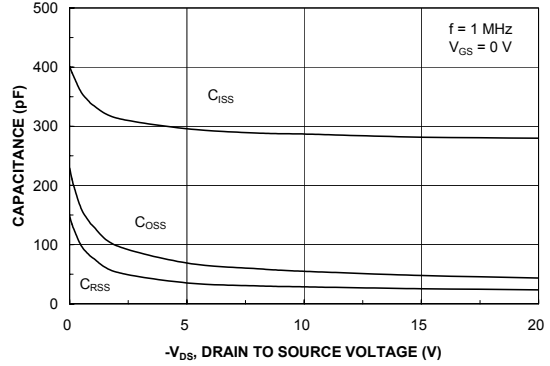


Figure 8. Capacitance Characteristics.

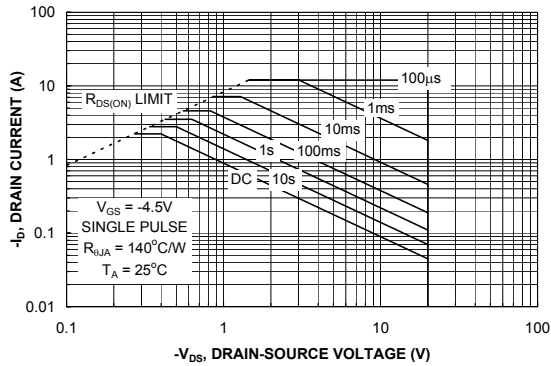


Figure 9. Maximum Safe Operating Area.

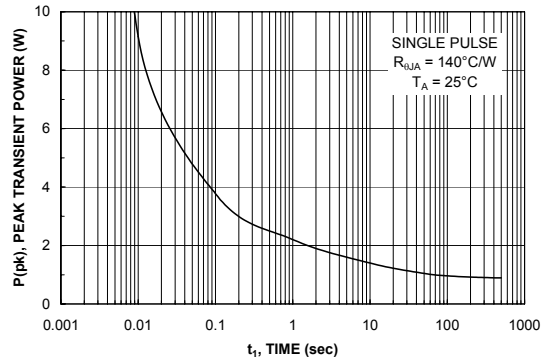


Figure 10. Single Pulse Maximum Power Dissipation.

Typical Characteristics : Q2

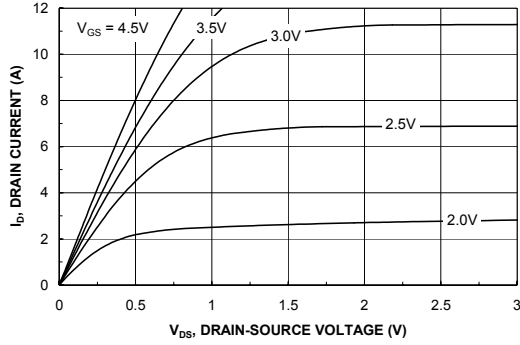


Figure 11. On-Region Characteristics.

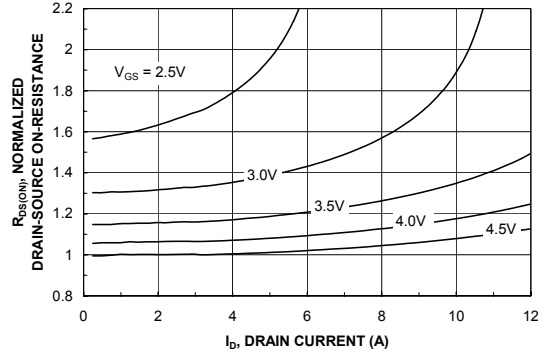


Figure 12. On-Resistance Variation with Drain Current and Gate Voltage.

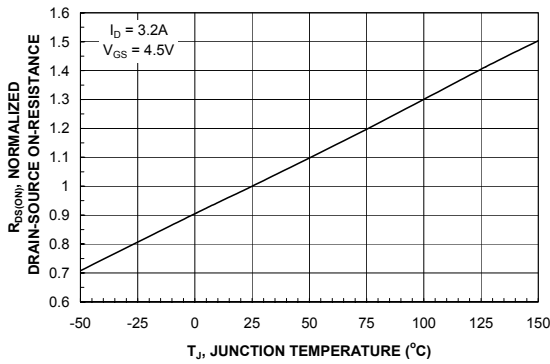


Figure 13. On-Resistance Variation with Temperature.

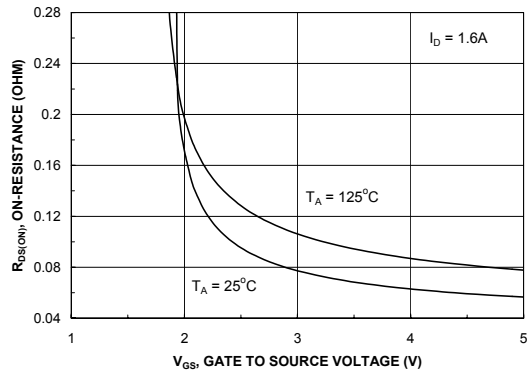


Figure 14. On-Resistance Variation with Gate-to-Source Voltage.

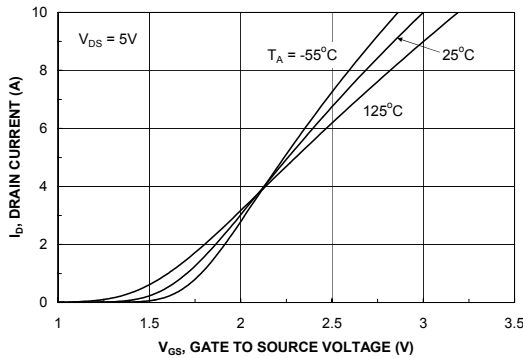


Figure 15. Transfer Characteristics.

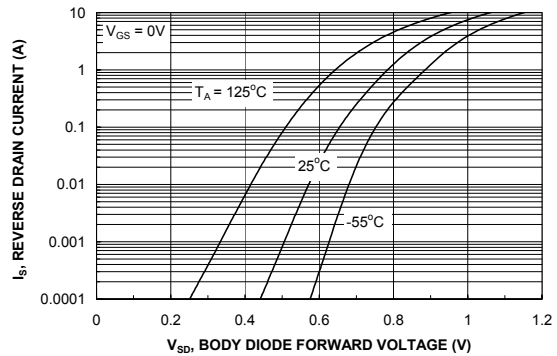


Figure 16. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics : Q2

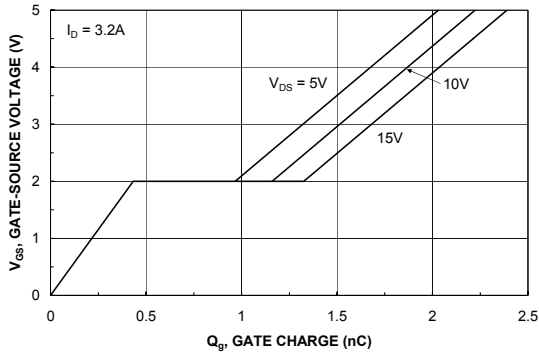


Figure 17. Gate Charge Characteristics.

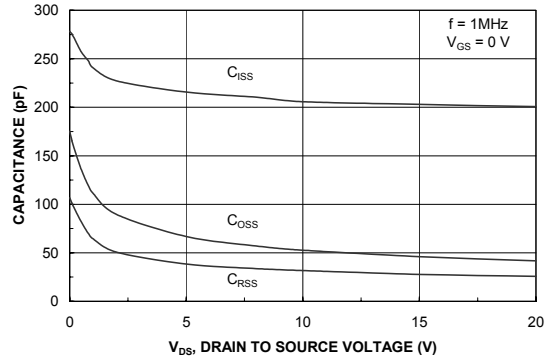


Figure 18. Capacitance Characteristics.

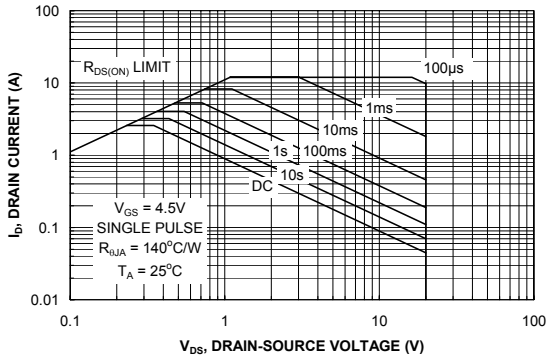


Figure 19. Maximum Safe Operating Area.

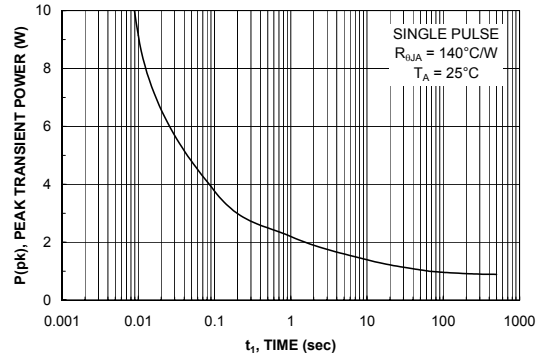


Figure 20. Single Pulse Maximum Power Dissipation.

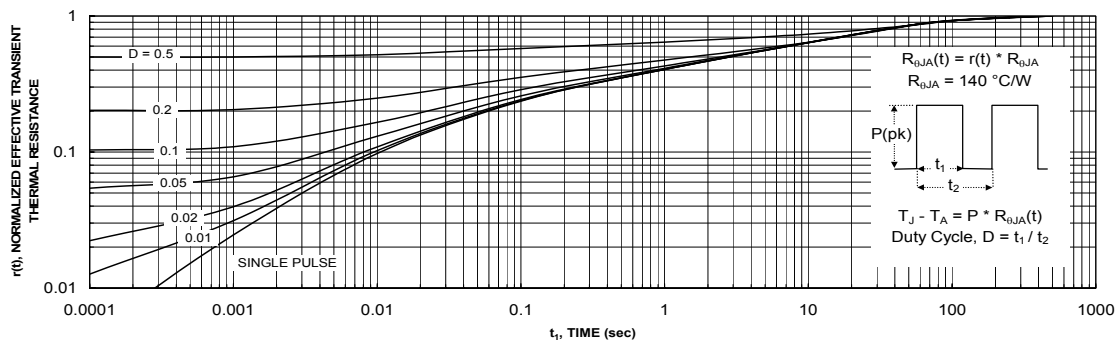
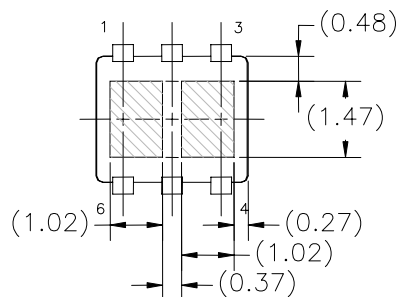


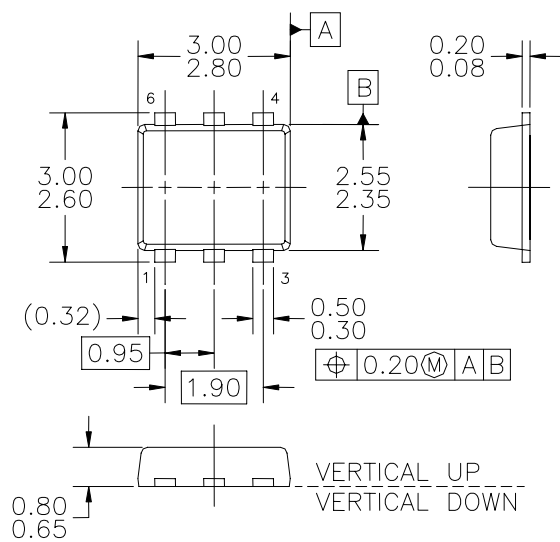
Figure 21. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

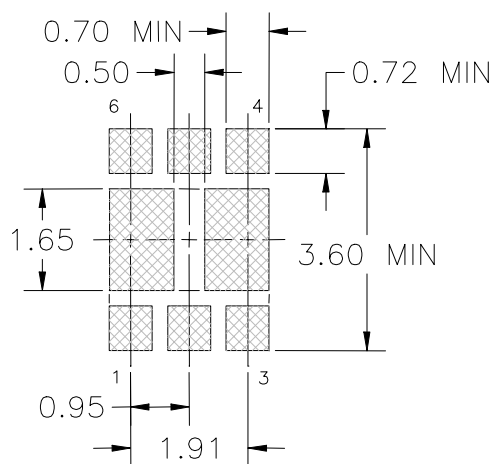
Dimensional Outline and Pad Layout



Bottom View



Top View



**Recommended Landing Pattern
For Standard Dual Configuration**

NOTES: UNLESS OTHERWISE SPECIFIED
ALL DIMENSIONS ARE IN MILLIMETERS.

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EnSigna™	i-Lo™	OCX™	RapidConfigure™	TruTranslation™
FACT™	ImpliedDisconnect™	OCXPro™	RapidConnect™	UHC™
FACT Quiet Series™		OPTOLOGIC®	µSerDes™	UltraFET®
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Programmable Active Droop™		POP™	SPM™	

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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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