

FDB12N50F

N-Channel UniFET™ FRFET® MOSFET 500 V, 11.5 A, 700 mΩ

Features

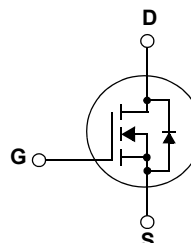
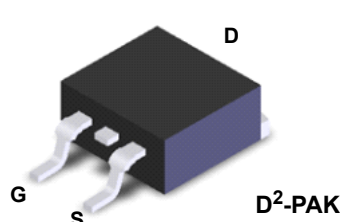
- $R_{DS(on)} = 590 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 6 \text{ A}$
- Low Gate Charge (Typ. 21 nC)
- Low C_{rss} (Typ. 11 pF)
- 100% Avalanche Tested
- Improve dv/dt Capability
- RoHS Compliant

Applications

- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its t_{rr} is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDB12N50F	Unit
V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	11.5
		- Continuous ($T_C = 100^\circ\text{C}$)	6.9
I_{DM}	Drain Current	- Pulsed (Note 1)	46
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	456
I_{AR}	Avalanche Current	(Note 1)	11.5
E_{AR}	Repetitive Avalanche Energy	(Note 1)	16.5
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	165
		- Derate above 25°C	1.33
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDB12N50F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.75	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB12N50F	FDB12N50FTM_WS	D2-PAK	330mm	24mm	800

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.5	-	$V/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}$, $V_{GS} = 0\text{V}$	-	-	10	μA
		$V_{DS} = 400\text{V}$, $T_C = 125^\circ\text{C}$	-	-	100	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 6\text{A}$	-	0.59	0.7	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{V}$, $I_D = 6\text{A}$	-	12	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	1050	1395	pF
C_{oss}	Output Capacitance		-	135	180	pF
C_{rss}	Reverse Transfer Capacitance		-	11	17	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\text{V}$, $I_D = 11.5\text{A}$ $V_{GS} = 10\text{V}$ (Note 4)	-	21	30	nC
Q_{gs}	Gate to Source Gate Charge		-	6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	9	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}$, $I_D = 11.5\text{A}$ $R_G = 25\Omega$ (Note 4)	-	21	50	ns
t_r	Turn-On Rise Time		-	45	100	ns
$t_{d(off)}$	Turn-Off Delay Time		-	50	110	ns
t_f	Turn-Off Fall Time		-	35	80	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current	-	-	11.5	A	
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	46	A	
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 11.5A	-	-	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 11.5A	-	134	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100A/μs	-	0.37	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 6.9\text{mH}$, $I_{AS} = 11.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 11.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

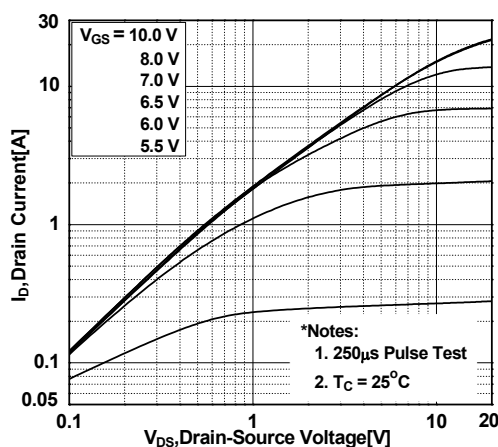


Figure 2. Transfer Characteristics

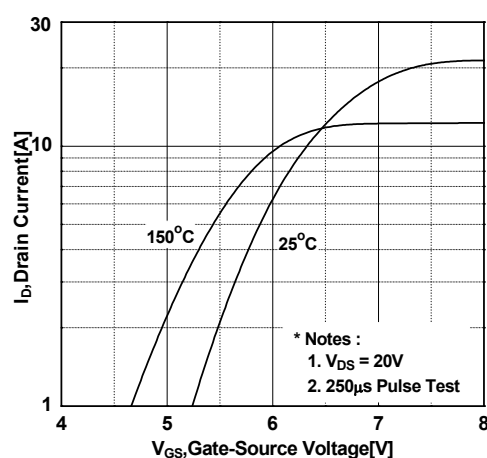


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

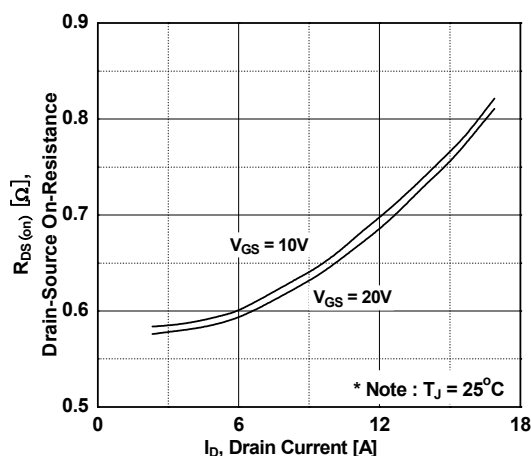


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

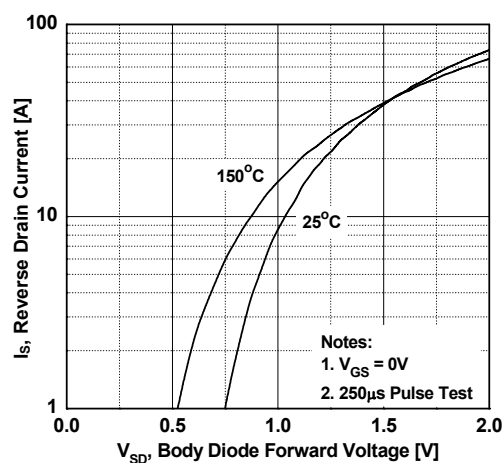


Figure 5. Capacitance Characteristics

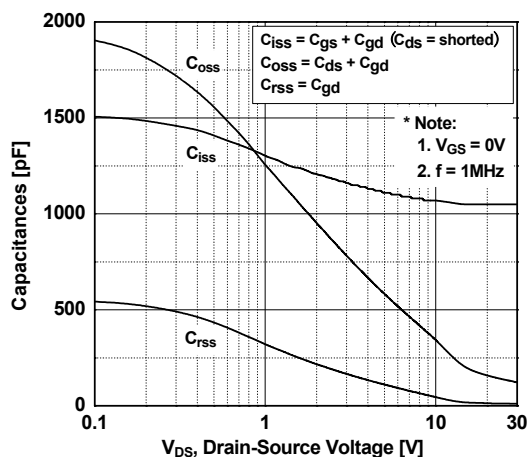
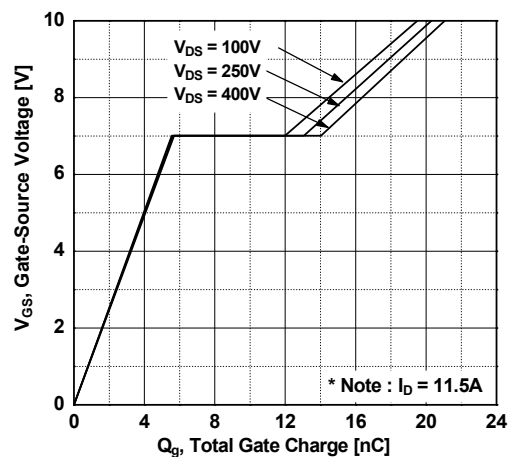


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

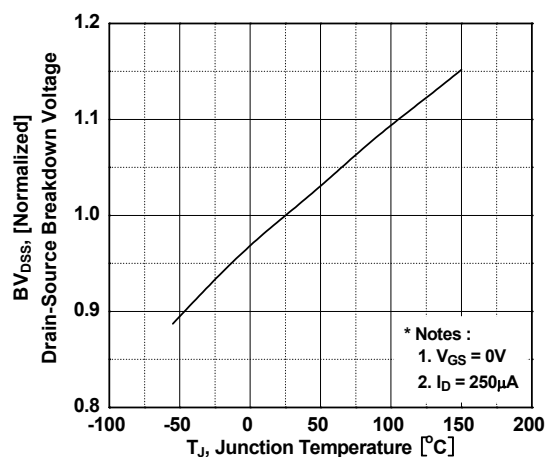


Figure 8. Maximum Safe Operating Area

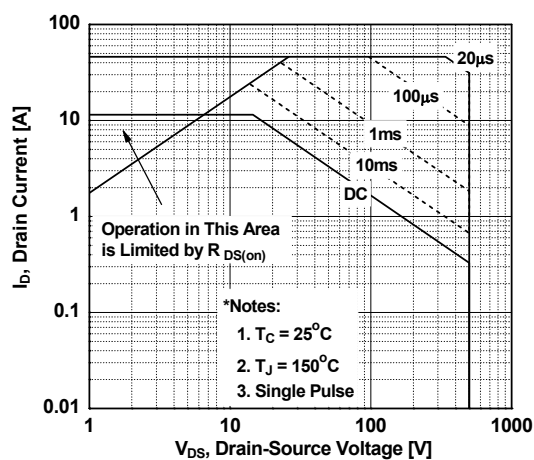


Figure 9. Maximum Drain Current vs. Case Temperature

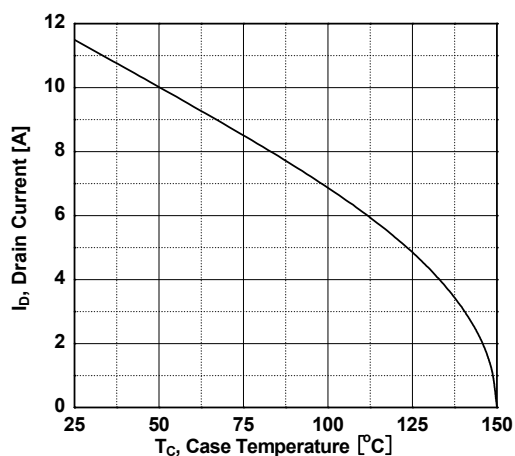
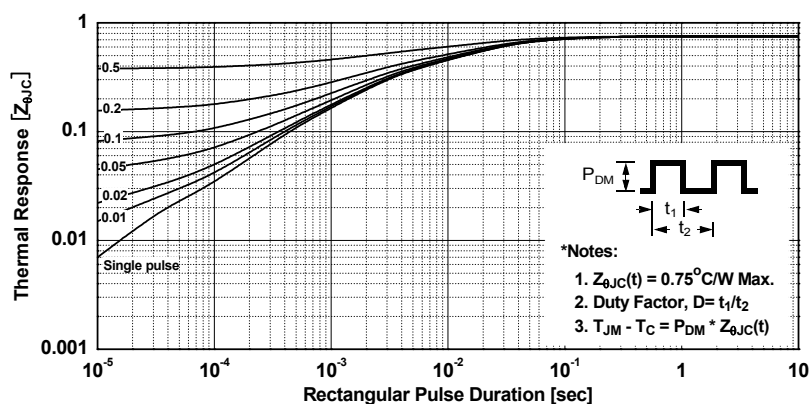
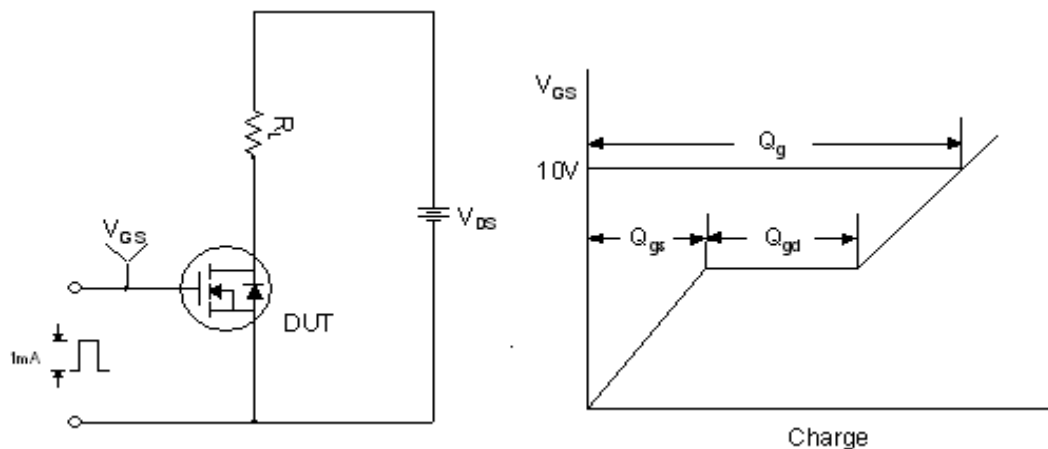


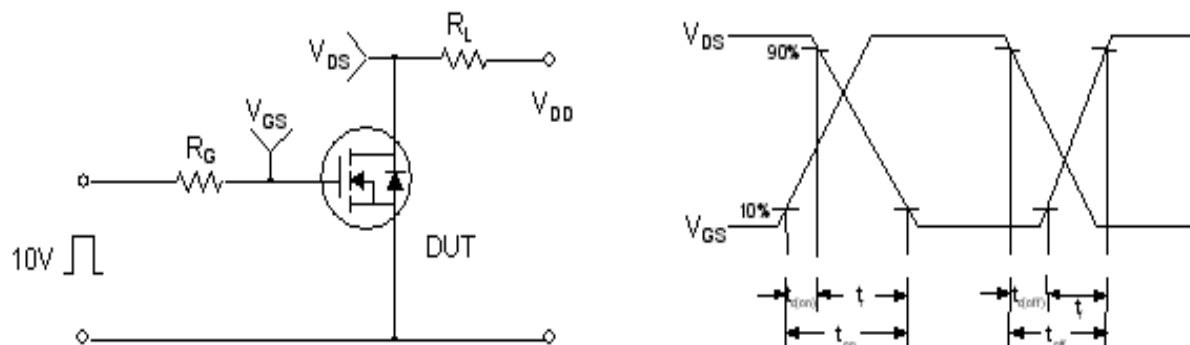
Figure 10. Transient Thermal Response Curve



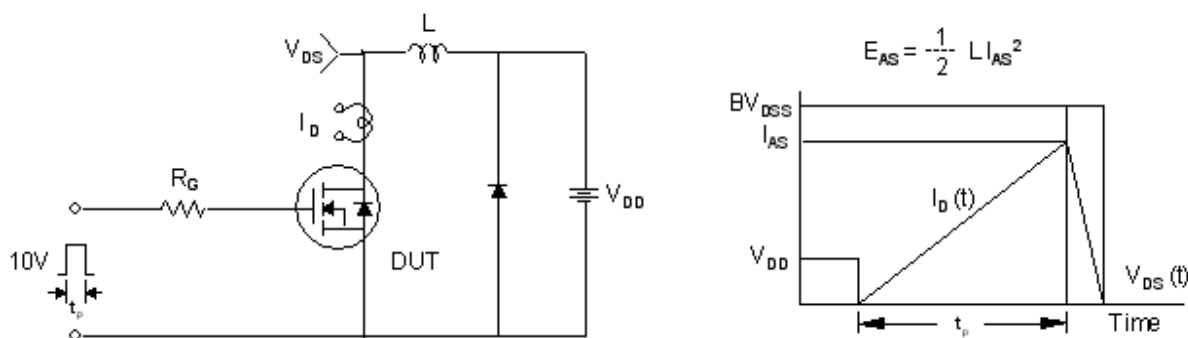
Gate Charge Test Circuit & Waveform



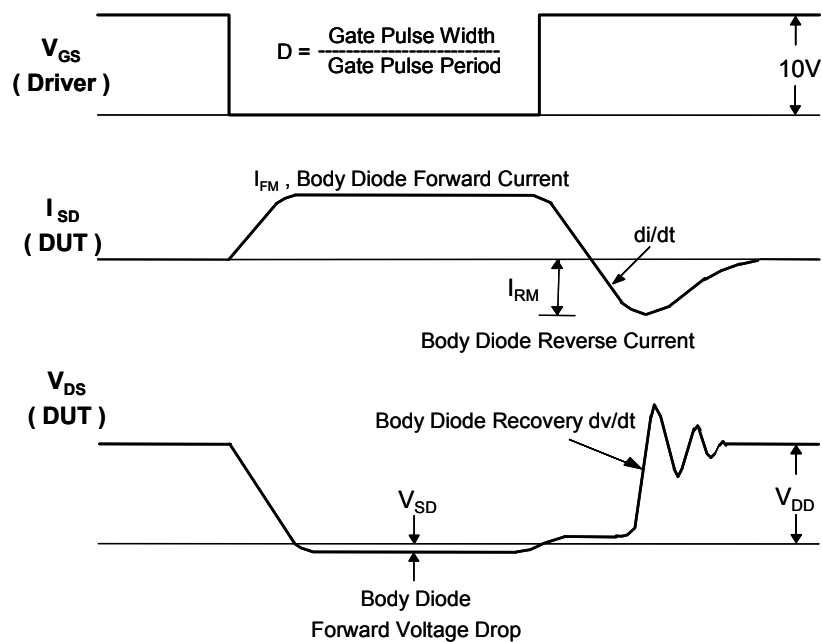
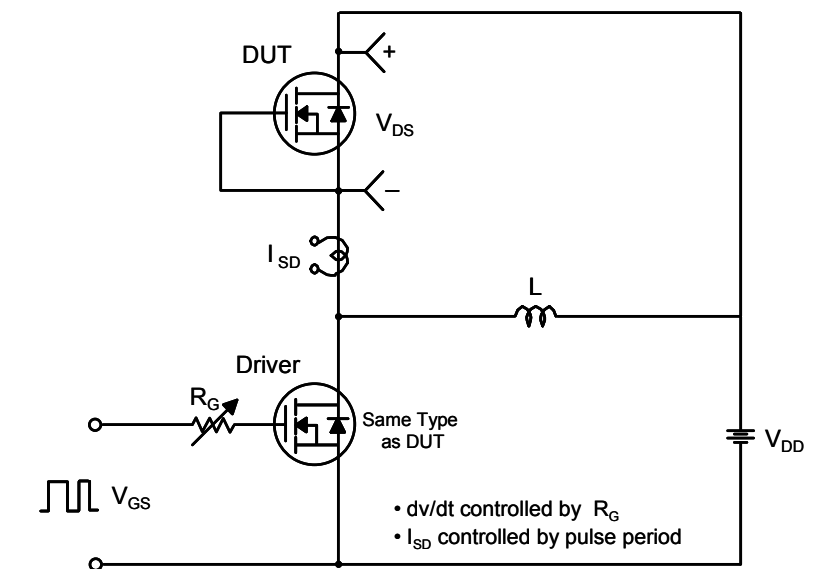
Resistive Switching Test Circuit & Waveforms



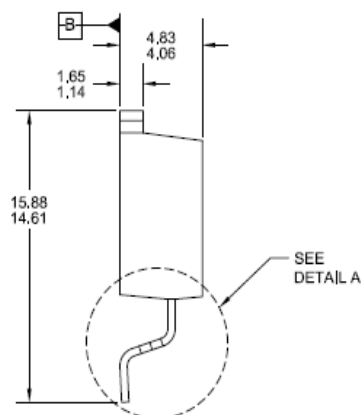
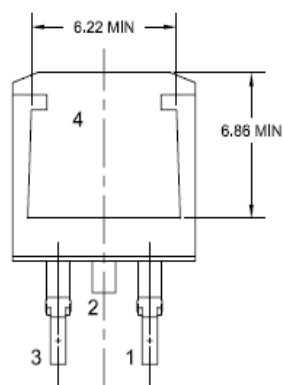
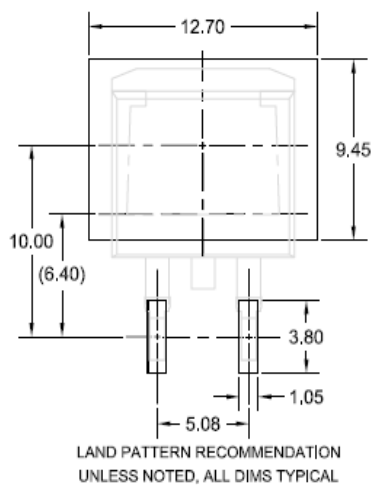
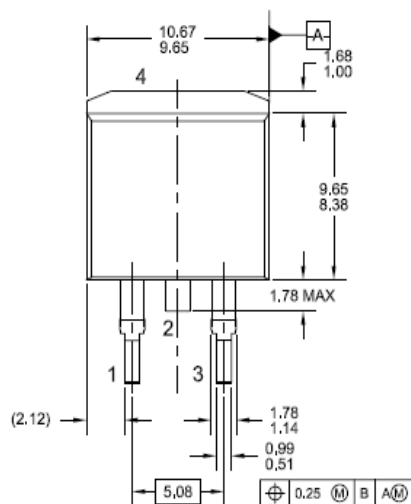
Unclamped Inductive Switching Test Circuit & Waveforms



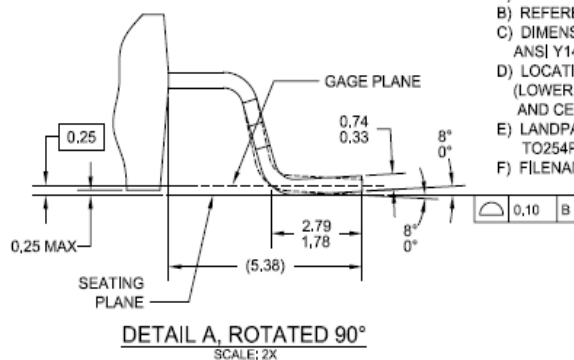
Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D²PAK

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) ALL DIMENSIONS ARE IN MILLIMETERS.
 - B) REFERENCE JEDEC, TO-263, VARIATION AB.
 - C) DIMENSIONING AND TOLERANCING PER
ANSI Y14.5M - 1994.
 - D) LOCATION OF THE PIN HOLE MAY VARY
(LOWER LEFT CORNER, LOWER CENTER
AND CENTER OF THE PACKAGE).
 - E) LANDPATTERN RECOMMENDATION PER IPC
TO254P1524X482-3N
 - F) FILENAME: TO263A02REV6



Dimensions in Millimeters



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