

FDP55N06/FDPF55N06

60V N-Channel MOSFET

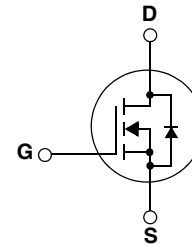
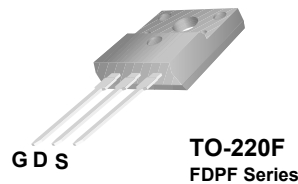
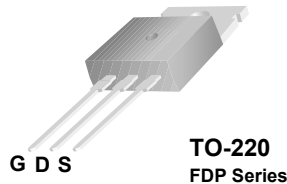
Features

- 55A, 60V, $R_{DS(on)} = 0.022 \Omega @ V_{GS} = 10 V$
- Low gate charge (typical 30 nC)
- Low C_{rss} (typical 60 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficient switched mode power supplies, active power factor correction, electronic lamp ballast based on half bridge topology.



Absolute Maximum Ratings $T_C = 25^\circ C$ unless otherwise noted

Symbol	Parameter	FDP55N06	FDPF55N06	Units
V_{DSS}	Drain-Source Voltage	60		V
I_D	Drain Current - Continuous ($T_C = 25^\circ C$) - Continuous ($T_C = 100^\circ C$)	55	55 *	A
		34.8	34.8 *	A
I_{DM}	Drain Current - Pulsed (Note 1)	220	220 *	A
V_{GSS}	Gate-Source Voltage	± 25		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	480		mJ
I_{AR}	Avalanche Current (Note 1)	55		A
E_{AR}	Repetitive Avalanche Energy (Note 1)	11.4		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5		V/ns
P_D	Power Dissipation ($T_C = 25^\circ C$) - Derate above $25^\circ C$	114	48	W
		0.9	0.4	W/ $^\circ C$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150		$^\circ C$
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300		$^\circ C$

* Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP55N06	FDPF55N06	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	1.1	2.58	$^\circ C/W$
$R_{\theta JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5	--	$^\circ C/W$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	$^\circ C/W$

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP55N06	FDP55N06	TO-220			50
FDPF55N06	FDPF55N06	TO-220F			50

Electrical Characteristics T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} = 0 V, I _D = 250 μA	60	--	--	V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C	--	0.05	--	V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 60 V, V _{GS} = 0 V	--	--	1	μA
		V _{DS} = 48 V, T _C = 150°C	--	--	10	μA
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	--	--	100	nA
I _{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -20 V, V _{DS} = 0 V	--	--	-100	nA
On Characteristics						
V _{GS(th)}	Gate Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	2.0	--	4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 27.5 A	--	0.018	0.022	Ω
g _{FS}	Forward Transconductance	V _{DS} = 25 V, I _D = 27.5 A (Note 4)	--	33	--	S
Dynamic Characteristics						
C _{iss}	Input Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz	--	1160	1510	pF
C _{oss}	Output Capacitance		--	375	490	pF
C _{rss}	Reverse Transfer Capacitance		--	60	90	pF
Switching Characteristics						
t _{d(on)}	Turn-On Delay Time	V _{DD} = 30 V, I _D = 55 A, R _G = 25 Ω	--	30	65	ns
t _r	Turn-On Rise Time		--	130	265	ns
t _{d(off)}	Turn-Off Delay Time		--	70	150	ns
t _f	Turn-Off Fall Time		(Note 4, 5)	--	95	195
Q _g	Total Gate Charge	V _{DS} = 48 V, I _D = 55A, V _{GS} = 10 V	--	30	37	nC
Q _{gs}	Gate-Source Charge		--	6.5	--	nC
Q _{gd}	Gate-Drain Charge		(Note 4, 5)	--	7.5	--
Drain-Source Diode Characteristics and Maximum Ratings						
I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	55	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	220	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 55 A	--	--	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 55 A, dI _F / dt = 100 A/μs (Note 4)	--	40	--	ns
Q _{rr}	Reverse Recovery Charge		--	55	--	μC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 5.6mH, I_{AS} = 55A, V_{DD} = 50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 55A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300μs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Performance Characteristics

Figure 1. On-Region Characteristics

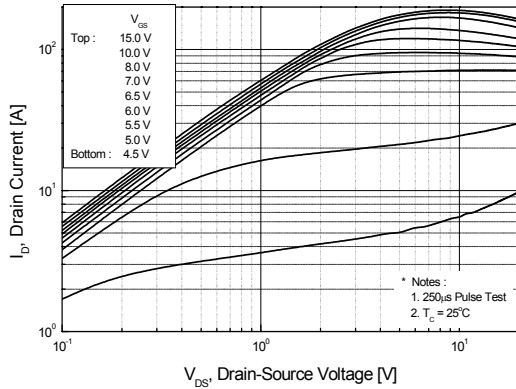


Figure 2. Transfer Characteristics

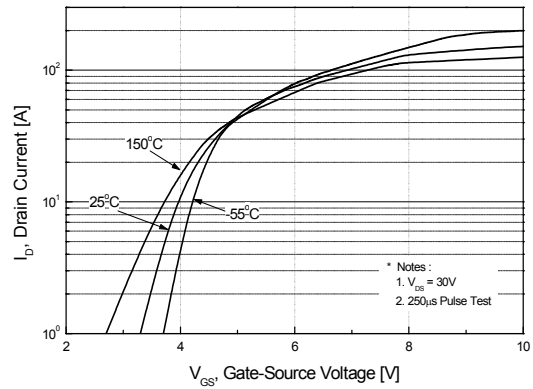


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

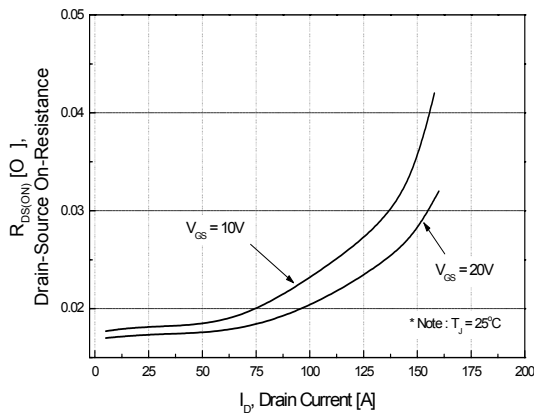


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

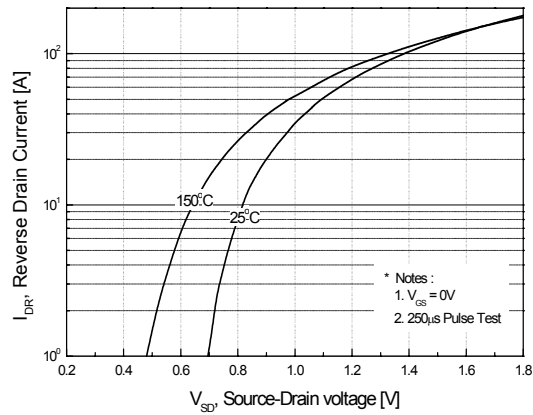


Figure 5. Capacitance Characteristics

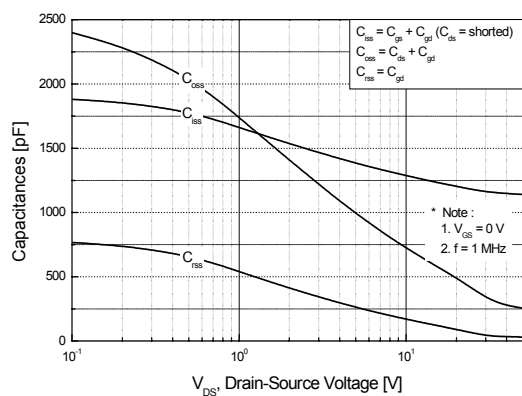
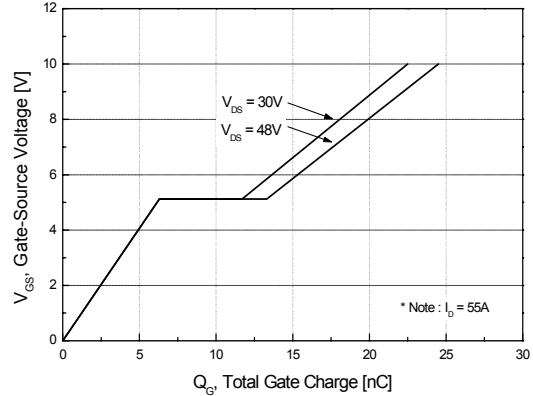


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

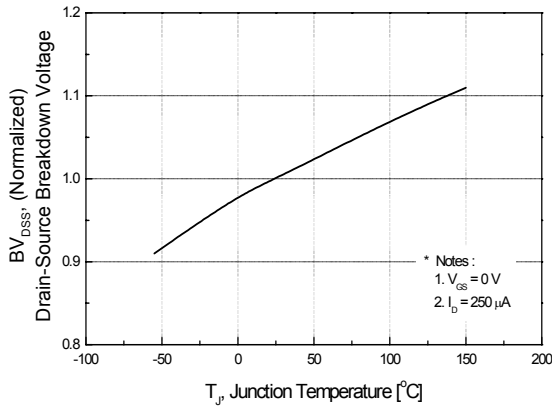


Figure 8. On-Resistance Variation vs. Temperature

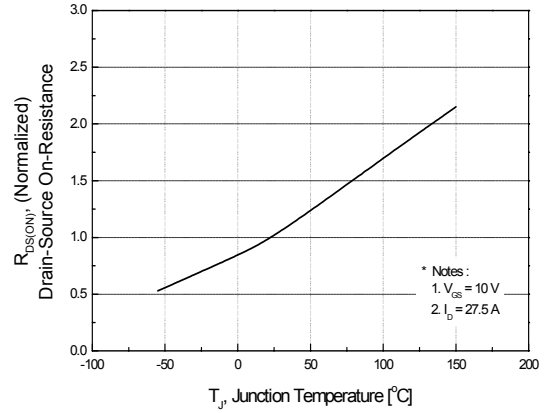


Figure 9-1. Maximum Safe Operating Area for FDP55N06

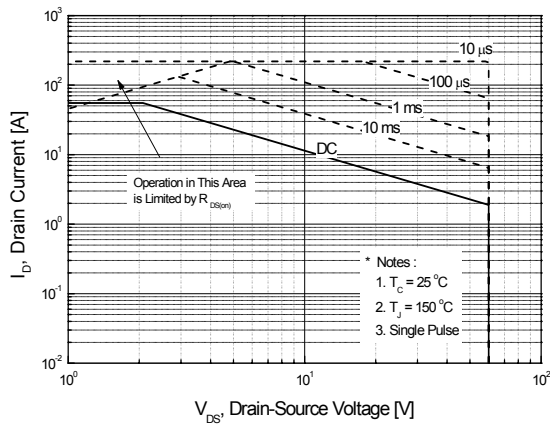


Figure 9-2. Maximum Safe Operating Area for FDPF55N06

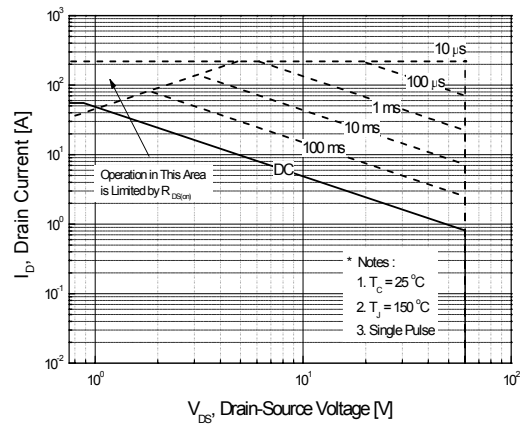
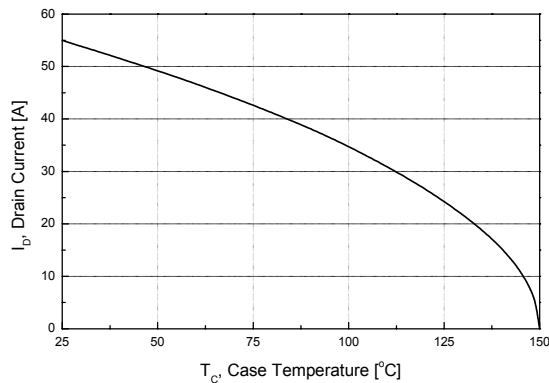


Figure 10. Maximum Drain Current vs. Case Temperature



Typical Performance Characteristics (Continued)

Figure 11-1. Transient Thermal Response Curve for FDP55N06

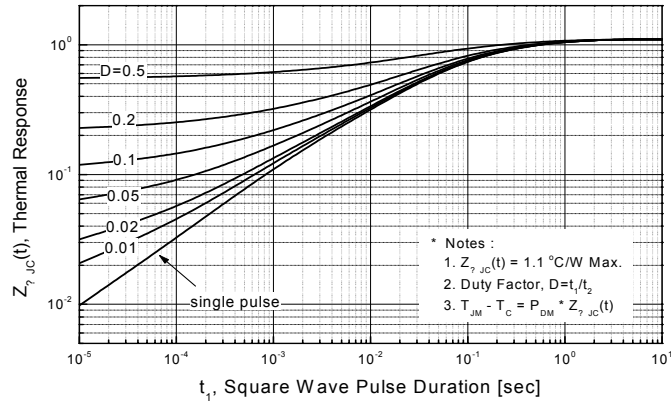
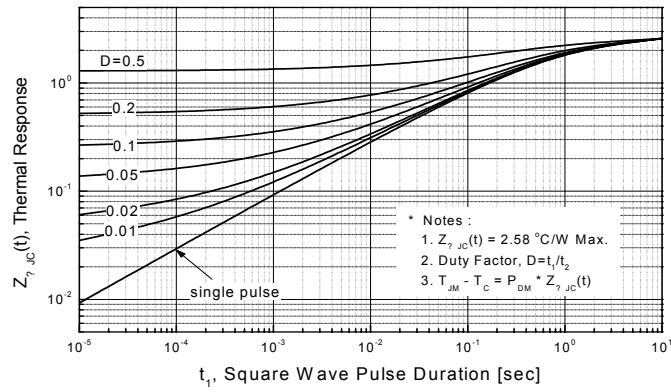
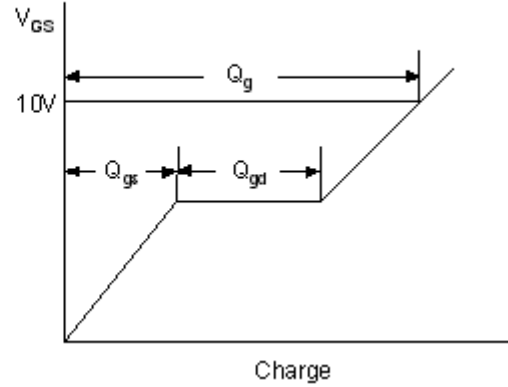
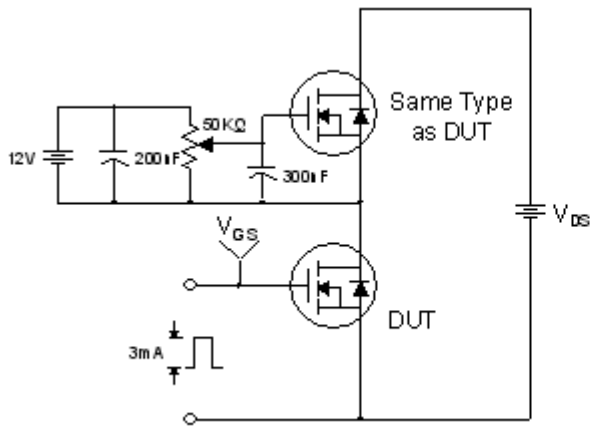


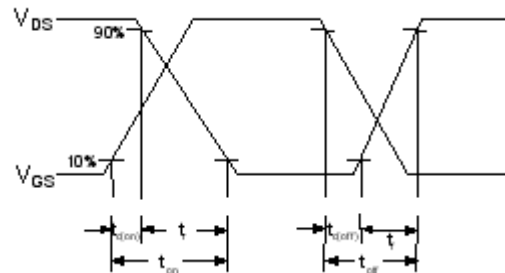
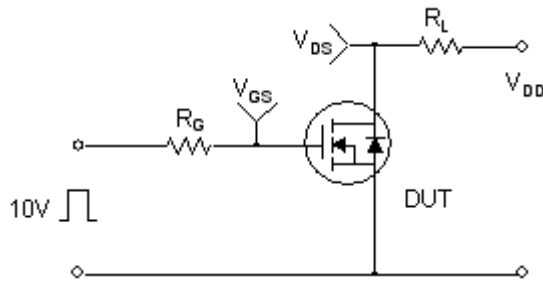
Figure 11-2. Transient Thermal Response Curve for FDPF55N06



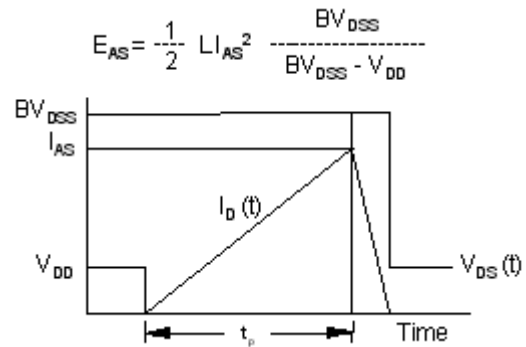
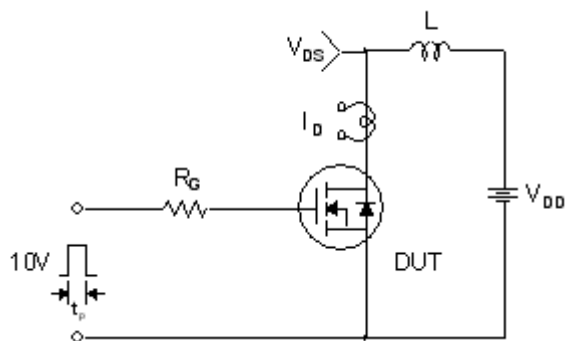
Gate Charge Test Circuit & Waveform



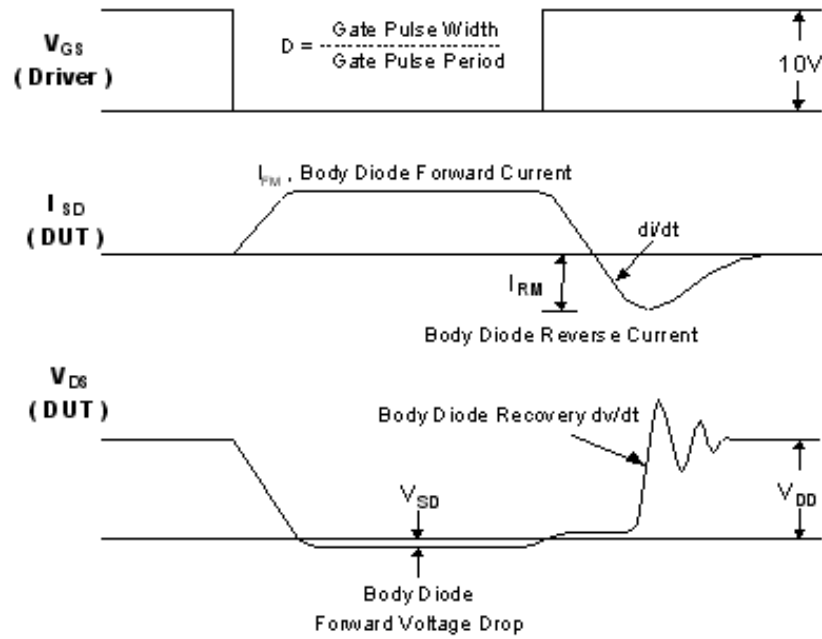
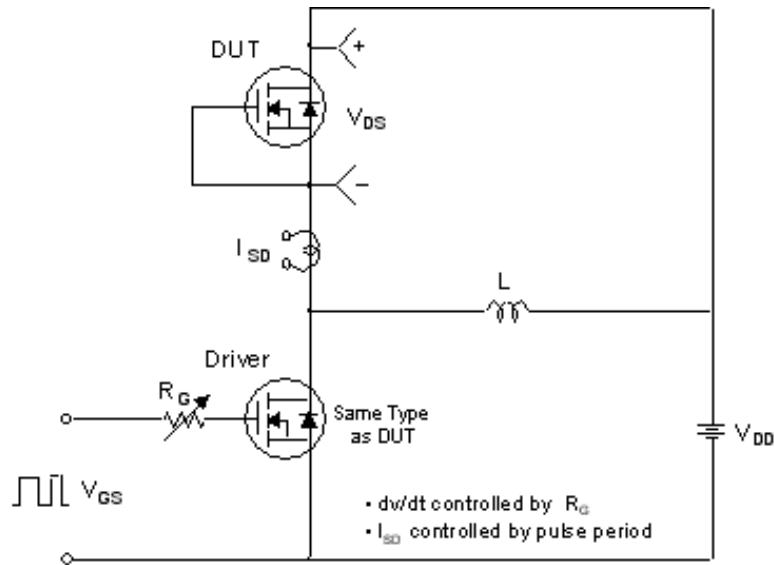
Resistive Switching Test Circuit & Waveforms



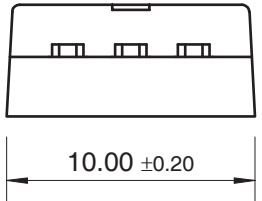
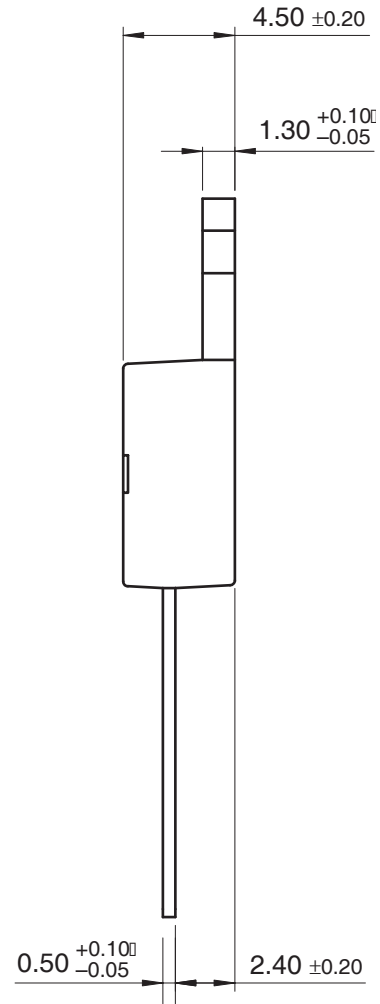
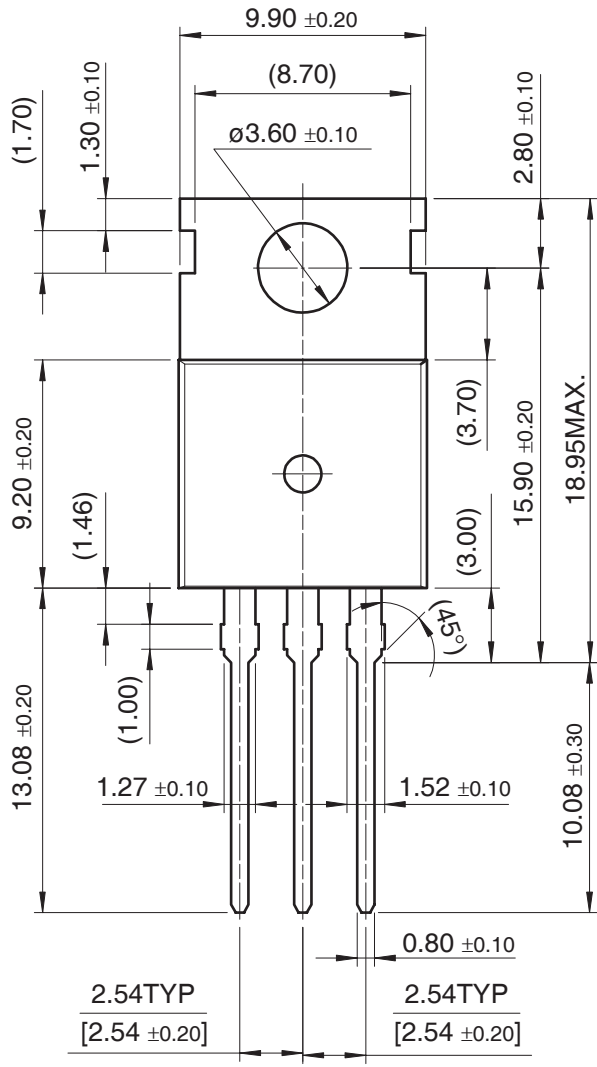
Unclamped Inductive Switching Test Circuit & Waveforms



Peak Diode Recovery dv/dt Test Circuit & Waveforms

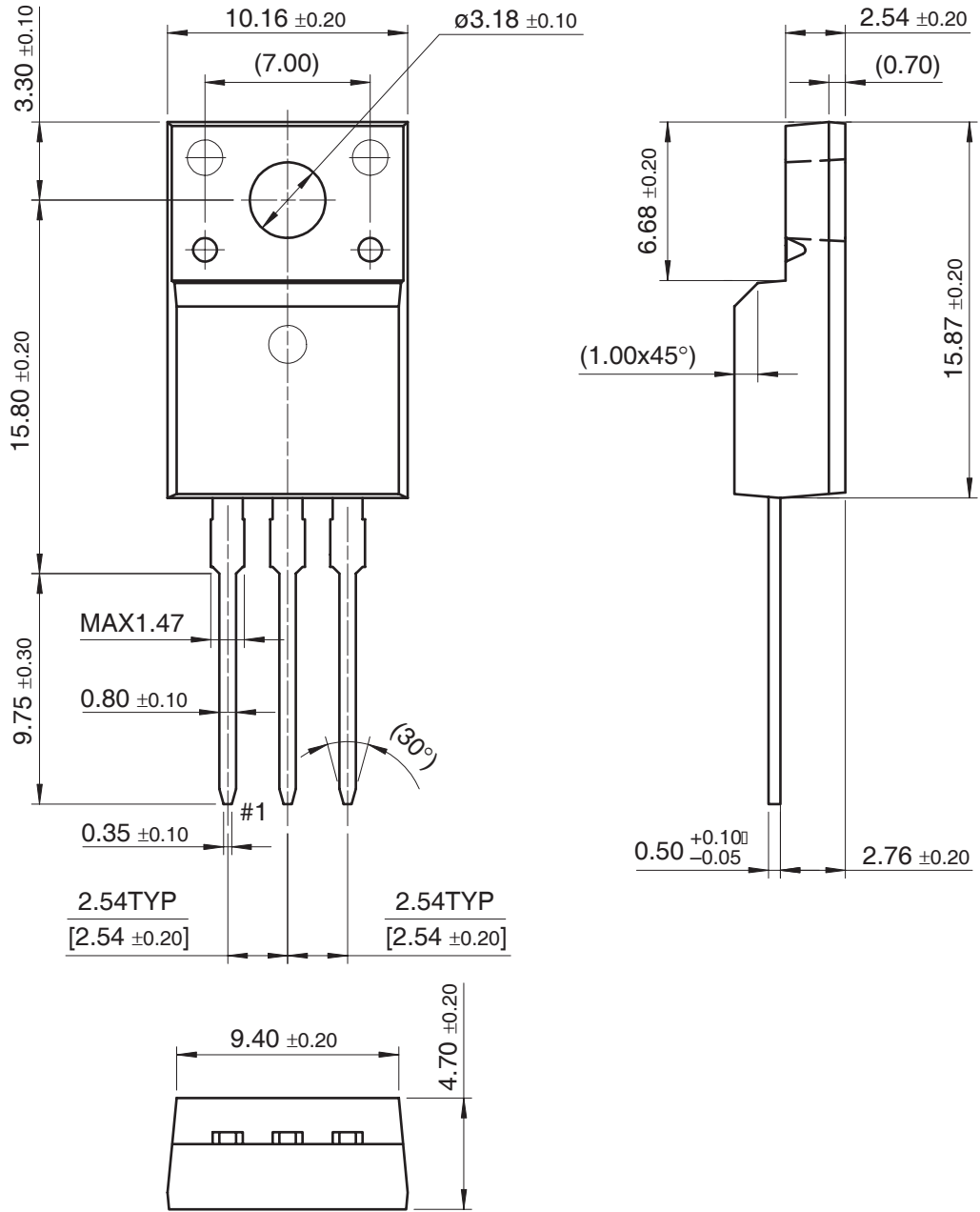


TO-220



Mechanical Dimensions

TO-220F



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