

FDS4435BZ

P-Channel PowerTrench® MOSFET -30V, -8.8A, 20mΩ

Features

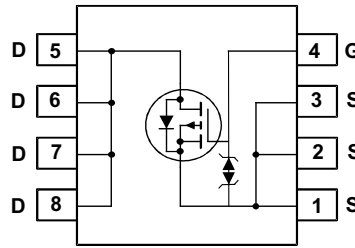
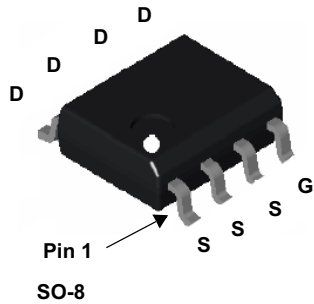
- Max $r_{DS(on)}$ = 20mΩ at $V_{GS} = -10V$, $I_D = -8.8A$
- Max $r_{DS(on)}$ = 35mΩ at $V_{GS} = -4.5V$, $I_D = -6.7A$
- Extended V_{GSS} range (-25V) for battery applications
- HBM ESD protection level of ±3.8KV typical (note 3)
- High performance trench technology for extremely low $r_{DS(on)}$
- High power and current handling capability
- Termination is Lead-free and RoHS compliant



General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench® process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	-30	V
V_{GS}	Gate to Source Voltage	±25	V
I_D	Drain Current -Continuous	$T_A = 25^\circ\text{C}$ (Note 1a)	-8.8
	-Pulsed		-50
P_D	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	2.5
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1b)	1.0
E_{AS}	Single Pulse Avalanche Energy	(Note 4)	24
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	25	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS4435BZ	FDS4435BZ	SO-8	13"	12mm	2500units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		-21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{V}, V_{GS} = 0\text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 25\text{V}, V_{DS} = 0\text{V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	-1	-2.1	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = -250\mu\text{A}$, referenced to 25°C		6		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = -10\text{V}, I_D = -8.8\text{A}$		16	20	m Ω
		$V_{GS} = -4.5\text{V}, I_D = -6.7\text{A}$		26	35	
		$V_{GS} = -10\text{V}, I_D = -8.8\text{A}, T_J = 125^\circ\text{C}$		22	28	
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{V}, I_D = -8.8\text{A}$		24		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$		1385	1845	pF
C_{oss}	Output Capacitance			275	365	pF
C_{rss}	Reverse Transfer Capacitance			230	345	pF
R_g	Gate Resistance	$f = 1\text{MHz}$		4.5		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -15\text{V}, I_D = -8.8\text{A}, V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$		10	20	ns
t_r	Rise Time			6	12	ns
$t_{d(off)}$	Turn-Off Delay Time			30	48	ns
t_f	Fall Time			12	22	ns
Q_g	Total Gate Charge		$V_{GS} = 0\text{V to } -10\text{V}$		28	40
Q_g	Total Gate Charge	$V_{GS} = 0\text{V to } -5\text{V}$		16	23	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = -15\text{V}, I_D = -8.8\text{A}$		5.2		nC
Q_{gd}	Gate to Drain "Miller" Charge			7.4		nC

Drain-Source Diode Characteristics

V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = -8.8\text{A}$ (Note 2)		-0.9	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -8.8\text{A}, di/dt = 100\text{A}/\mu\text{s}$		29	44	ns
Q_{rr}	Reverse Recovery Charge			23	35	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $50^\circ\text{C}/\text{W}$ when mounted on a 1in^2 pad of 2 oz copper.



b. $125^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

4. Starting $T_J = 25^\circ\text{C}$, $L = 1\text{mH}$, $I_{AS} = -7\text{A}$, $V_{DD} = -30\text{V}$, $V_{GS} = -10\text{V}$

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

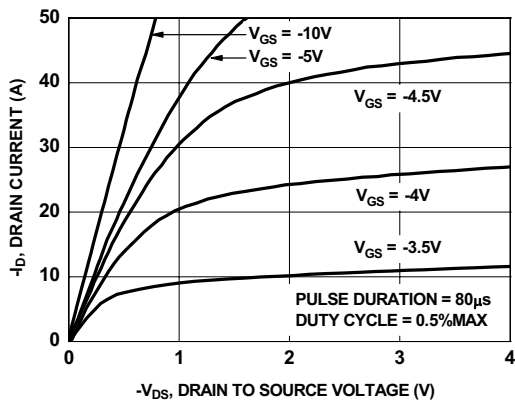


Figure 1. On-Region Characteristics

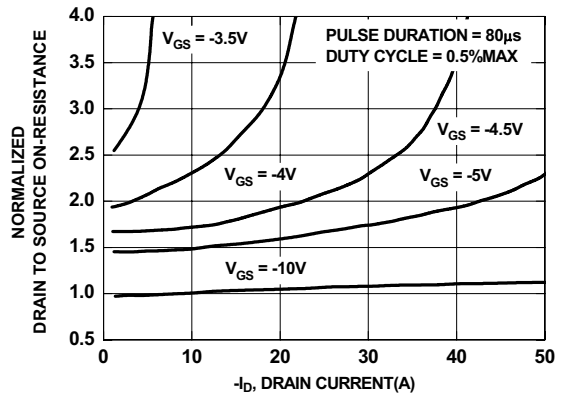


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

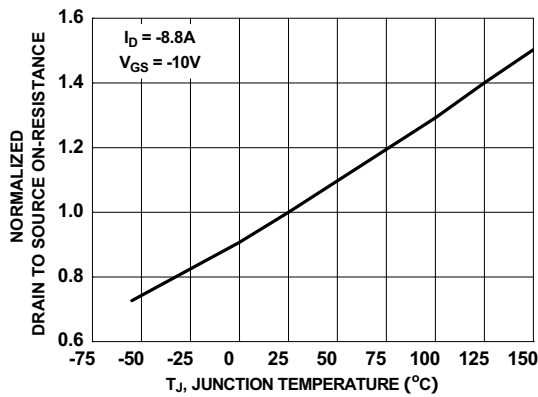


Figure 3. Normalized On-Resistance vs Junction Temperature

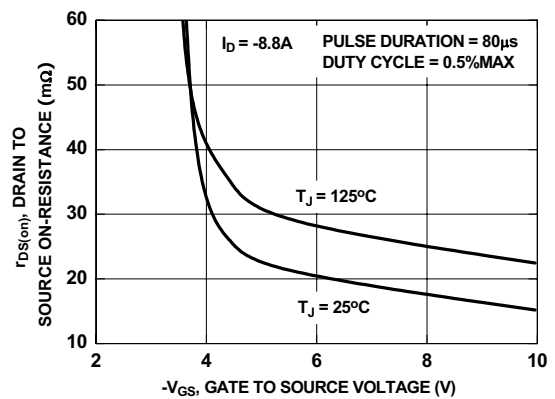


Figure 4. On-Resistance vs Gate to Source Voltage

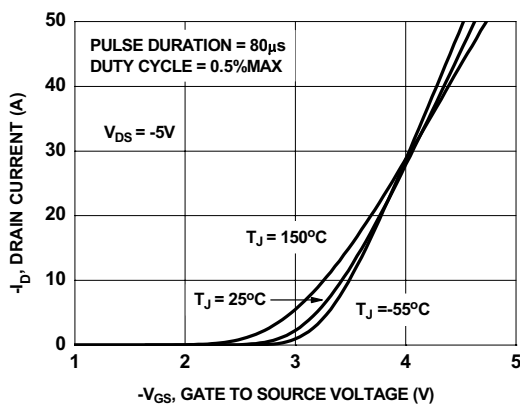


Figure 5. Transfer Characteristics

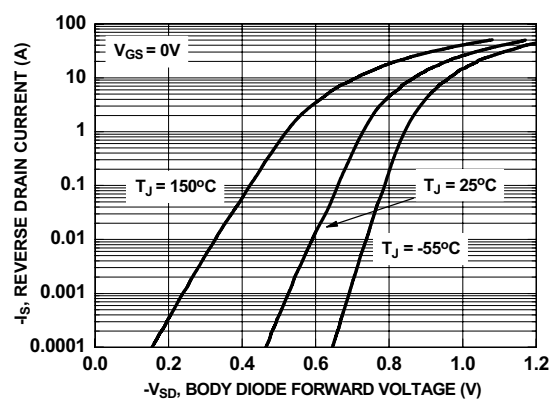


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

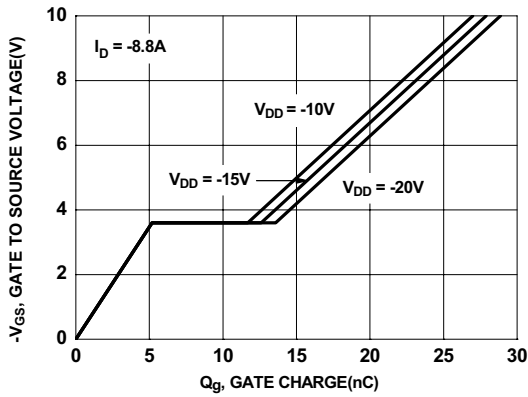


Figure 7. Gate Charge Characteristics

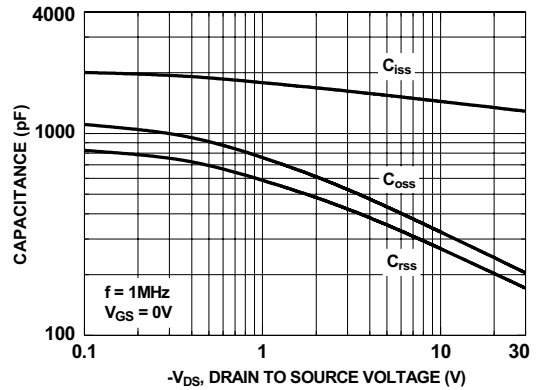


Figure 8. Capacitance vs Drain to Source Voltage

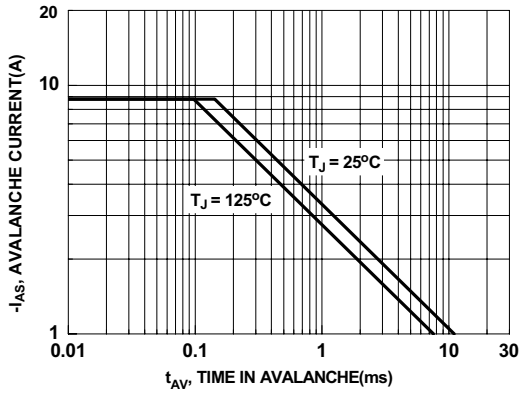


Figure 9. Unclamped Inductive Switching Capability

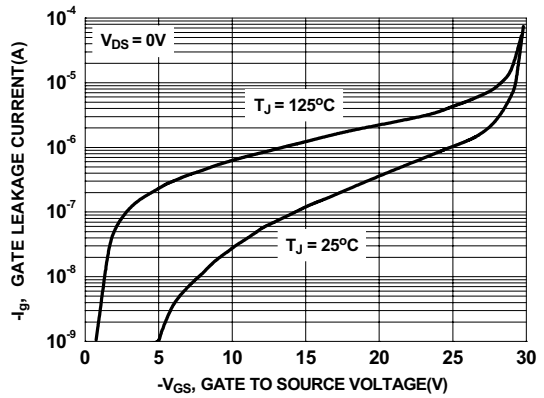


Figure 10. Gate Leakage Current vs Gate to Source Voltage

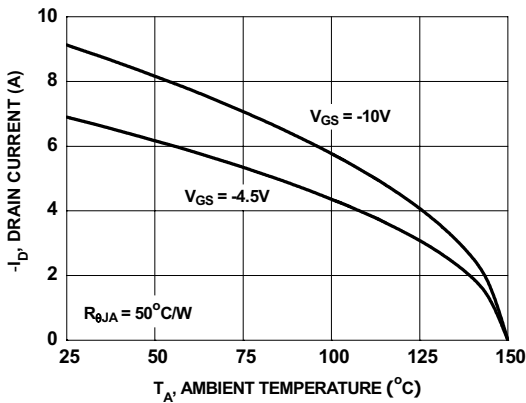


Figure 11. Maximum Continuous Drain Current vs Ambient Temperature

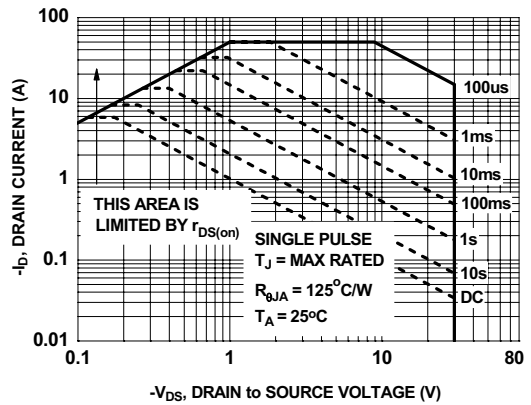


Figure 12. Forward Bias Safe Operating Area

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

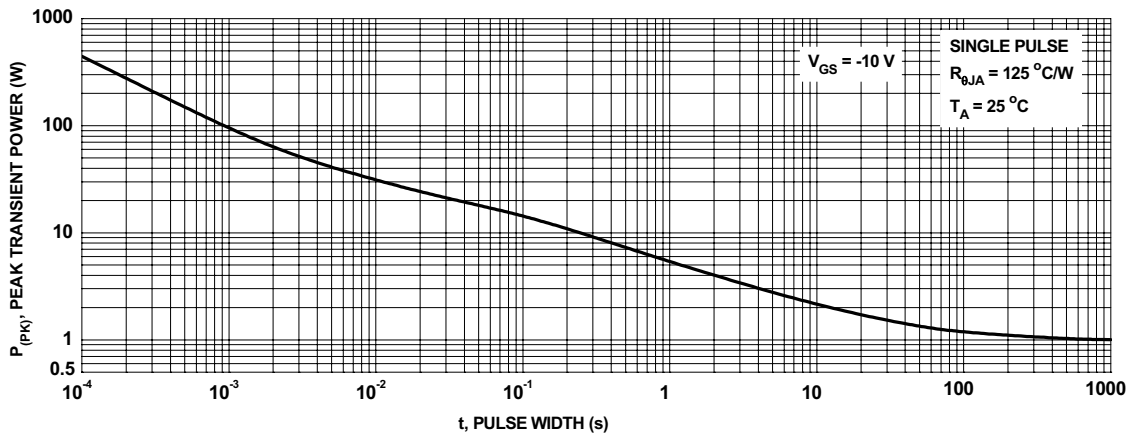


Figure 13. Single Pulse Maximum Power Dissipation

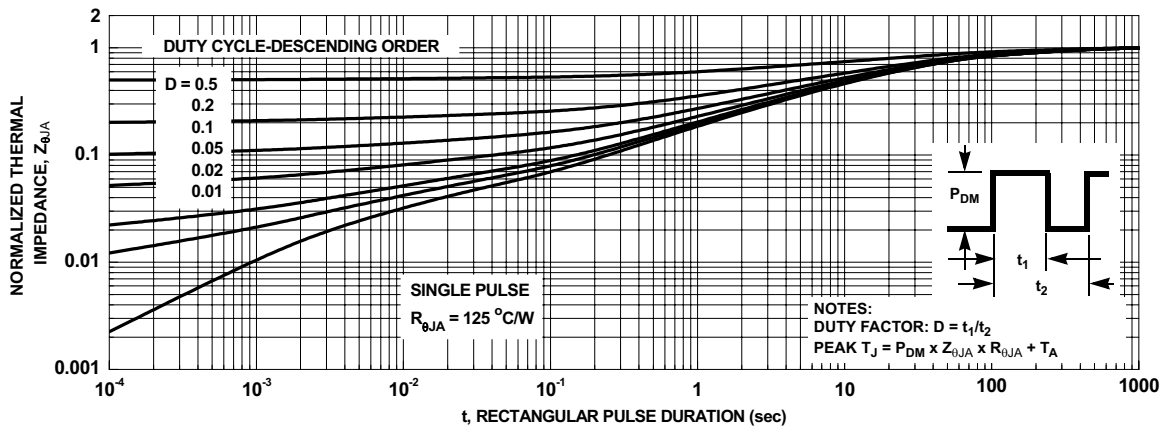








Figure 14. Transient Thermal Response Curve



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