

FDW2507NZ

Dual N-Channel 2.5V specified PowerTrench® MOSFET

General Description

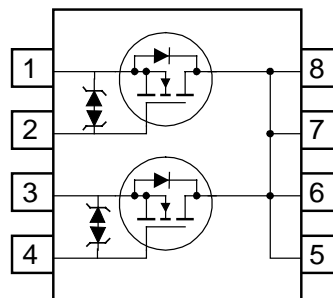
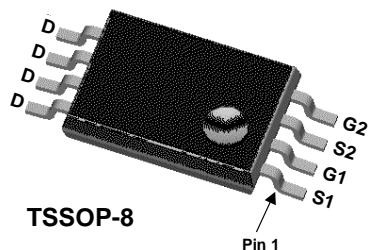
This dual N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced PowerTrench process to optimize the $R_{DS(ON)}$ @ $V_{GS} = 2.5V$ on special TSSOP-8 lead frame with all the drains on one side of the package.

Applications

- Li-Ion Battery Pack

Features

- 7.5 A, 20 V $R_{DS(ON)} = 19\text{ m}\Omega$ @ $V_{GS} = 4.5\text{ V}$
 $R_{DS(ON)} = 23\text{ m}\Omega$ @ $V_{GS} = 2.5\text{ V}$
- Isolated source and drain pins
- ESD protection diode (note 3)
- High performance trench technology for extremely low $R_{DS(ON)}$ @ $V_{GS} = 2.5\text{ V}$
- Low profile TSSOP-8 package



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous (Note 1a)	7.5	A
	– Pulsed	30	
P_D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.6	W
		1.1	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	77	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	114	$^\circ\text{C/W}$

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2507NZ	FDW2507NZ	13"	12mm	3000 units

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		-13		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	μA
I_{GSSF}	Gate–Body Leakage, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			10	μA
I_{GSSR}	Gate–Body Leakage, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-10	μA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	0.8	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C		4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 7.5\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 6.8\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 7.5\text{ A}, T_J = 125^\circ\text{C}$		15 17 20	19 23 27	m Ω
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	30			A
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 7.5\text{ A}$		31		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2152		pF
C_{oss}	Output Capacitance			512		pF
C_{riss}	Reverse Transfer Capacitance			263		pF

Switching Characteristics (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		12	22	ns
t_r	Turn–On Rise Time			13	23	ns
$t_{d(off)}$	Turn–Off Delay Time			35	56	ns
t_f	Turn–Off Fall Time			19	34	ns
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 4.5\text{ V}$		20	28	nC
Q_{gs}	Gate–Source Charge			3		nC
Q_{gd}	Gate–Drain Charge			5		nC

Drain–Source Diode Characteristics and Maximum Ratings

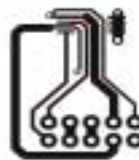
I_S	Maximum Continuous Drain–Source Diode Forward Current			1.3		A
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)		0.6	1.2	V
t_{rr}	Diode Reverse Recovery Time	$I_F = 7.5\text{ A}$		26		nS
Q_{rr}	Diode Reverse Recovery Charge	$d_I/d_t = 100\text{ A}/\mu\text{s}$ (Note 2)		21		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



- a) $77^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



- b) $114^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < $300\ \mu\text{s}$, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics

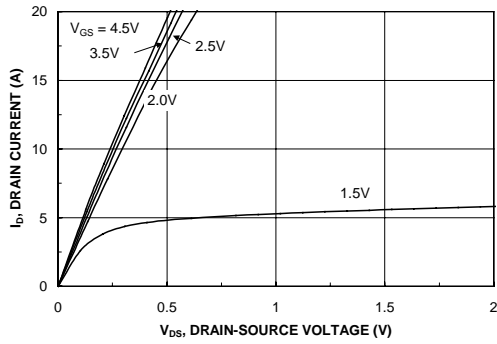


Figure 1. On-Region Characteristics.

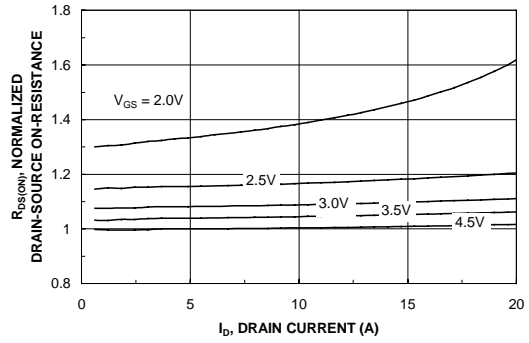


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

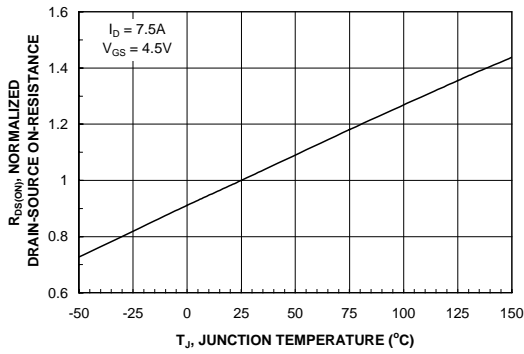


Figure 3. On-Resistance Variation with Temperature.

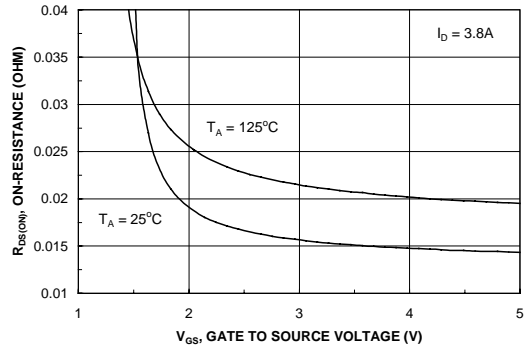


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

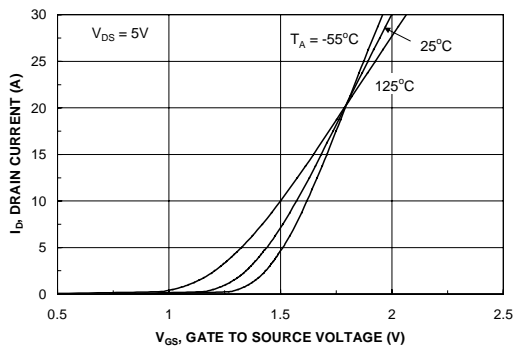


Figure 5. Transfer Characteristics.

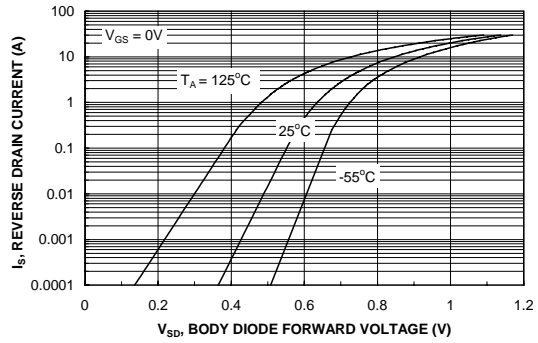


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

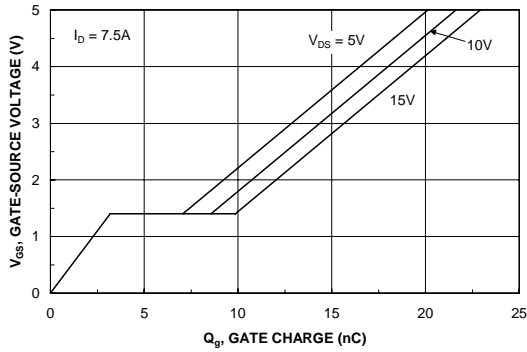


Figure 7. Gate Charge Characteristics.

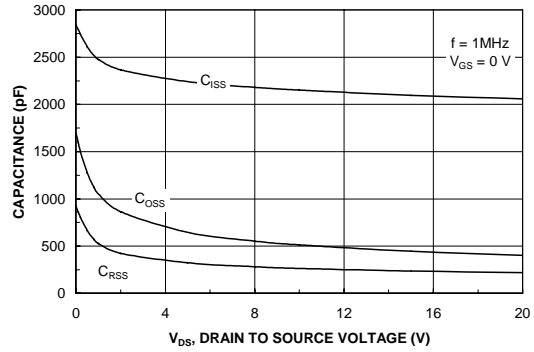


Figure 8. Capacitance Characteristics.

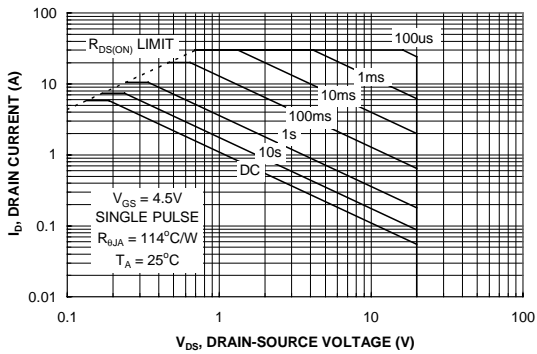


Figure 9. Maximum Safe Operating Area.

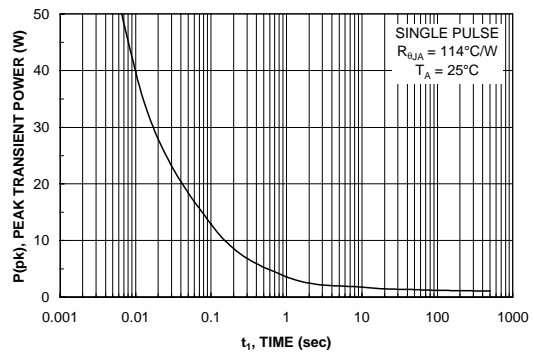


Figure 10. Single Pulse Maximum Power Dissipation.

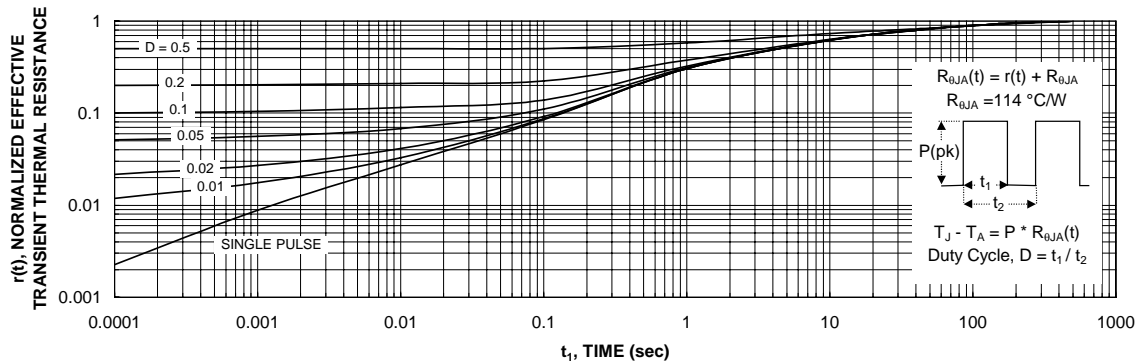


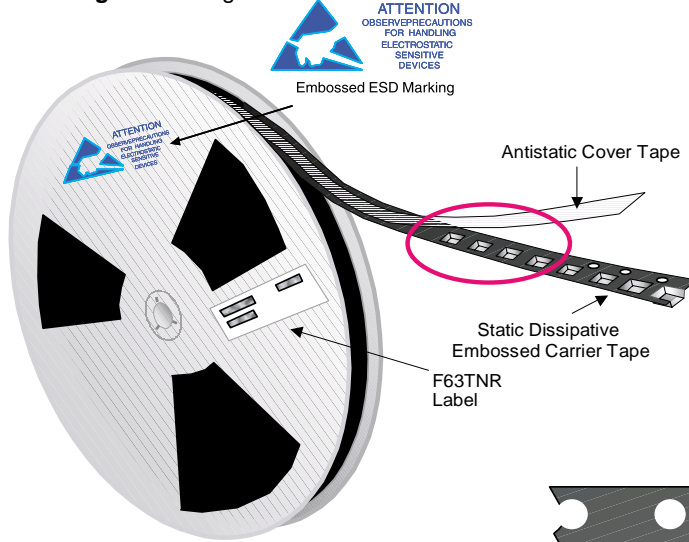
Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

TSSOP(8lds) Tape and Reel Data



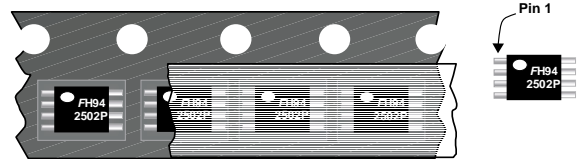
TSSOP(8lds) Packaging Configuration: Figure 1.0



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Packaging Description:
TSSOP-8lds parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are white in color and is made of polystyrene plastic (anti-static coated).
These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains one reel. These boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.

TSSOP (8lds) Packaging Information	
Packaging Option	Standard (no flow code)
Packaging type	TNR
Qty per Reel/Tube/Bag	2,500
Reel Size	13" Dia
Box Dimension (mm)	355x333x40
Max qty per Box	5,000
Weight per unit (gm)	0.020
Weight per Reel (kg)	0.426
Note/Comments	

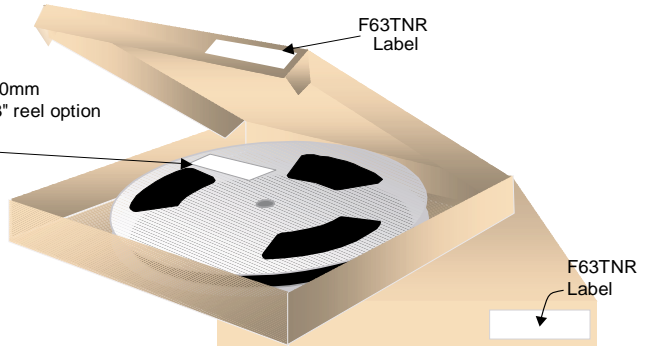


TSSOP-8lds Unit Orientation

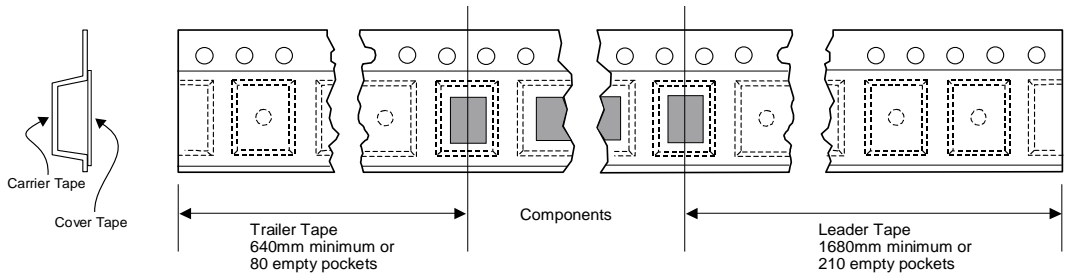
355mm x 333mm x 40mm
Intermediate container for 13" reel option

F63TNR Label sample

LOT: CBHK741B019 QTY: 2500
 PART ID: FDW2502P SPEC:
 D/C1: H9942AB QTY1: SPEC REV:
 D/G2: FAIRCHILD SEMICONDUCTOR CORPORATION (F63TNR)3.2

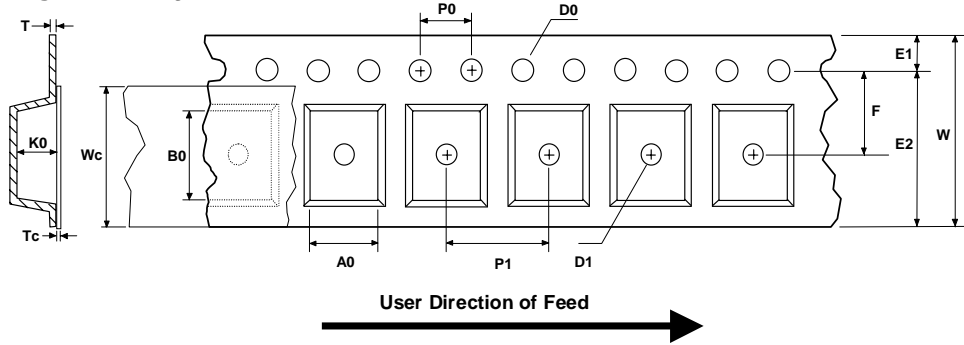


TSSOP(8lds) Tape Leader and Trailer Configuration: Figure 2.0



TSSOP(8lds) Tape and Reel Data, continued

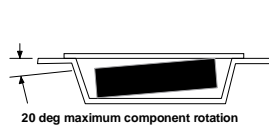
TSSOP(8lds) Embossed Carrier Tape Configuration: Figure 1.0



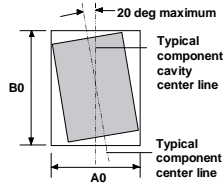
Dimensions are in millimeter

Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
TSSOP(8lds) (16mm)	see notes below	see notes below	16.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	14.25 min	7.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	see notes below	0.450 +/- 0.150	13.0 +/-0.3	0.06 +/-0.02

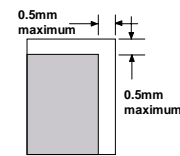
Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

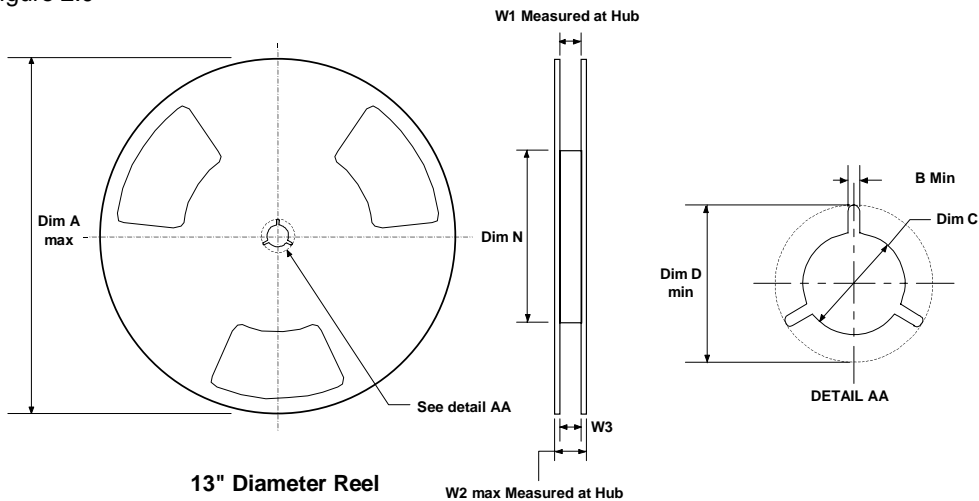


Sketch B (Top View)
Component Rotation



Sketch C (Top View)
Component lateral movement

TSSOP(8lds) Reel Configuration: Figure 2.0



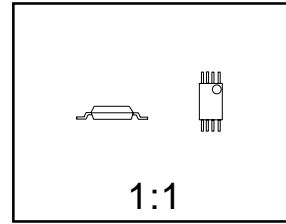
Dimensions are in inches and millimeters

Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
16mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 101.6	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.626 - 0.764 15.9 - 19.4

TSSOP-8 Package Dimensions



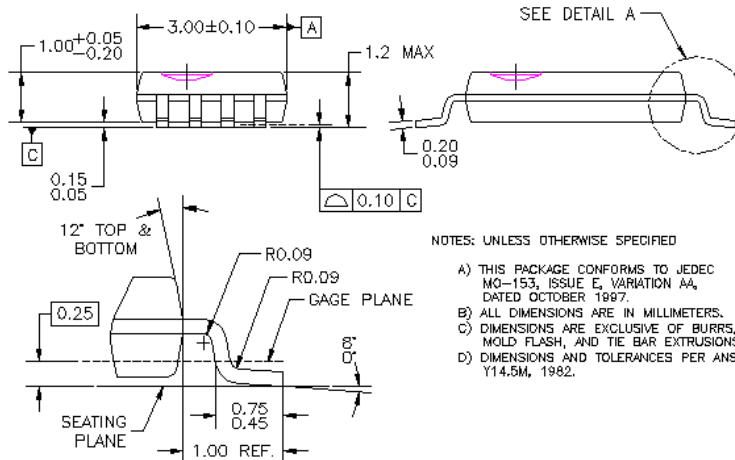
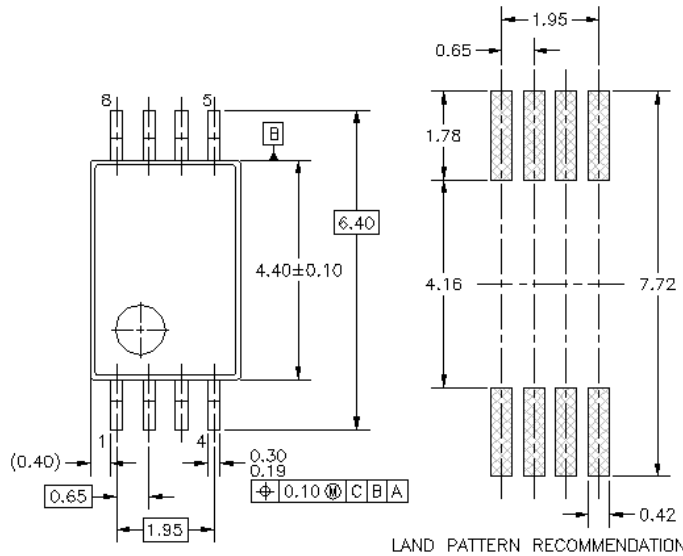
TSSOP-8 (FS PKG Code S4)



Scale 1:1 on letter size paper

Dimensions shown below are in millimeters

Part Weight per unit (gram): 0.0334



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE CONFORMS TO JEDEC MO-153, ISSUE E, VARIATION AA, DATED OCTOBER 1987.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D) DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

DETAIL A
SCALE: 2X
MTC00BREV8

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DOMET TM	HiSeC TM	PowerTrench [®]	SuperSOT TM -8	
EcoSPARK TM	ISOPLANAR TM	QFET TM	SyncFET TM	
E ² CMOS TM	LittleFET TM	QST TM	TinyLogic TM	
EnSigna TM	MicroFET TM	QT Optoelectronics TM	TruTranslation TM	
FACT TM	MicroPak TM	Quiet Series TM	UHC TM	
FACT Quiet Series TM	MICROWIRE TM	SILENT SWITCHER [®]	UltraFET [®]	

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.



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