

FQA170N06

60V N-Channel MOSFET

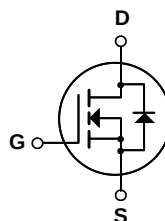
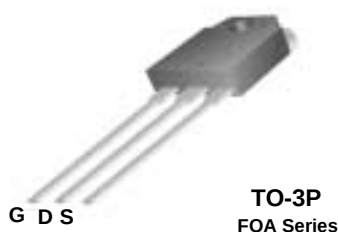
General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for low voltage applications such as automotive, DC/DC converters, and high efficiency switching for power management in portable and battery operated products.

Features

- 170A, 60V, $R_{DS(on)} = 0.0056\Omega$ @ $V_{GS} = 10\text{ V}$
- Low gate charge (typical 220 nC)
- Low C_{rss} (typical 620 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- 175°C maximum junction temperature rating



Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FQA170N06	Units
V_{DSS}	Drain-Source Voltage	60	V
I_D	Drain Current - Continuous ($T_C = 25^\circ\text{C}$) - Continuous ($T_C = 100^\circ\text{C}$)	170	A
		120	A
I_{DM}	Drain Current - Pulsed (Note 1)	680	A
V_{GSS}	Gate-Source Voltage	± 25	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	990	mJ
I_{AR}	Avalanche Current (Note 1)	170	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	37.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	7.0	V/ns
P_D	Power Dissipation ($T_C = 25^\circ\text{C}$) - Derate above 25°C	375	W
		2.5	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +175	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	0.4	°C/W
$R_{\theta CS}$	Thermal Resistance, Case-to-Sink	0.24	--	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	40	°C/W

Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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Off Characteristics

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to 25°C	--	0.053	--	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	μA
		$V_{DS} = 48\text{ V}, T_C = 150^\circ\text{C}$	--	--	10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 85\text{ A}$	--	0.0045	0.0056	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 30\text{ V}, I_D = 85\text{ A}$ (Note 4)	--	85	--	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	7200	9350	pF
C_{oss}	Output Capacitance		--	3100	4000	pF
C_{rss}	Reverse Transfer Capacitance		--	620	810	pF

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 30\text{ V}, I_D = 85\text{ A},$ $R_G = 25\text{ }\Omega$ (Note 4, 5)	--	85	180	ns
t_r	Turn-On Rise Time		--	700	1400	ns
$t_{d(off)}$	Turn-Off Delay Time		--	260	530	ns
t_f	Turn-Off Fall Time		--	430	870	ns
Q_g	Total Gate Charge	$V_{DS} = 48\text{ V}, I_D = 170\text{ A},$ $V_{GS} = 10\text{ V}$ (Note 4, 5)	--	220	290	nC
Q_{gs}	Gate-Source Charge		--	50	--	nC
Q_{gd}	Gate-Drain Charge		--	100	--	nC

Drain-Source Diode Characteristics and Maximum Ratings

I _S	Maximum Continuous Drain-Source Diode Forward Current		--	--	170	A
I _{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	680	A
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 170 A	--	--	1.5	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 170 A,	--	100	--	ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs (Note 4)	--	315	--	nC

Notes:

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. $L = 40\text{ }\mu\text{H}$, $I_{AS} = 170\text{ A}$, $V_{DD} = 25\text{ V}$, $R_G = 25\text{ }\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 170\text{ A}$, $dI/dt \leq 300\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width $\leq 300\text{ }\mu\text{s}$, Duty cycle $\leq 2\%$
5. Essentially independent of operating temperature
6. Continuous Drain Current Calculated by Maximum Junction Temperature : Limited by Package

Typical Characteristics

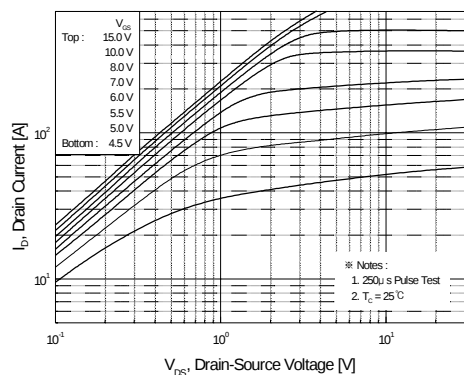


Figure 1. On-Region Characteristics.

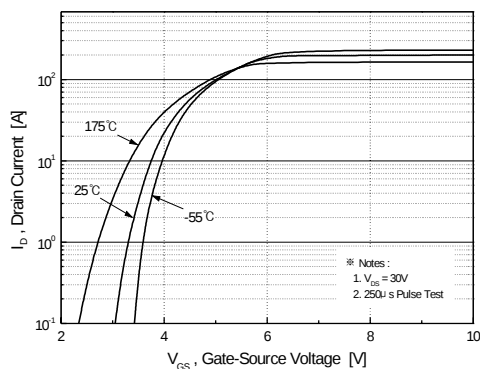


Figure 2. Transfer Characteristics.

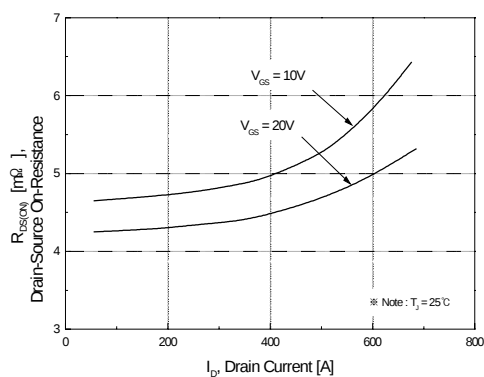


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage.

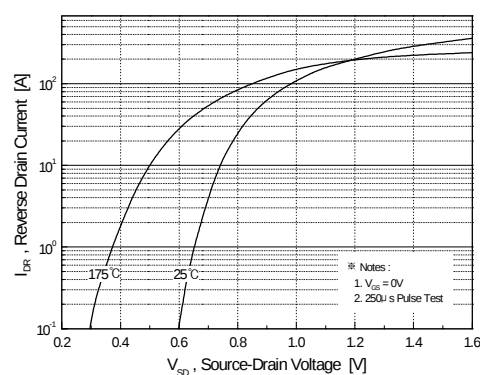


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature.

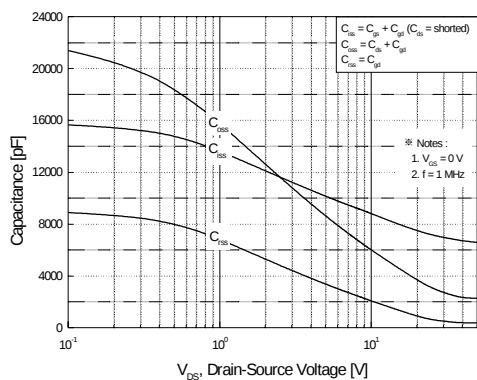


Figure 5. Capacitance Characteristics.

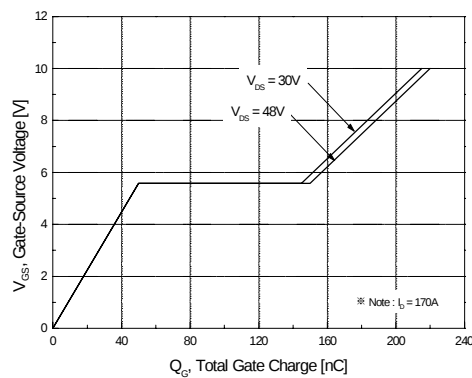


Figure 6. Gate -Charge Characteristics.

Typical Characteristics (Continued)

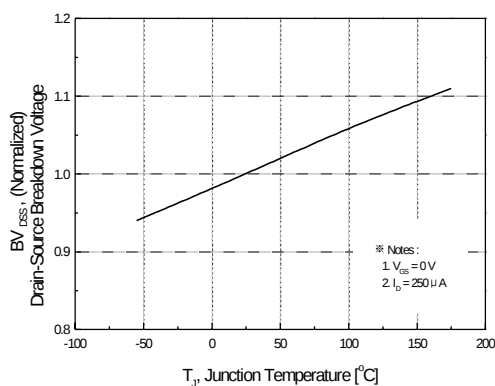


Figure 7. Breakdown Voltage Variation vs Temperature.

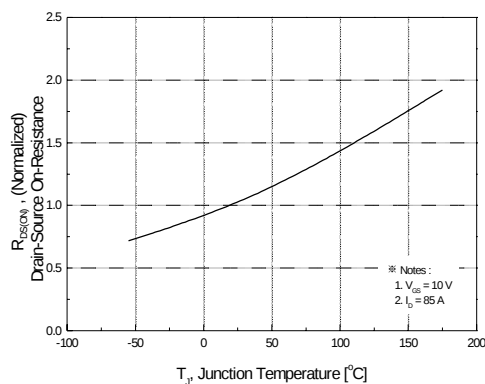


Figure 8. On-Resistance Variation vs Temperature.

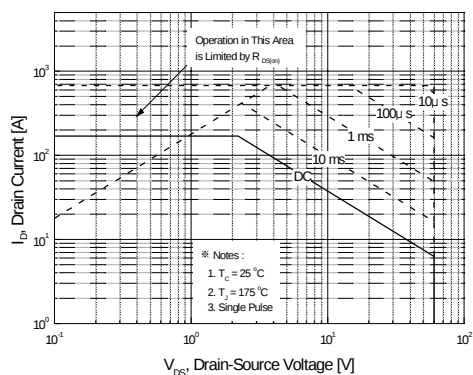


Figure 9. Maximum Safe Operating Area.

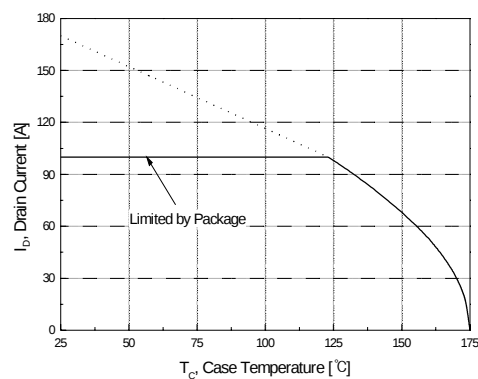


Figure 10. Maximum Drain Current vs Case Temperature.

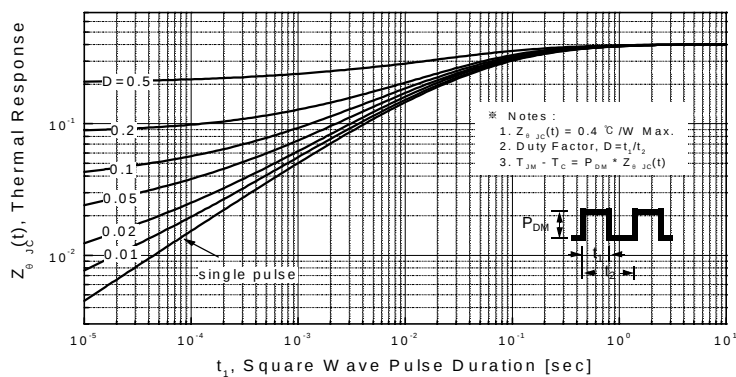


Figure 11. Transient Thermal Response Curve.

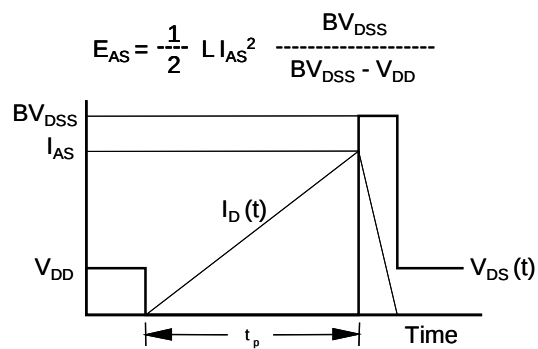
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

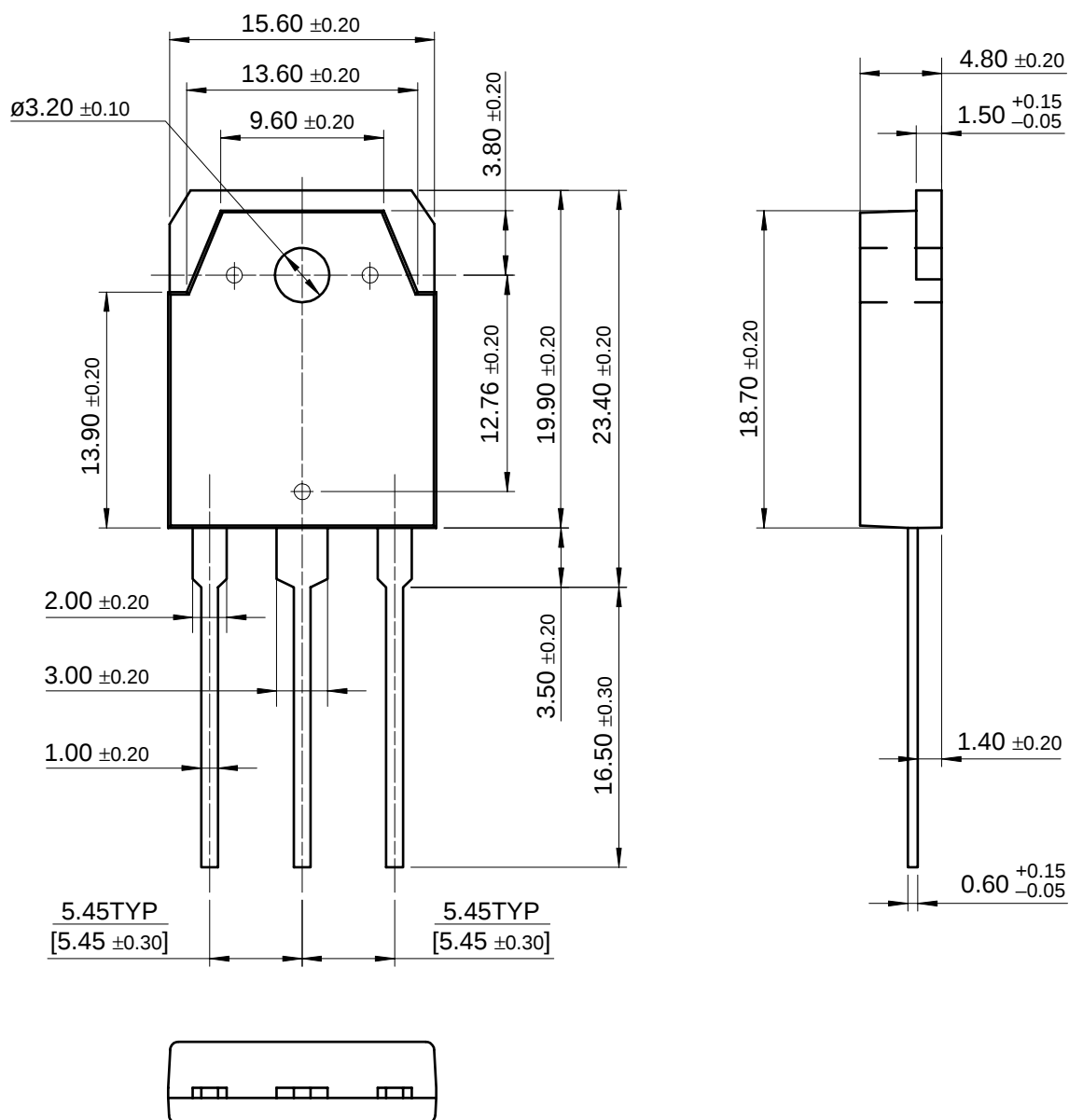


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-3P



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