

FDB12N50

N-Channel UniFET™ MOSFET

500 V, 11.5 A, 650 mΩ

Features

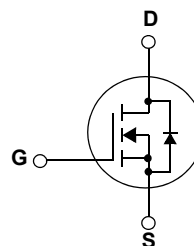
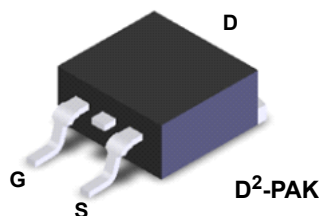
- $R_{DS(on)} = 550 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 6 \text{ A}$
- Low Gate Charge (Typ. 22 nC)
- Low C_{rss} (Typ. 12 pF)
- 100% Avalanche Tested
- RoHS Compliant

Applications

- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	FDB12N50	Unit
V_{DSS}	Drain to Source Voltage	500	V
V_{GSS}	Gate to Source Voltage	± 30	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	A
		- Continuous ($T_C = 100^\circ\text{C}$)	
I_{DM}	Drain Current	- Pulsed (Note 1)	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	mJ
I_{AR}	Avalanche Current	(Note 1)	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	W
		- Derate above 25°C	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Thermal Characteristics

Symbol	Parameter	FDB12N50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.75	$^\circ\text{C/W}$
$R_{\theta JA}^*$	Thermal Resistance, Junction to Ambient*	40	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

*When mounted on the minimum pad size recommended (PCB Mount)

Package Marking and Ordering Information $T_C = 25^\circ\text{C}$ unless otherwise noted

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDB12N50	FDB12N50TM	D ² -PAK	330mm	24mm	800

Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$, $T_J = 25^\circ\text{C}$	500	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.66	-	V/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}$, $V_{GS} = 0\text{V}$	-	-	1	μA
		$V_{DS} = 400\text{V}$, $T_C = 125^\circ\text{C}$	-	-	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}$, $V_{DS} = 0\text{V}$	-	-	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}$, $I_D = 6\text{A}$	-	0.55	0.65	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 25\text{V}$, $I_D = 6\text{A}$	-	11	-	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	985	1315	pF
C_{oss}	Output Capacitance		-	140	190	pF
C_{rss}	Reverse Transfer Capacitance		-	12	17	pF
Q_g	Total Gate Charge at 10V	$V_{DS} = 400\text{V}$, $I_D = 11.5\text{A}$ $V_{GS} = 10\text{V}$ (Note 4)	-	22	30	nC
Q_{gs}	Gate to Source Gate Charge		-	6	-	nC
Q_{gd}	Gate to Drain "Miller" Charge		-	10	-	nC

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}$, $I_D = 11.5\text{A}$ $R_G = 25\Omega$ (Note 4)	-	25	60	ns
t_r	Turn-On Rise Time		-	60	130	ns
$t_{d(off)}$	Turn-Off Delay Time		-	45	105	ns
t_f	Turn-Off Fall Time		-	35	85	ns

Drain-Source Diode Characteristics

I _S	Maximum Continuous Drain to Source Diode Forward Current		-	-	11.5	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	46	A
V _{SD}	Drain to Source Diode Forward Voltage	V _{GS} = 0V, I _{SD} = 11.5A	-	-	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0V, I _{SD} = 11.5A	-	370	-	ns
Q _{rr}	Reverse Recovery Charge	dI _F /dt = 100A/μs	-	3.8	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. $L = 6.9\text{mH}$, $I_{AS} = 11.5\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$
3. $I_{SD} \leq 11.5\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25^\circ\text{C}$
4. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

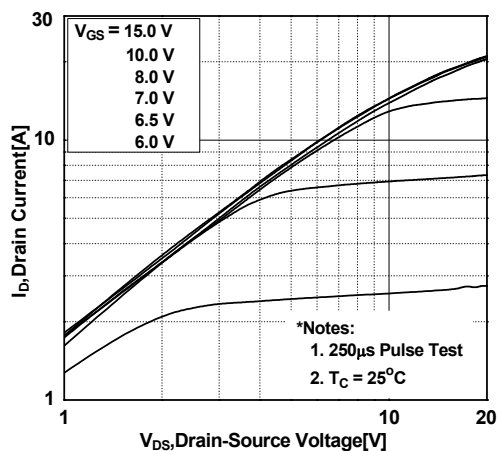


Figure 2. Transfer Characteristics

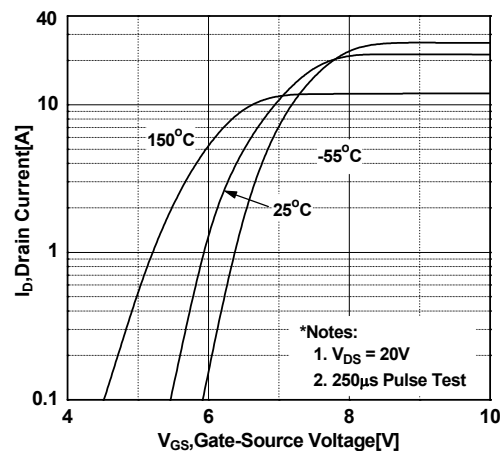


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

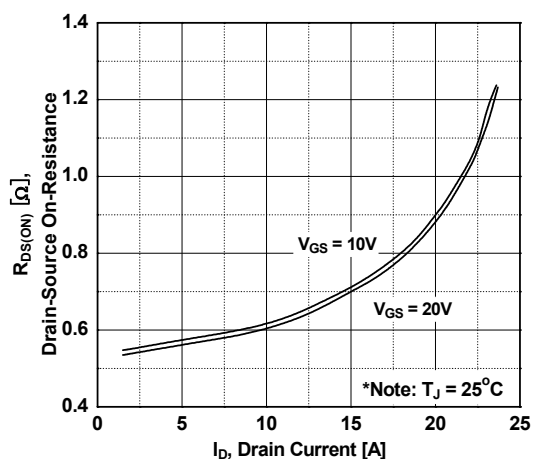


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

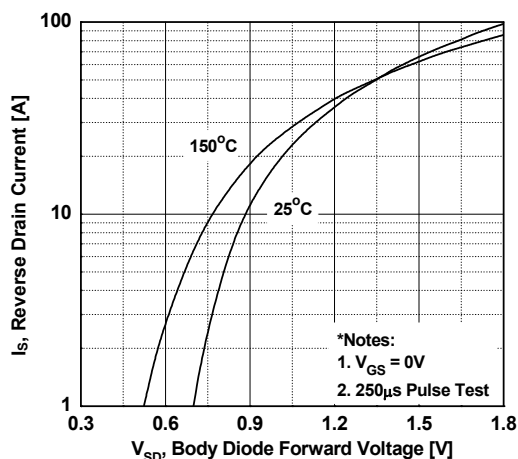


Figure 5. Capacitance Characteristics

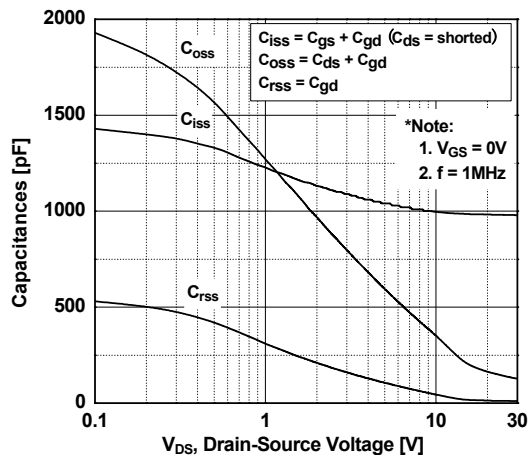
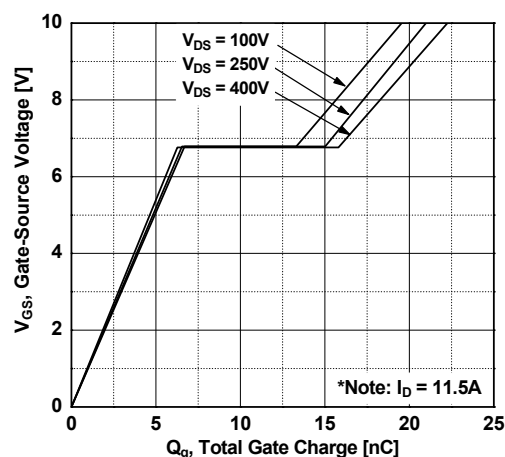


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

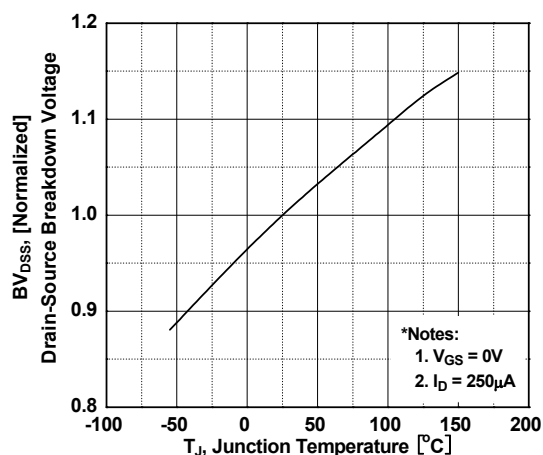


Figure 8. On-Resistance Variation vs. Temperature

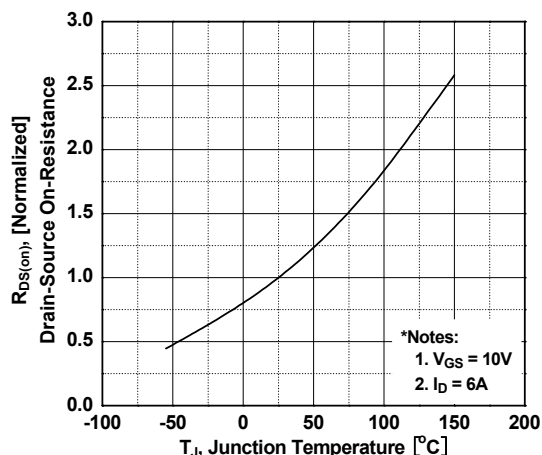


Figure 9. Maximum Safe Operating Area

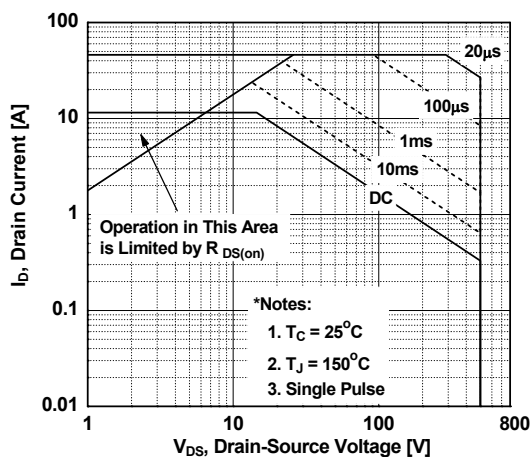


Figure 10. Maximum Drain Current vs. Case Temperature

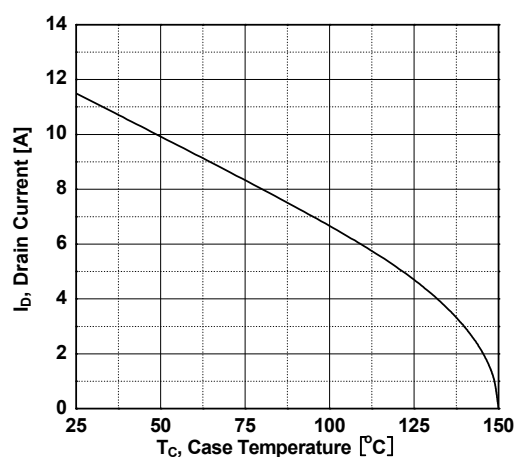
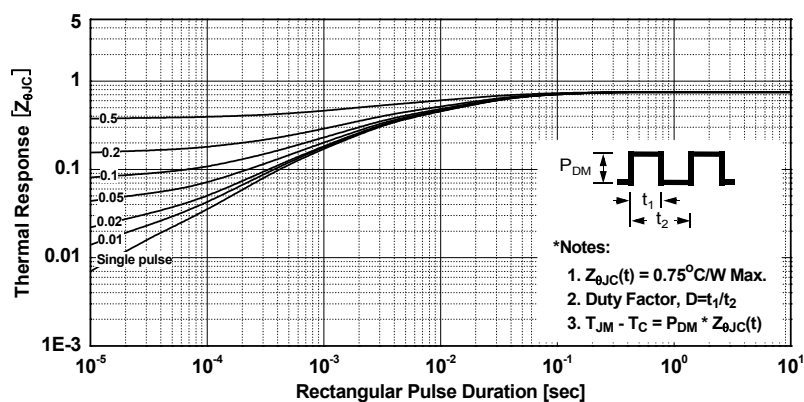
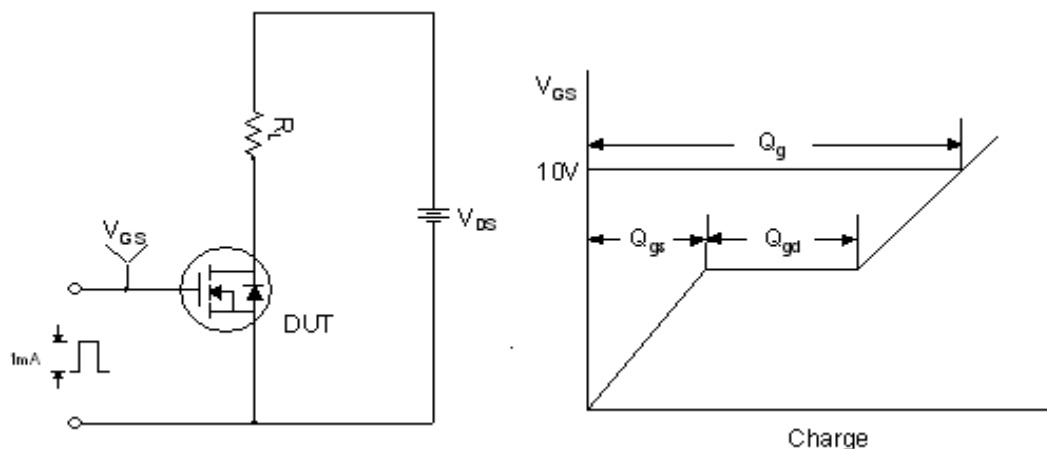


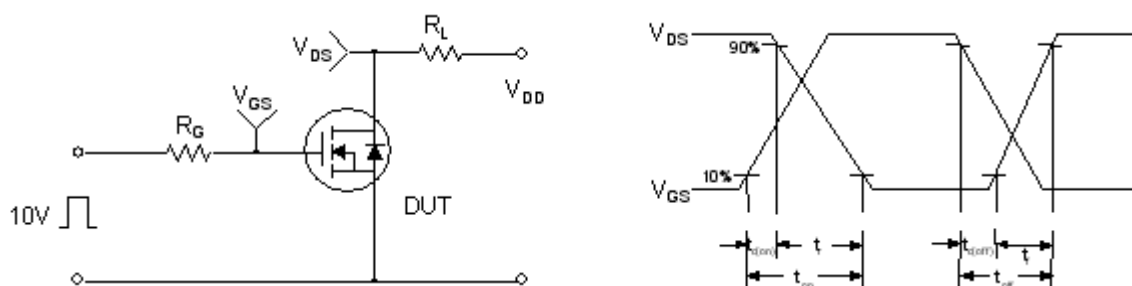
Figure 11. Transient Thermal Response Curve



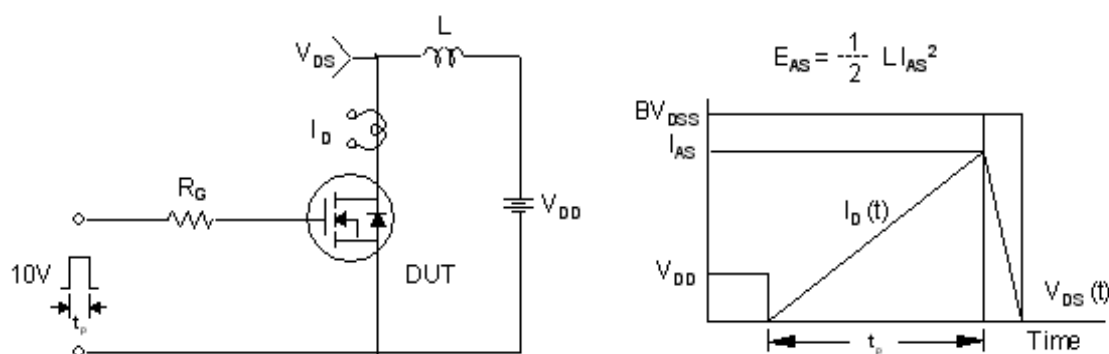
Gate Charge Test Circuit & Waveform



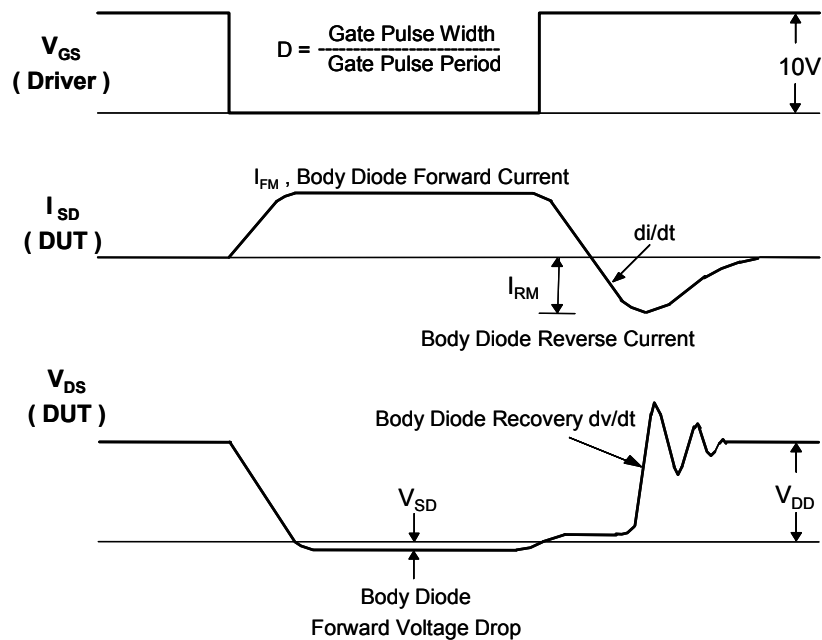
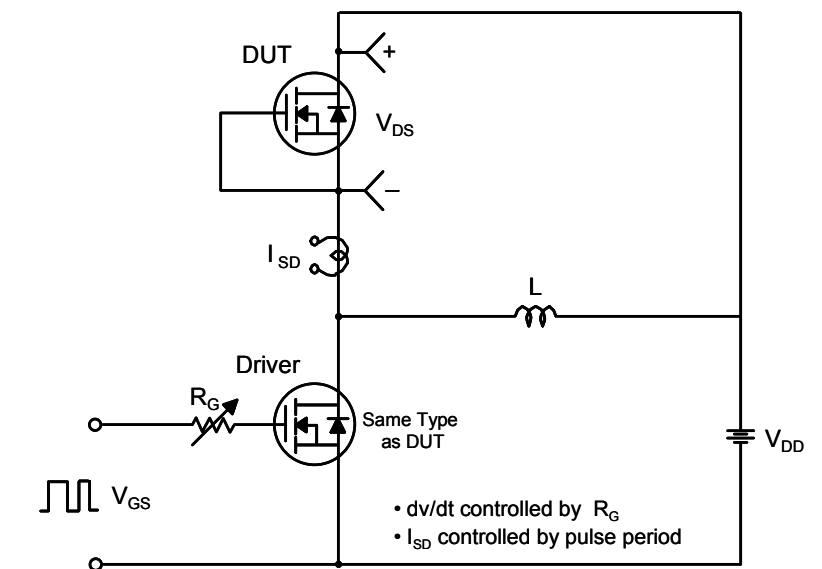
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

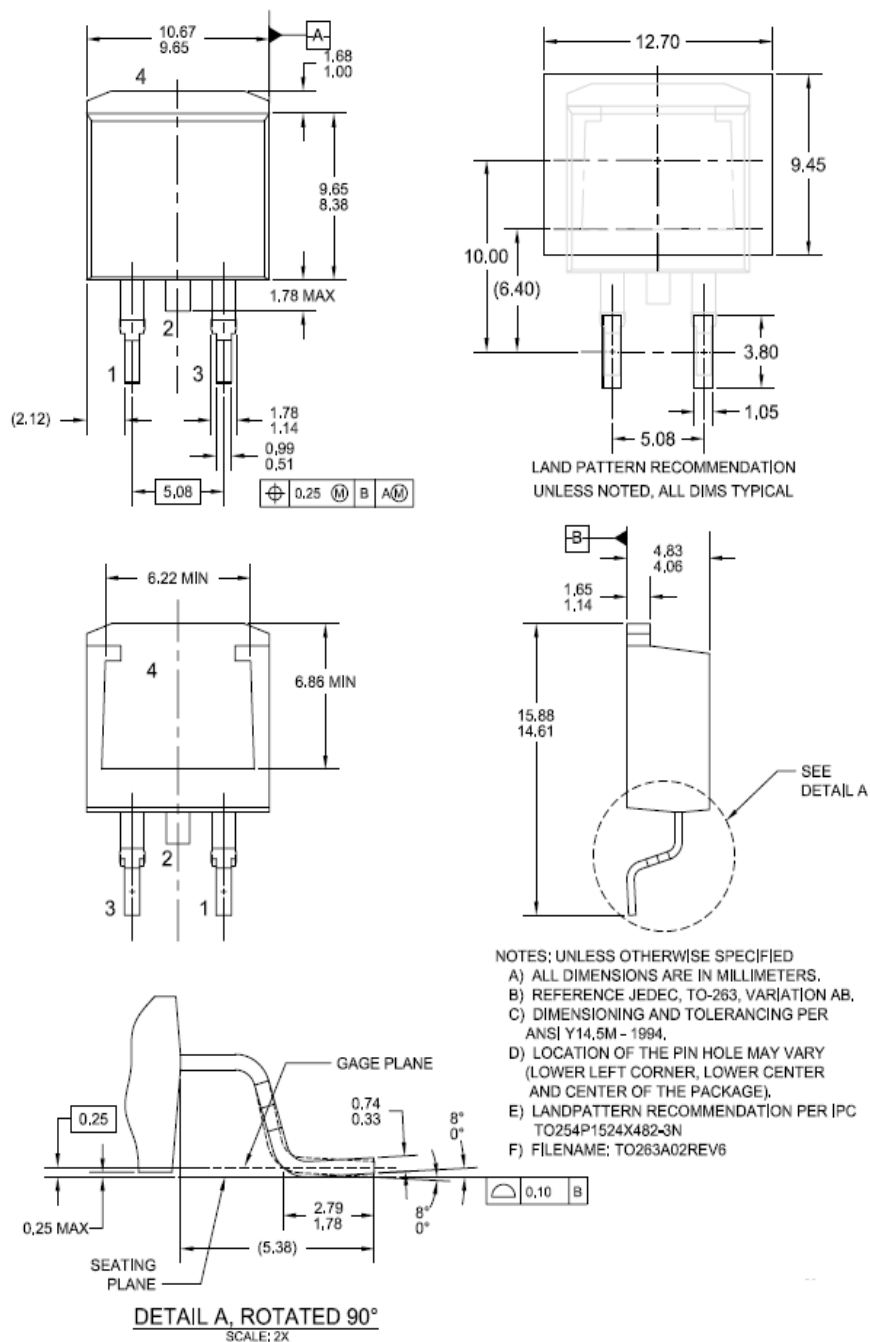


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

D²PAK



Dimensions in Millimeters



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