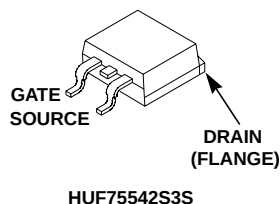
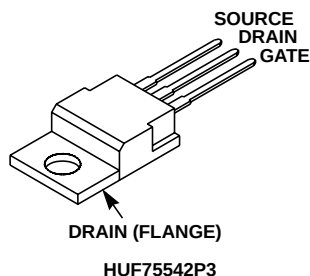


75A, 80V, 0.014 Ohm, N-Channel, UltraFET Power MOSFETs

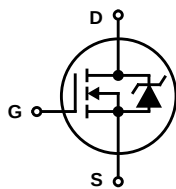
Packaging

JEDEC TO-220AB

JEDEC TO-263AB



Symbol



Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.014\Omega$, $V_{GS} = 10V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER® Electrical Models
 - Spice and SABER® Thermal Impedance Models
 - www.intersil.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75542P3	TO-220AB	75542P
HUF75542S3S	TO-263AB	75542S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUF75542S3ST.

Absolute Maximum Ratings $T_C = 25^\circ C$, Unless Otherwise Specified

	HUF75542P3, HUF75542S3S	UNITS
Drain to Source Voltage (Note 1)	V_{DSS} 80	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR} 80	V
Gate to Source Voltage	V_{GS} ± 20	V
Drain Current		
Continuous ($T_C = 25^\circ C$, $V_{GS} = 10V$) (Figure 2)	I_D 75	A
Continuous ($T_C = 100^\circ C$, $V_{GS} = 10V$) (Figure 2)	I_D 58	A
Pulsed Drain Current	I_{DM} Figure 4	
Pulsed Avalanche Rating	UIS Figures 6, 14, 15	
Power Dissipation	P_D 230	W
Derate Above $25^\circ C$	1.54	W/ $^\circ C$
Operating and Storage Temperature	T_J, T_{STG} -55 to 175	$^\circ C$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s.	T_L 300	$^\circ C$
Package Body for 10s, See Techbrief TB334.	T_{pkg} 260	$^\circ C$

NOTE:

1. $T_J = 25^\circ C$ to $150^\circ C$.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

HUF75542P3, HUF75542S3S

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV _{DSS}	I _D = 250μA, V _{GS} = 0V (Figure 11)	80	-	-	V	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 75V, V _{GS} = 0V	-	-	1	μA	
		V _{DS} = 70V, V _{GS} = 0V, T _C = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±20V	-	-	±100	nA	
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250μA (Figure 10)	2	-	4	V	
Drain to Source On Resistance	r _{DS(ON)}	I _D = 75A, V _{GS} = 10V (Figure 9)	-	0.012	0.014	Ω	
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	R _{θJC}	TO-220 and TO-263	-	-	0.65	°C/W	
Thermal Resistance Junction to Ambient	R _{θJA}		-	-	62	°C/W	
SWITCHING SPECIFICATIONS (V _{GS} = 10V)							
Turn-On Time	t _{ON}	V _{DD} = 40V, I _D = 75A V _{GS} = 10V, R _{GS} = 3.9Ω (Figures 18, 19)	-	-	195	ns	
Turn-On Delay Time	t _{d(ON)}		-	12.5	-	ns	
Rise Time	t _r		-	117	-	ns	
Turn-Off Delay Time	t _{d(OFF)}		-	50	-	ns	
Fall Time	t _f		-	80	-	ns	
Turn-Off Time	t _{OFF}		-	-	195	ns	
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	Q _{g(TOT)}	V _{GS} = 0V to 20V	V _{DD} = 40V, I _D = 75A, I _{g(REF)} = 1.0mA (Figures 13, 16, 17)	-	150	180	nC
Gate Charge at 10V	Q _{g(10)}	V _{GS} = 0V to 10V		-	80	96	nC
Threshold Gate Charge	Q _{g(TH)}	V _{GS} = 0V to 2V		-	5.7	7	nC
Gate to Source Gate Charge	Q _{gs}			-	15	-	nC
Gate to Drain "Miller" Charge	Q _{gd}			-	33	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C _{ISS}	V _{DS} = 25V, V _{GS} = 0V, f = 1MHz (Figure 12)	-	2750	-	pF	
Output Capacitance	C _{OSS}		-	700	-	pF	
Reverse Transfer Capacitance	C _{RSS}		-	250	-	pF	

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 75\text{A}$	-	-	1.25	V
		$I_{SD} = 37.5\text{A}$	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	102	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$	-	-	255	nC

Typical Performance Curves

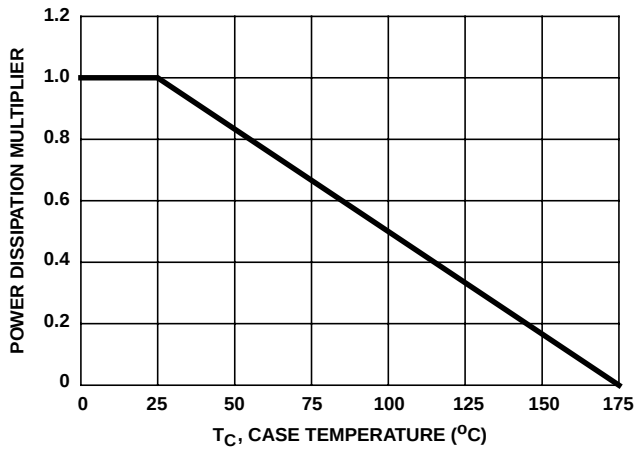


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

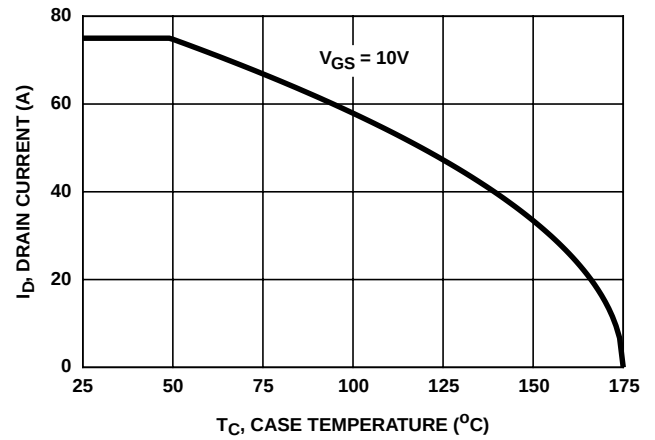


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

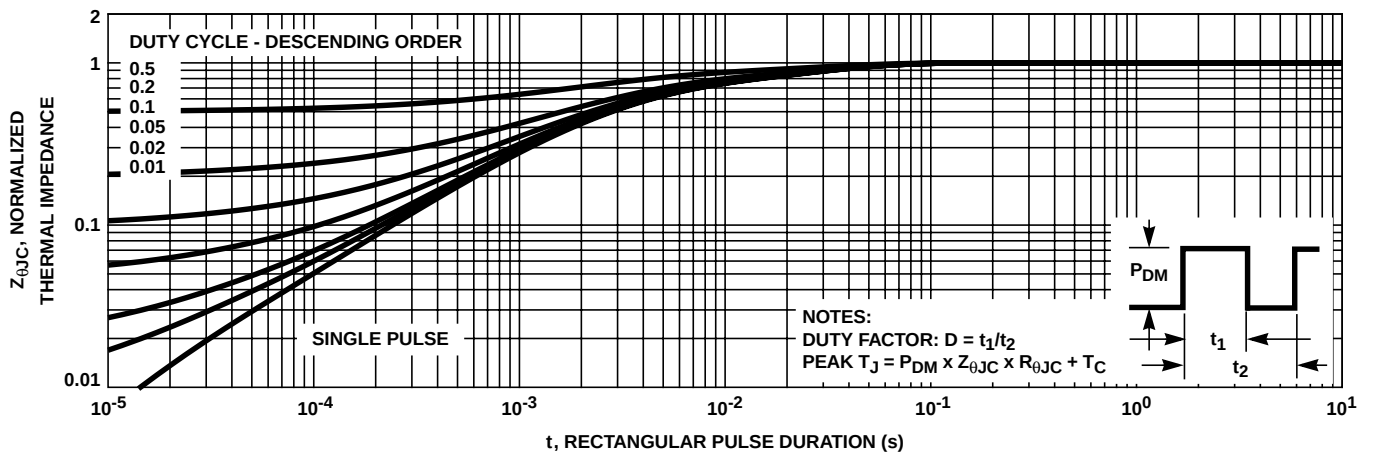


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

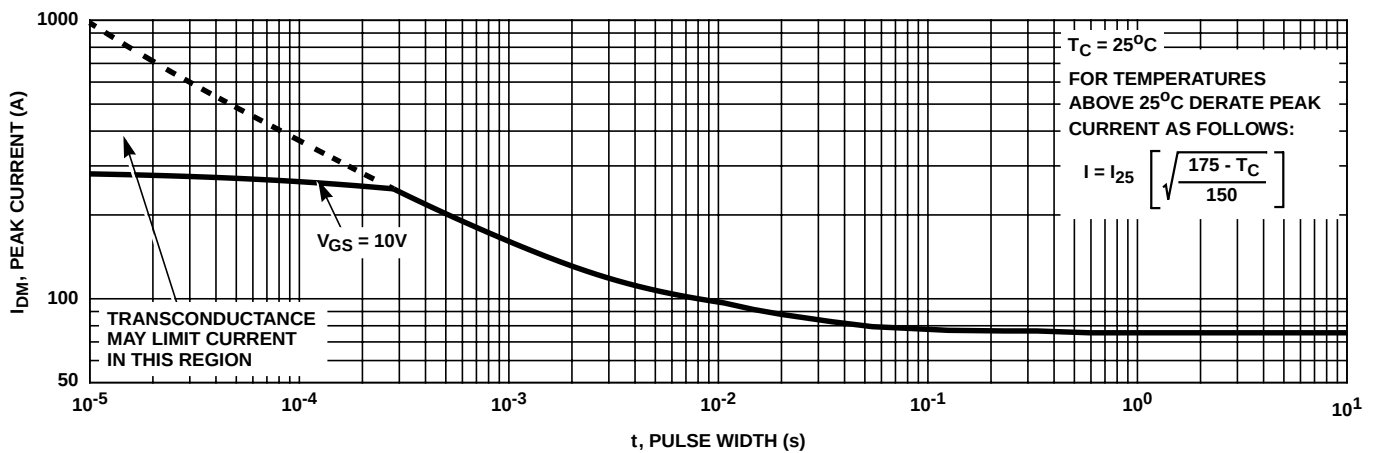


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

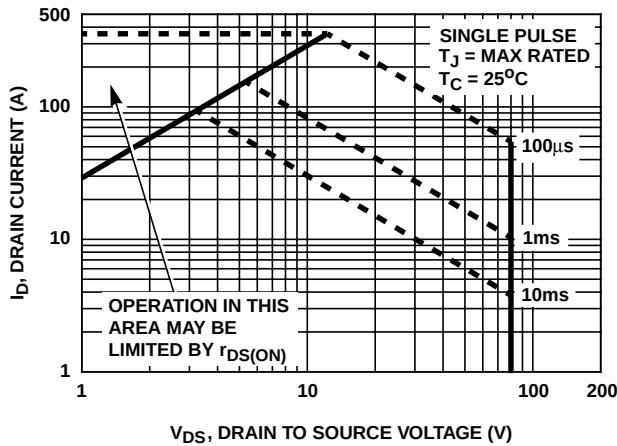
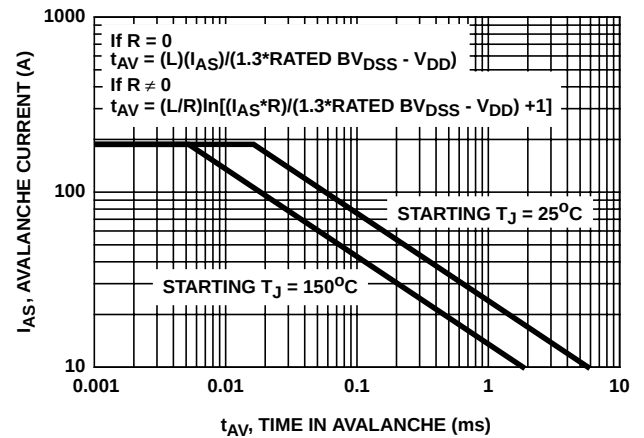


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

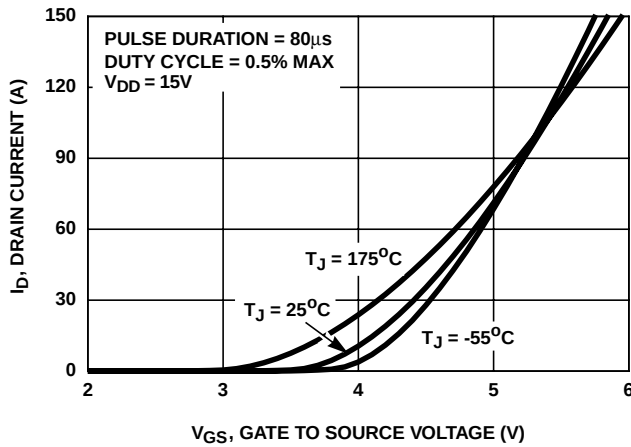


FIGURE 7. TRANSFER CHARACTERISTICS

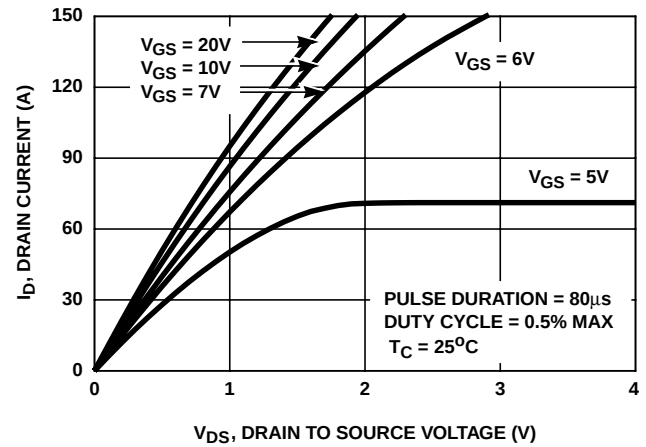


FIGURE 8. SATURATION CHARACTERISTICS

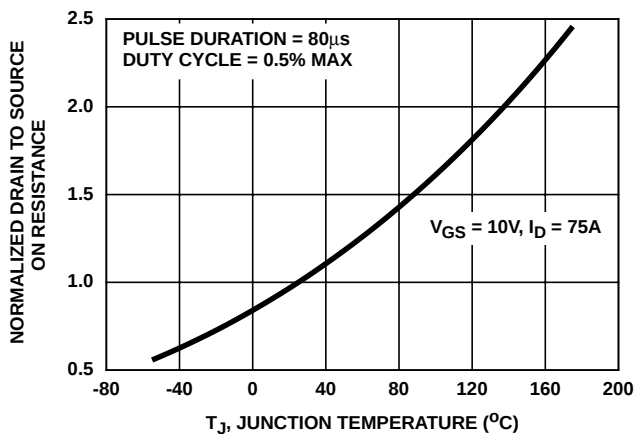


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

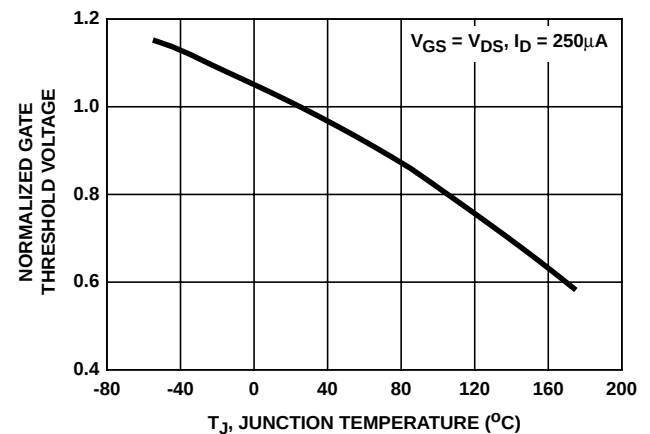


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

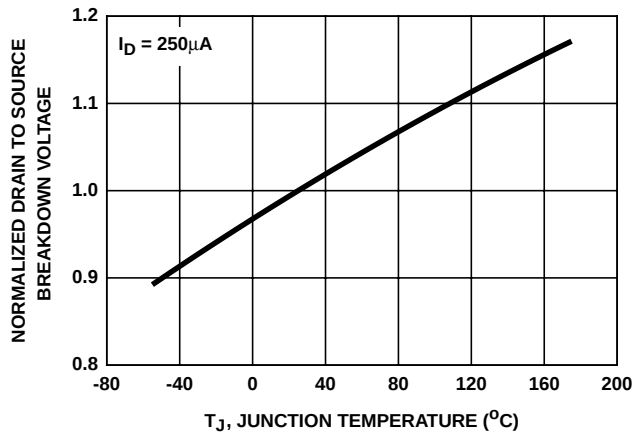


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

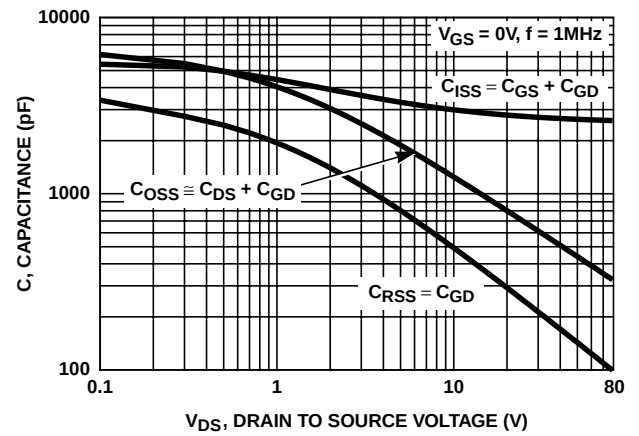
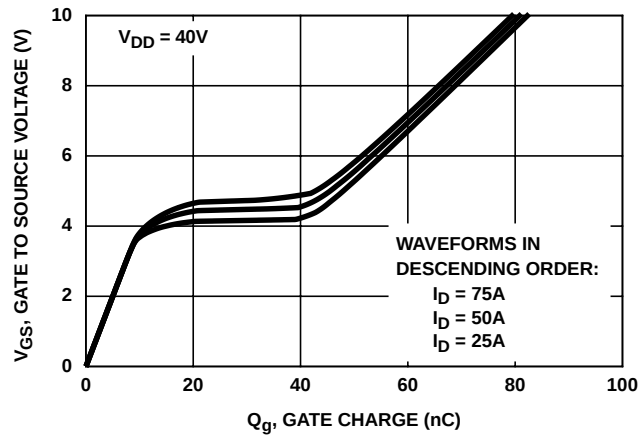


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

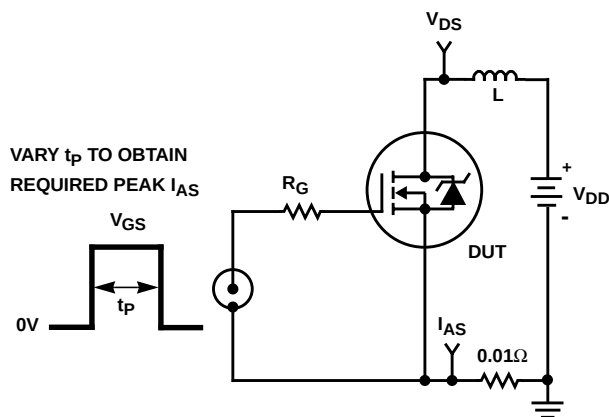


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

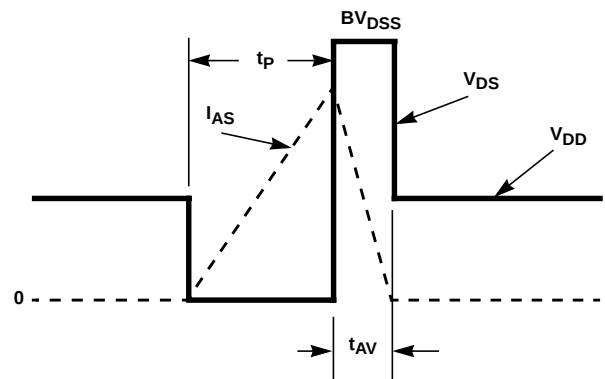


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

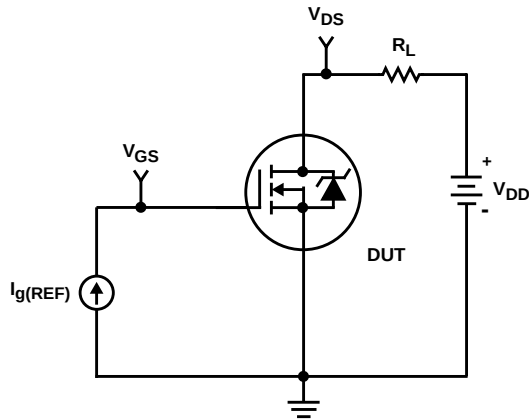


FIGURE 16. GATE CHARGE TEST CIRCUIT

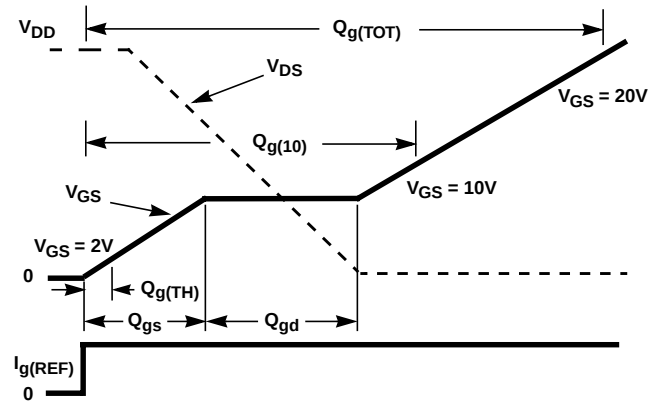


FIGURE 17. GATE CHARGE WAVEFORMS

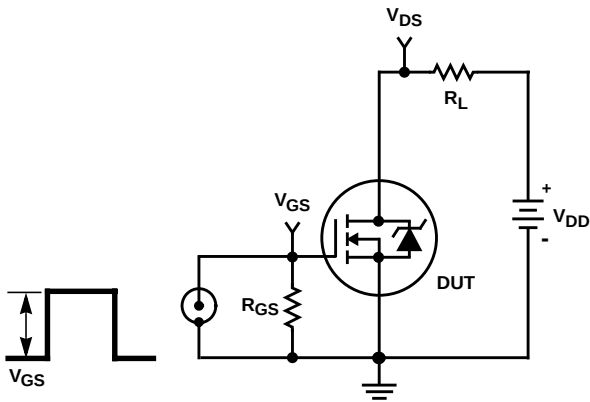


FIGURE 18. SWITCHING TIME TEST CIRCUIT

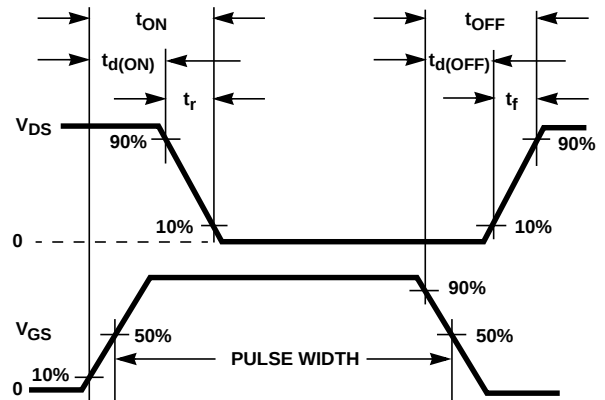


FIGURE 19. SWITCHING TIME WAVEFORM

PSPICE Electrical Model

.SUBCKT HUF75542P3 2 1 3 ; rev 15 Feb 2000

CA 12 8 4.4e-9
CB 15 14 4.2e-9
CIN 6 8 2.5e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 87.2
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9
LGATE 1 9 2.6e-9
LSOURCE 3 7 1.1e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 5.5e-3
RGATE 9 20 1.0
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 3.3e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

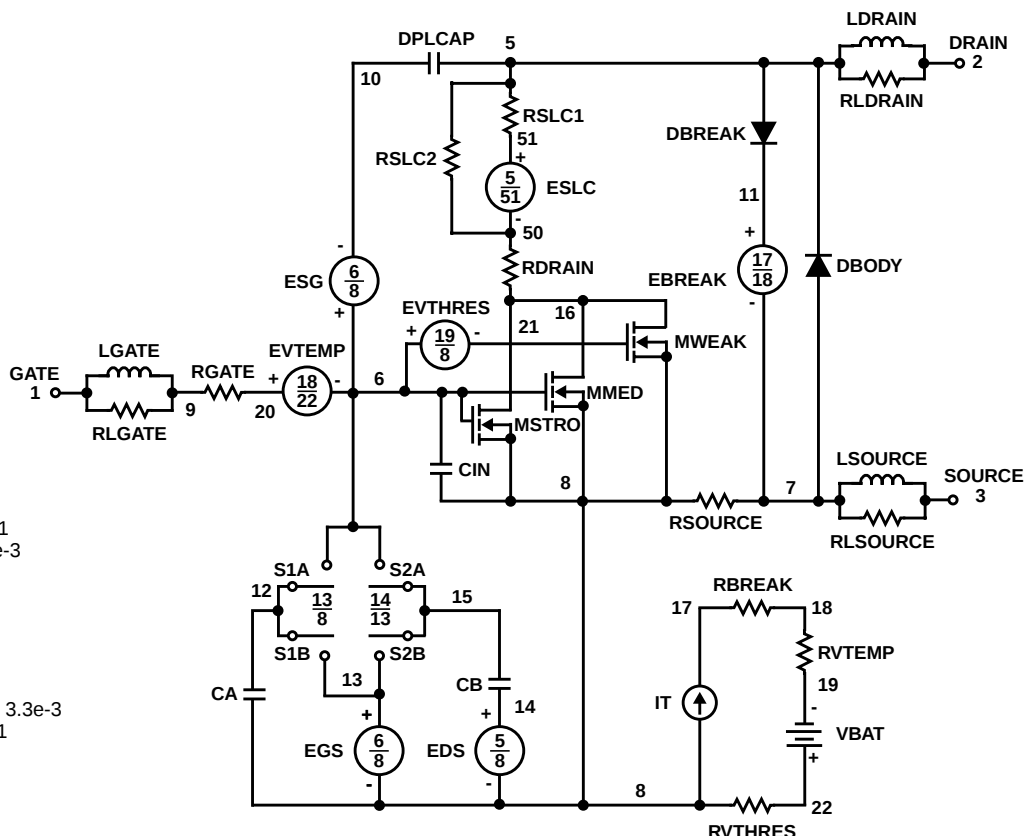
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*230),2.5))}

.MODEL DBODYMOD D (IS = 2.5e-12 RS = 2.85e-3 XTI = 5.5 TRS1 = 2e-3 TRS2 = 1e-6 CJO = 3.2e-9 TT = 5.5e-8 M = 0.6)
.MODEL DBREAKMOD D (RS = 2.9e-1 TRS1 = 1e-3 TRS2 = 1e-6)
.MODEL DPLCAPMOD D (CJO = 3.4e-9 IS = 1e-30 M = 0.8 N = 10)
.MODEL MMEDMOD NMOS (VTO = 3.06 KP = 4.8 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1)
.MODEL MSTROMOD NMOS (VTO = 3.5 KP = 80 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.67 KP = 0.08 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 10)
.MODEL RBREAKMOD RES (TC1 = 1.3e-3 TC2 = -9e-7)
.MODEL RDRAINMOD RES (TC1 = 1.1e-2 TC2 = 2.5e-5)
.MODEL RSLCMOD RES (TC1 = 4.5e-3 TC2 = 1e-5)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.5e-3 TC2 = -1.1e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.75e-3 TC2 = 0)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.0 VOFF = -4.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.5 VOFF = -6.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF = 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -0.5)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV 15 Feb 00

T75542

CTHERM1 th 6 4.1e-3
 CHERM2 6 5 5.5e-3
 CHERM3 5 4 8.6e-3
 CHERM4 4 3 1.5e-2
 CHERM5 3 2 1.6e-2
 CHERM6 2 tl 6.5e-2

RHERM1 th 6 2.0e-4
 RHERM2 6 5 3.5e-3
 RHERM3 5 4 2.5e-2
 RHERM4 4 3 9.0e-2
 RHERM5 3 2 1.6e-1
 RHERM6 2 tl 2.3e-1

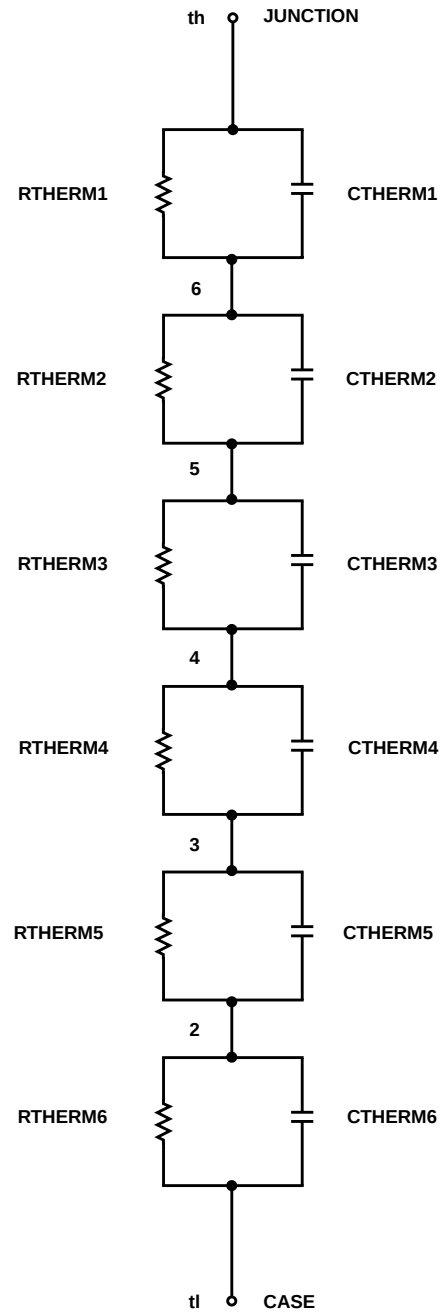
SABER Thermal Model

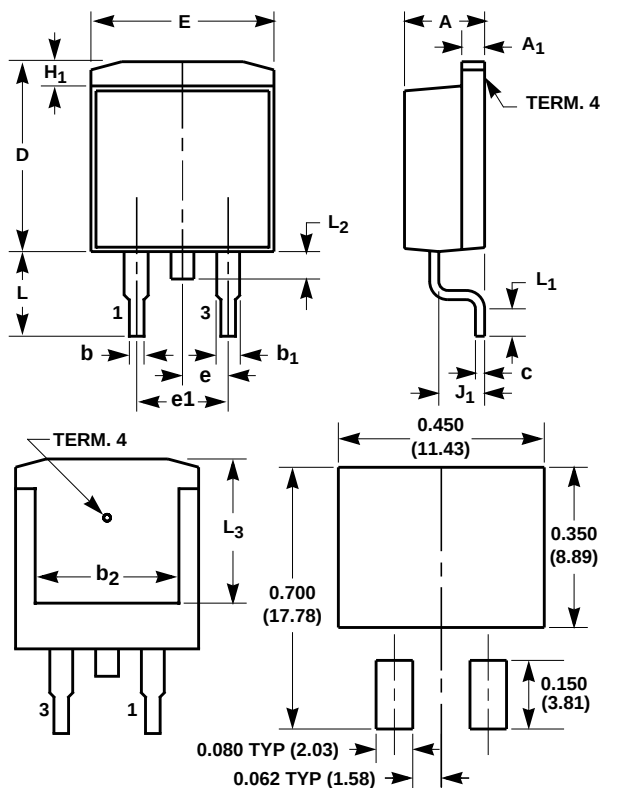
SABER thermal model t75542

template thermal_model th tl
 thermal_c th, tl

```
{
    ctherm.therm1 th 6 = 4.1e-3
    ctherm.therm2 6 5 = 5.5e-3
    ctherm.therm3 5 4 = 8.6e-3
    ctherm.therm4 4 3 = 1.5e-2
    ctherm.therm5 3 2 = 1.6e-2
    ctherm.therm6 2 tl = 6.5e-2
```

```
rtherm.rtherm1 th 6 = 2.0e-4
rtherm.rtherm2 6 5 = 3.5e-3
rtherm.rtherm3 5 4 = 2.5e-2
rtherm.rtherm4 4 3 = 9.0e-2
rtherm.rtherm5 3 2 = 1.6e-1
rtherm.rtherm6 2 tl = 2.3e-1
}
```



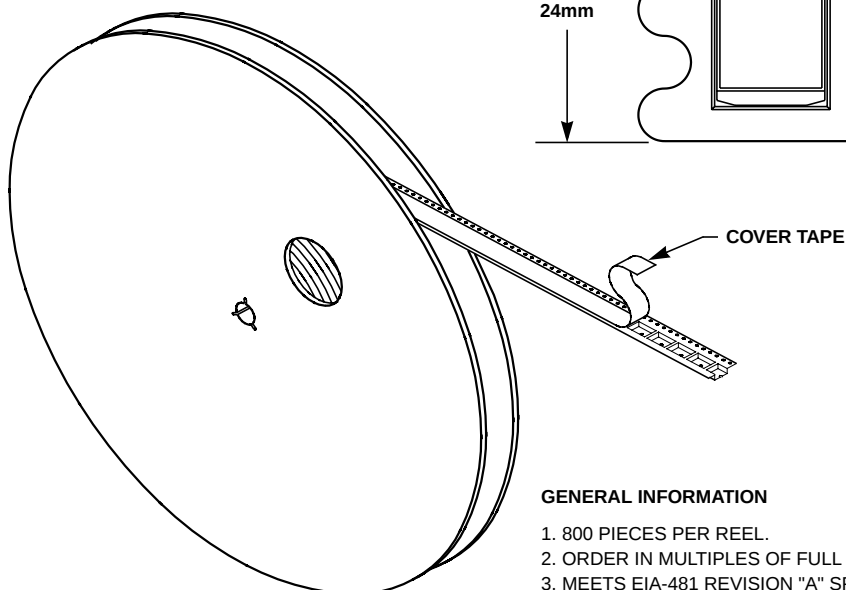
TO-263AB SURFACE MOUNT JEDEC TO-263AB PLASTIC PACKAGE


MINIMUM PAD SIZE RECOMMENDED FOR
SURFACE-MOUNTED APPLICATIONS

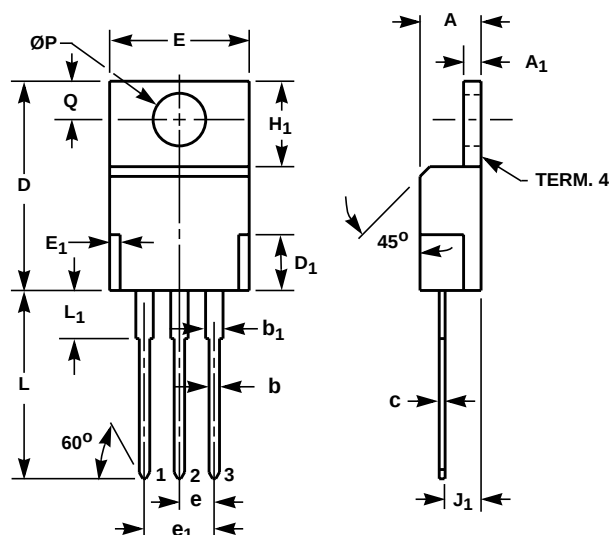
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	4, 5
b	0.030	0.034	0.77	0.86	4, 5
b ₁	0.045	0.055	1.15	1.39	4, 5
b ₂	0.310	-	7.88	-	2
c	0.018	0.022	0.46	0.55	4, 5
D	0.405	0.425	10.29	10.79	-
E	0.395	0.405	10.04	10.28	-
e	0.100 TYP		2.54 TYP		7
e ₁	0.200 BSC		5.08 BSC		7
H ₁	0.045	0.055	1.15	1.39	-
J ₁	0.095	0.105	2.42	2.66	-
L	0.175	0.195	4.45	4.95	-
L ₁	0.090	0.110	2.29	2.79	4, 6
L ₂	0.050	0.070	1.27	1.77	3
L ₃	0.315	-	8.01	-	2

NOTES:

- These dimensions are within allowable dimensions of Rev. C of JEDEC TO-263AB outline dated 2-92.
- L₃ and b₂ dimensions established a minimum mounting surface for terminal 4.
- Solder finish uncontrolled in this area.
- Dimension (without solder).
- Add typically 0.002 inches (0.05mm) for solder plating.
- L₁ is the terminal length for soldering.
- Position of lead to be measured 0.120 inches (3.05mm) from bottom of dimension D.
- Controlling dimension: Inch.
- Revision 10 dated 5-99.

TO-263AB
24mm TAPE AND REEL

GENERAL INFORMATION

- 800 PIECES PER REEL.
- ORDER IN MULTIPLES OF FULL REELS ONLY.
- MEETS EIA-481 REVISION "A" SPECIFICATIONS.

TO-220AB**3 LEAD JEDEC TO-220AB PLASTIC PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
A ₁	0.048	0.052	1.22	1.32	-
b	0.030	0.034	0.77	0.86	3, 4
b ₁	0.045	0.055	1.15	1.39	2, 3
c	0.014	0.019	0.36	0.48	2, 3, 4
D	0.590	0.610	14.99	15.49	-
D ₁	-	0.160	-	4.06	-
E	0.395	0.410	10.04	10.41	-
E ₁	-	0.030	-	0.76	-
e	0.100 TYP		2.54 TYP		5
e ₁	0.200 BSC		5.08 BSC		5
H ₁	0.235	0.255	5.97	6.47	-
J ₁	0.100	0.110	2.54	2.79	6
L	0.530	0.550	13.47	13.97	-
L ₁	0.130	0.150	3.31	3.81	2
$\varnothing P$	0.149	0.153	3.79	3.88	-
Q	0.102	0.112	2.60	2.84	-

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in L₁.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.

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TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA

Intersil Ltd.
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Taipei, Taiwan 104
Republic of China
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