

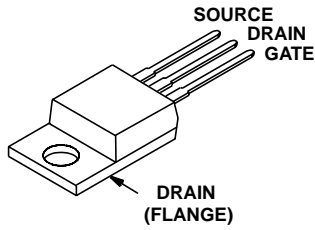
**75A, 80V, 0.010 Ohm, N-Channel, UltraFET
Power MOSFET**



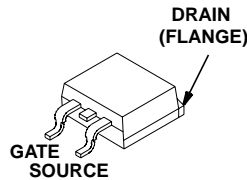
Packaging

JEDEC TO-220AB

JEDEC TO-263AB



HUF75545P3

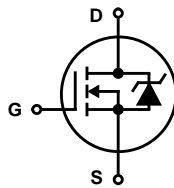


HUF75545S3S

Features

- Ultra Low On-Resistance
 - $r_{DS(ON)} = 0.010\Omega, V_{GS} = 10V$
- Simulation Models
 - Temperature Compensated PSPICE® and SABER® Electrical Models
 - Spice and SABER® Thermal Impedance Models
 - www.semi.Intersil.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Symbol



Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|-------------|----------|--------|
| HUF75545P3 | TO-220AB | 75545P |
| HUF75545S3S | TO-263AB | 75545S |

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the TO-263AB variant in tape and reel, e.g., HUF75545S3ST.

Absolute Maximum Ratings $T_C = 25^\circ C$, Unless Otherwise Specified

| | HUF75545P3, HUF75545S3S | UNITS |
|---|-------------------------|-----------------------|
| Drain to Source Voltage (Note 1) | V_{DSS} | 80 V |
| Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1) | V_{DGR} | 80 V |
| Gate to Source Voltage | V_{GS} | ± 20 V |
| Drain Current | | |
| Continuous ($T_C = 25^\circ C, V_{GS} = 10V$) (Figure 2) | I_D | 75 A |
| Continuous ($T_C = 100^\circ C, V_{GS} = 10V$) (Figure 2) | I_D | 73 A |
| Pulsed Drain Current | I_{DM} | Figure 4 |
| Pulsed Avalanche Rating | UIS | Figures 6, 14, 15 |
| Power Dissipation | P_D | 270 W |
| Derate Above $25^\circ C$ | | 1.8 $W/^\circ C$ |
| Operating and Storage Temperature | T_J, T_{STG} | -55 to 175 $^\circ C$ |
| Maximum Temperature for Soldering | | |
| Leads at 0.063in (1.6mm) from Case for 10s | T_L | 300 $^\circ C$ |
| Package Body for 10s, See Techbrief TB334 | T_{pkg} | 260 $^\circ C$ |

NOTES:

1. $T_J = 25^\circ C$ to $150^\circ C$.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

HUF75545P3, HUF75545S3S

Electrical Specifications $T_C = 25^\circ\text{C}$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS | |
|--|-----------------|---|--|--------|-----------|--------------------|----|
| OFF STATE SPECIFICATIONS | | | | | | | |
| Drain to Source Breakdown Voltage | BV_{DSS} | $I_D = 250\mu\text{A}$, $V_{GS} = 0\text{V}$ (Figure 11) | 80 | - | - | V | |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 75\text{V}$, $V_{GS} = 0\text{V}$ | - | - | 1 | μA | |
| | | $V_{DS} = 70\text{V}$, $V_{GS} = 0\text{V}$, $T_C = 150^\circ\text{C}$ | - | - | 250 | μA | |
| Gate to Source Leakage Current | I_{GSS} | $V_{GS} = \pm 20\text{V}$ | - | - | ± 100 | nA | |
| ON STATE SPECIFICATIONS | | | | | | | |
| Gate to Source Threshold Voltage | $V_{GS(TH)}$ | $V_{GS} = V_{DS}$, $I_D = 250\mu\text{A}$ (Figure 10) | 2 | - | 4 | V | |
| Drain to Source On Resistance | $r_{DS(ON)}$ | $I_D = 75\text{A}$, $V_{GS} = 10\text{V}$ (Figure 9) | - | 0.0082 | 0.010 | Ω | |
| THERMAL SPECIFICATIONS | | | | | | | |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | TO-220 and TO-263 | - | - | 0.55 | $^\circ\text{C/W}$ | |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | | - | - | 62 | $^\circ\text{C/W}$ | |
| SWITCHING SPECIFICATIONS ($V_{GS} = 10\text{V}$) | | | | | | | |
| Turn-On Time | t_{ON} | $V_{DD} = 40\text{V}$, $I_D = 75\text{A}$ $V_{GS} = 10\text{V}$, $R_{GS} = 2.5\Omega$ (Figures 18, 19) | - | - | 210 | ns | |
| Turn-On Delay Time | $t_{d(ON)}$ | | - | 14 | - | ns | |
| Rise Time | t_r | | - | 125 | - | ns | |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | - | 40 | - | ns | |
| Fall Time | t_f | | - | 90 | - | ns | |
| Turn-Off Time | t_{OFF} | | - | - | 195 | ns | |
| GATE CHARGE SPECIFICATIONS | | | | | | | |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS} = 0\text{V}$ to 20V | $V_{DD} = 40\text{V}$, $I_D = 75\text{A}$, $I_{g(REF)} = 1.0\text{mA}$ (Figures 13, 16, 17) | - | 195 | 235 | nC |
| Gate Charge at 10V | $Q_{g(10)}$ | $V_{GS} = 0\text{V}$ to 10V | | - | 105 | 125 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS} = 0\text{V}$ to 2V | | - | 6.8 | 8.2 | nC |
| Gate to Source Gate Charge | Q_{gs} | | | - | 15 | - | nC |
| Reverse Transfer Capacitance | Q_{gd} | | | - | 43 | - | nC |
| CAPACITANCE SPECIFICATIONS | | | | | | | |
| Input Capacitance | C_{ISS} | $V_{DS} = 25\text{V}$, $V_{GS} = 0\text{V}$, $f = 1\text{MHz}$ (Figure 12) | - | 3750 | - | pF | |
| Output Capacitance | C_{OSS} | | - | 1100 | - | pF | |
| Reverse Transfer Capacitance | C_{RSS} | | - | 350 | - | pF | |

Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|-------------------------------|----------|--|-----|-----|------|-------|
| Source to Drain Diode Voltage | V_{SD} | $I_{SD} = 75\text{A}$ | - | - | 1.25 | V |
| | | $I_{SD} = 35\text{A}$ | - | - | 1.00 | V |
| Reverse Recovery Time | t_{rr} | $I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | - | - | 100 | ns |
| Reverse Recovered Charge | Q_{RR} | $I_{SD} = 75\text{A}$, $dI_{SD}/dt = 100\text{A}/\mu\text{s}$ | - | - | 300 | nC |

Typical Performance Curves

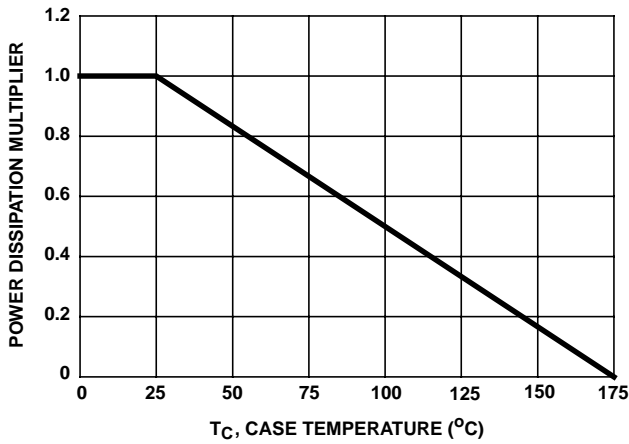


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

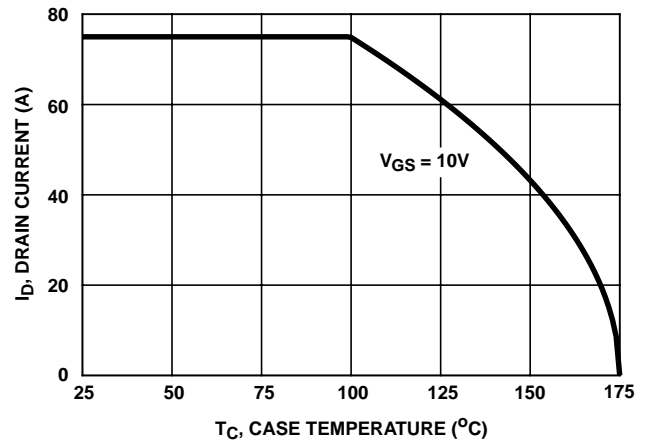


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

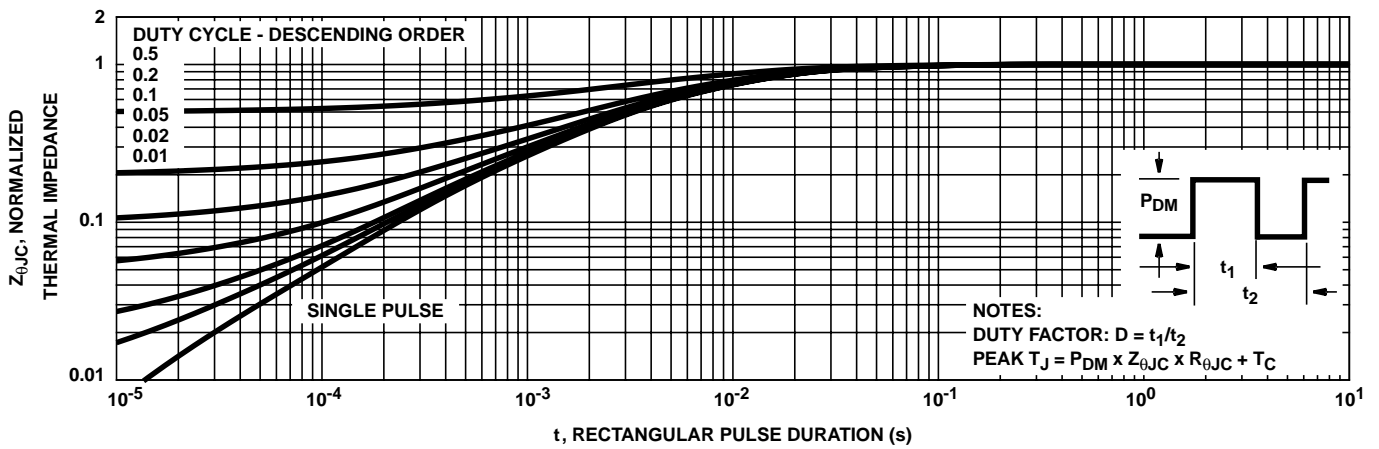


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

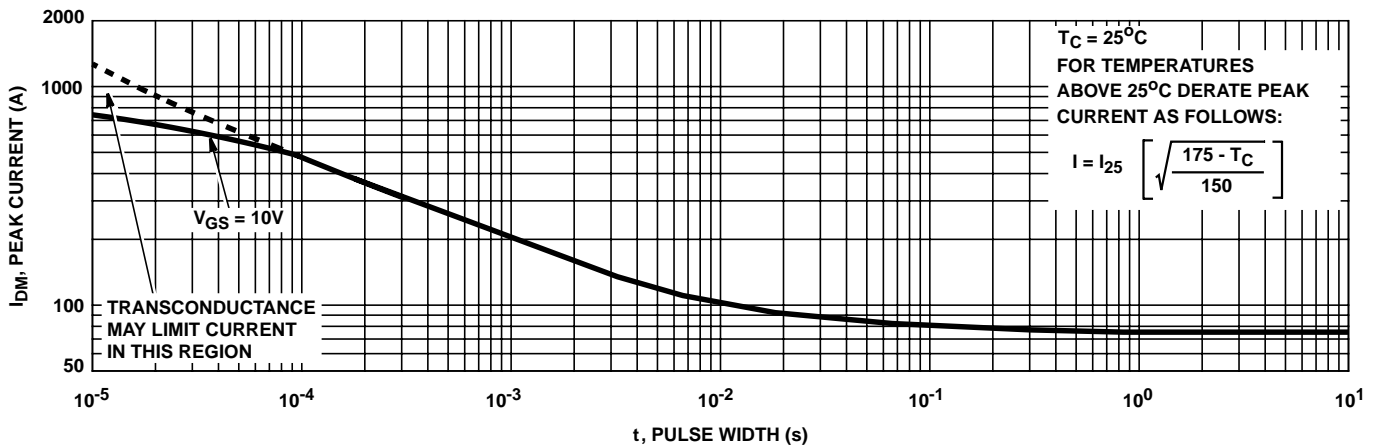


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

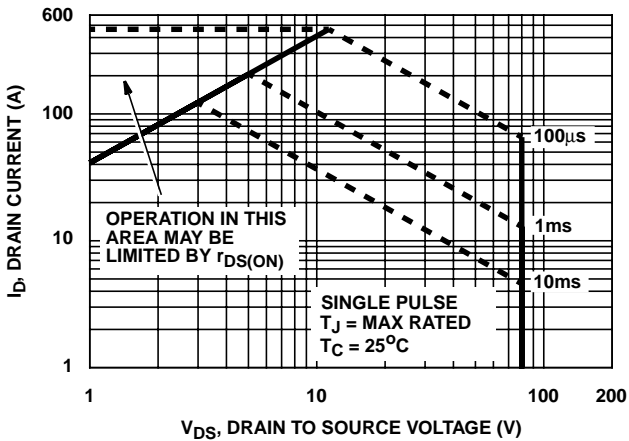
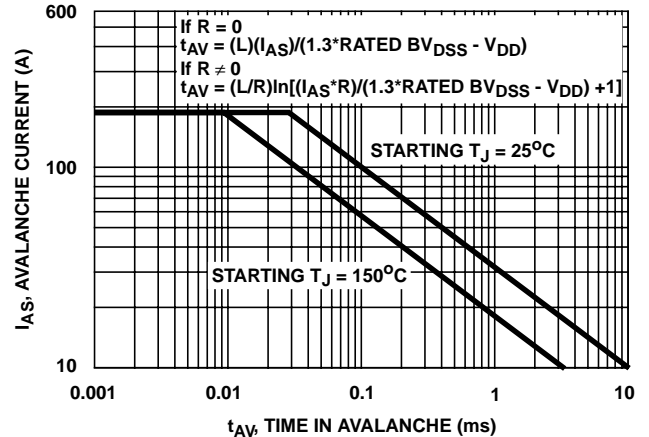


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

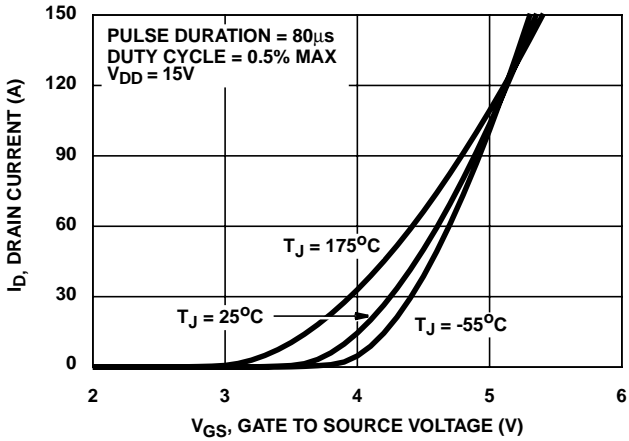


FIGURE 7. TRANSFER CHARACTERISTICS

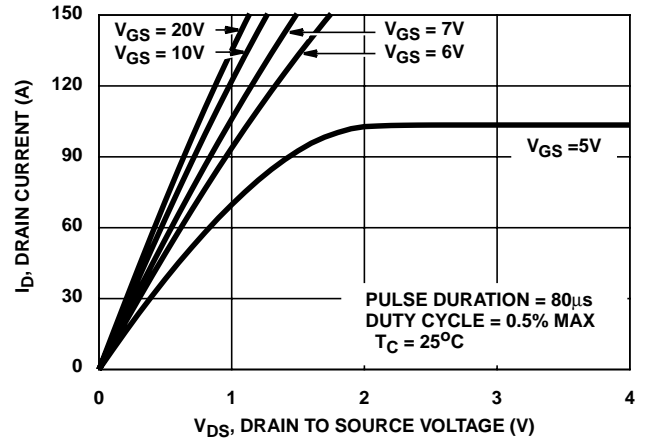


FIGURE 8. SATURATION CHARACTERISTICS

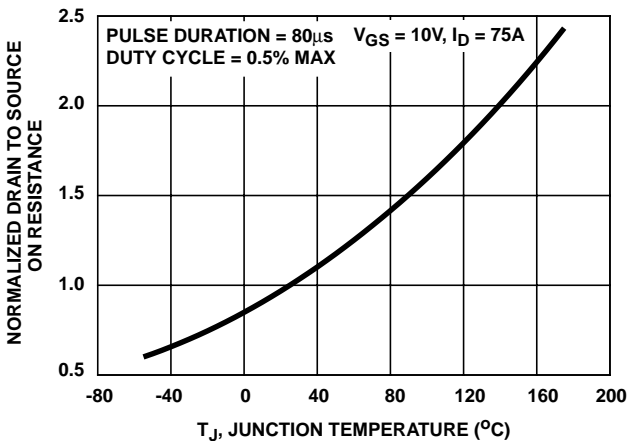


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

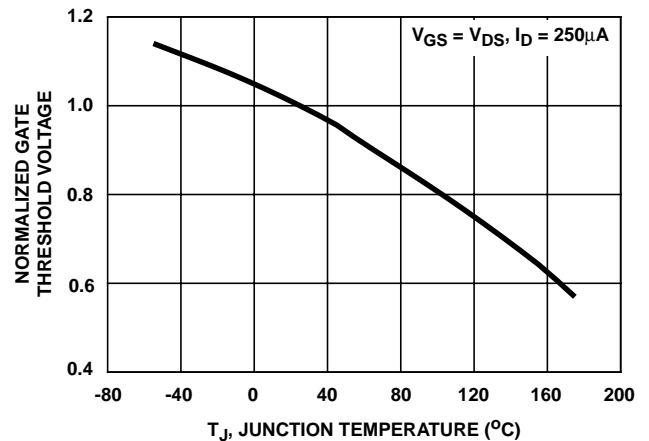


FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

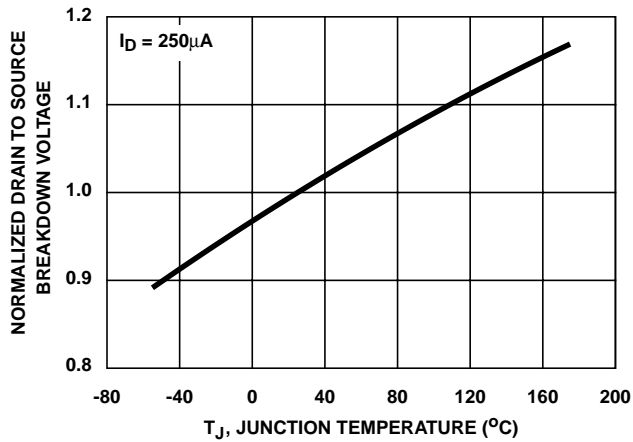


FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

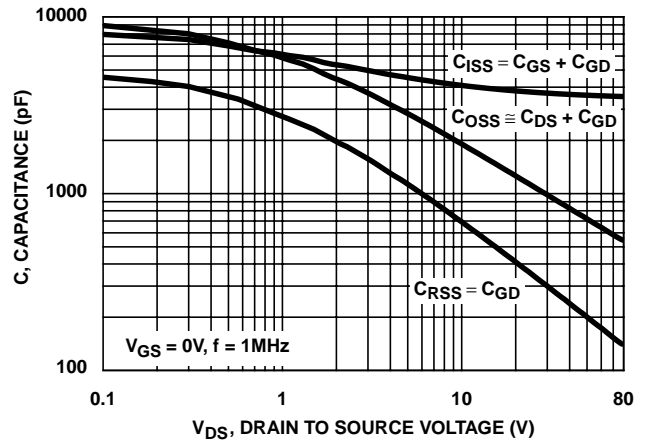
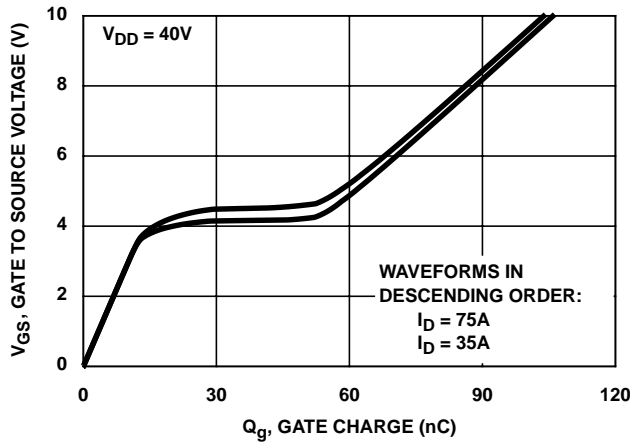


FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

Test Circuits and Waveforms

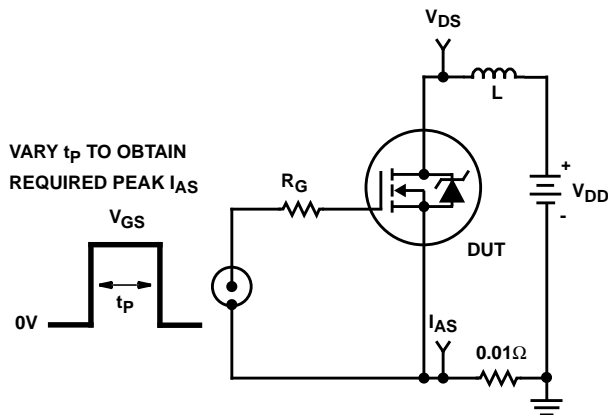


FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

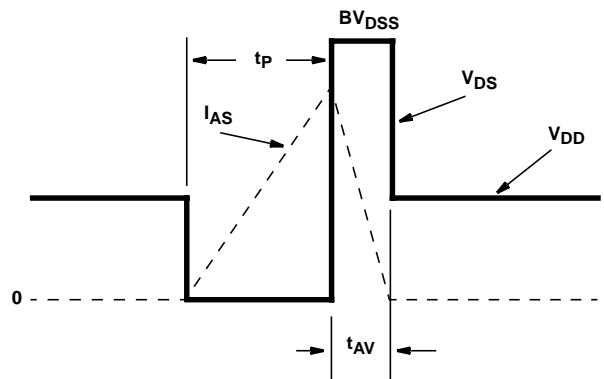


FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

Test Circuits and Waveforms (Continued)

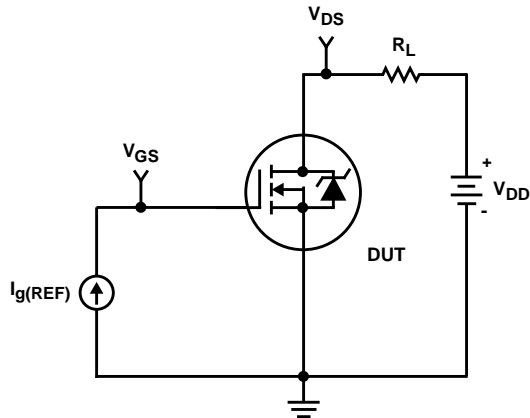


FIGURE 16. GATE CHARGE TEST CIRCUIT

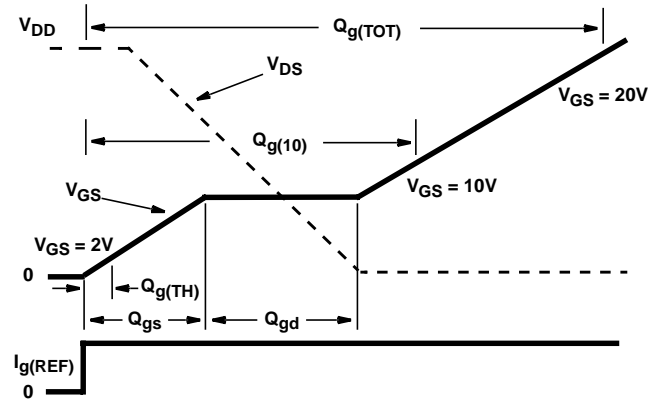


FIGURE 17. GATE CHARGE WAVEFORMS

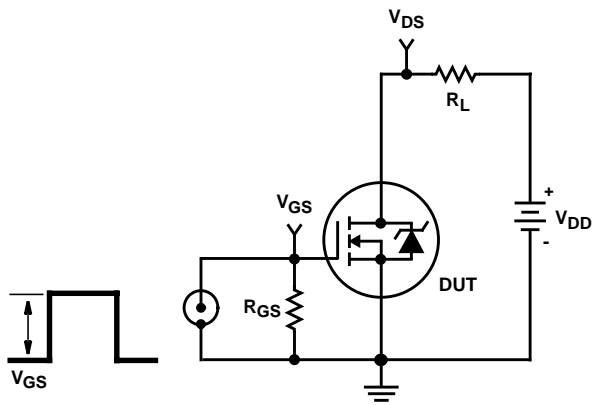


FIGURE 18. SWITCHING TIME TEST CIRCUIT

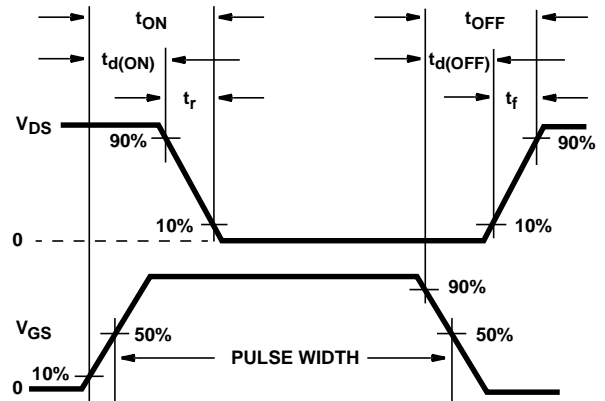


FIGURE 19. SWITCHING TIME WAVEFORM

HUF75545P3, HUF75545S3S

PSICE Electrical Model

.SUBCKT HUF75545 2 1 3 ; rev 21 May 1999

CA 12 8 5.4e-9
 CB 15 14 5.3e-9
 CIN 6 8 3.4e-9

DBODY 7 5 DBODYMOD
 DBREAK 5 11 DBREAKMOD
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 87.4
 EDS 14 8 5 8 1
 EGS 13 8 6 8 1
 ESG 6 10 6 8 1
 EVTHRES 6 21 19 8 1
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9
 LGATE 1 9 5.1e-9
 LSOURCE 3 7 4.4e-9

MMED 16 6 8 8 MMEDMOD
 MSTRO 16 6 8 8 MSTROMOD
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
 RDRAIN 50 16 RDRAINMOD 4.80e-3
 RGATE 9 20 0.87
 RLDRAIN 2 5 10
 RLGATE 1 9 51
 RLSOURCE 3 7 44
 RSLC1 5 51 RSLCMOD 1e-6
 RSLC2 5 50 1e3
 RSOURCE 8 7 RSOURCEMOD 1.6e-3
 RVTHRES 22 8 RVTHRESMOD 1
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
 S1B 13 12 13 8 S1BMOD
 S2A 6 15 14 13 S2AMOD
 S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

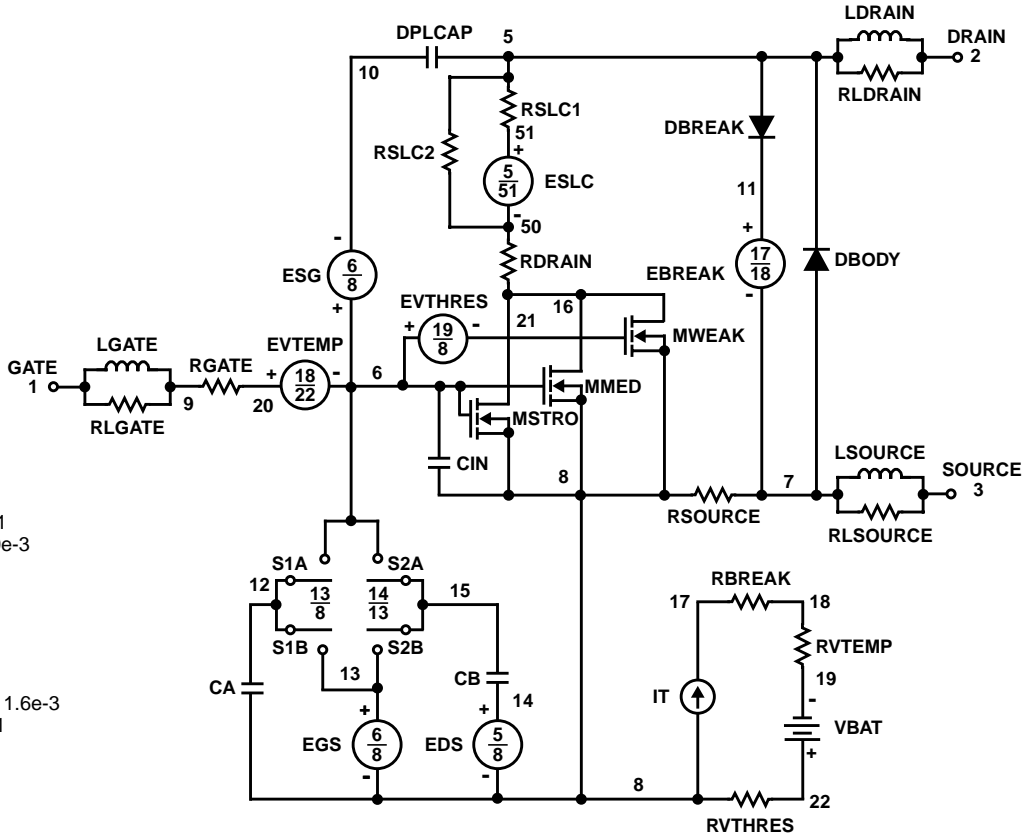
ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51))/(1e-6*320),3))}

.MODEL DBODYMOD D (IS = 3.6e-12 RS = 2.1e-3 TRS1 = 1.5e-3 TRS2 = 5.1e-6 CJO = 4.6e-9 TT = 3.3e-8 M = 0.55)
 .MODEL DBREAKMOD D (RS = 2.3e-1 TRS1 = 0 TRS2 = -1.8e-5)
 .MODEL DPLCAPMOD D (CJO = 4.8e-9 IS = 1e-30 N = 10 VJ = 1 M = 0.8)
 .MODEL MMEDMOD NMOS (VTO = 3.04 KP = 6 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 0.87)
 .MODEL MSTROMOD NMOS (VTO = 3.5 KP = 105 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
 .MODEL MWEAKMOD NMOS (VTO = 2.65 KP = 0.12 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 8.7)
 .MODEL RBREAKMOD RES (TC1 = 1.3e-3 TC2 = -1e-6)
 .MODEL RDRAINMOD RES (TC1 = 9e-3 TC2 = 2.8e-5)
 .MODEL RSLCMOD RES (TC1 = 1.53e-3 TC2 = 2e-5)
 .MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
 .MODEL RVTHRESMOD RES (TC1 = -2.3e-3 TC2 = -1.2e-5)
 .MODEL RVTEMPMOD RES (TC1 = -2.9e-3 TC2 = 5e-7)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -5 VOFF = -3)
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3 VOFF = -5)
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.5 VOFF = 0.5)
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -1.5)

.ENDS

NOTE: For further discussion of the PSICE model, consult **A New PSICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.



SPICE Thermal Model

REV 21 May 1999

HUF75545T

CTHERM1 th 6 6.4e-3
 CTHERM2 6 5 3.0e-2
 CTHERM3 5 4 1.4e-2
 CTHERM4 4 3 1.6e-2
 CTHERM5 3 2 5.5e-2
 CTHERM6 2 tl 1.5

RTHERM1 th 6 3.2e-3
 RTHERM2 6 5 8.1e-3
 RTHERM3 5 4 2.3e-2
 RTHERM4 4 3 1.3e-1
 RTHERM5 3 2 1.8e-1
 RTHERM6 2 tl 3.8e-2

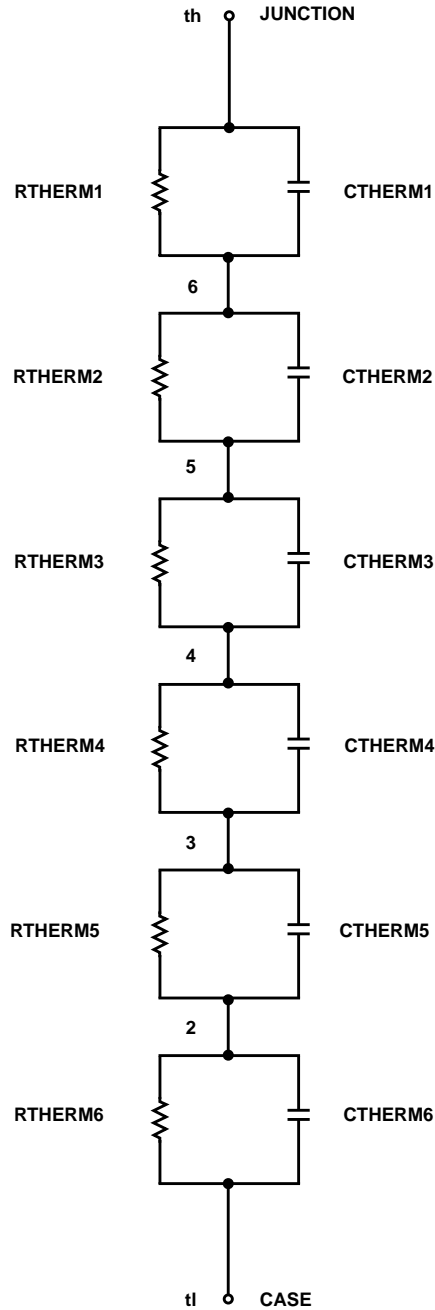
SABER Thermal Model

SABER thermal model HUF75545T

template thermal_model th tl
 thermal_c th, tl

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{
ctherm.ctherm1 th 6 = 6.4e-3
ctherm.ctherm2 6 5 = 3.0e-2
ctherm.ctherm3 5 4 = 1.4e-2
ctherm.ctherm4 4 3 = 1.6e-2
ctherm.ctherm5 3 2 = 5.5e-2
ctherm.ctherm6 2 tl = 1.5
```

```
rtherm.rtherm1 th 6 = 3.2e-3
rtherm.rtherm2 6 5 = 8.1e-3
rtherm.rtherm3 5 4 = 2.3e-2
rtherm.rtherm4 4 3 = 1.3e-1
rtherm.rtherm5 3 2 = 1.8e-1
rtherm.rtherm6 2 tl = 3.8e-2
}
```



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