

**14A, 370V N-Channel, Logic Level, Voltage Clamping IGBTs**

This N-Channel IGBT is a MOS gated, logic level device which is intended to be used as an ignition coil driver in automotive ignition circuits. Unique features include an active voltage clamp between the collector and the gate which provides Self Clamped Inductive Switching (SCIS) capability in ignition circuits. Internal diodes provide ESD protection for the logic level gate. Both a series resistor and a shunt resistor are provided in the gate circuit.

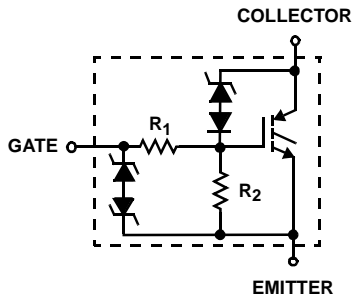
Formerly Developmental Type TA49169.

**Ordering Information**

PART NUMBER	PACKAGE	BRAND
HGT1S14N37G3VLS	TO-263AB	14N37GVL
HGTP14N37G3VL	TO-220AB	14N37GVL

NOTE: When ordering, use the entire part number. Add the suffix 9A to obtain the TO-263AB in tape and reel, i.e. HGT1S14N37G3VLS9A

**Symbol**

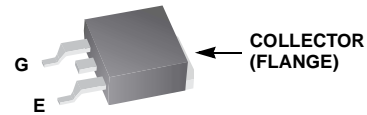


**Features**

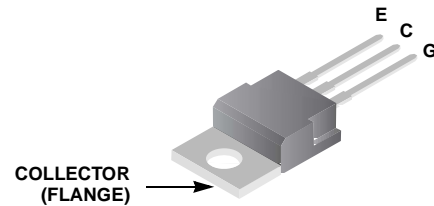
- Logic Level Gate Drive
- Internal Voltage Clamp
- ESD Gate Protection
- $T_J = 175^{\circ}\text{C}$
- Internal Series and Shunt Gate Resistors
- Low Conduction Loss
- Ignition Energy Capable

**Packaging**

JEDEC TO-263AB



JEDEC TO-220AB



**Fairchild CORPORATION IGBT PRODUCT IS COVERED BY ONE OR MORE OF THE FOLLOWING U.S. PATENTS**

4,364,073	4,417,385	4,430,792	4,443,931	4,466,176	4,516,143	4,532,534	4,587,713
4,598,461	4,605,948	4,620,211	4,631,564	4,639,754	4,639,762	4,641,162	4,644,637
4,682,195	4,684,413	4,694,313	4,717,679	4,743,952	4,783,690	4,794,432	4,801,986
4,803,533	4,809,045	4,809,047	4,810,665	4,823,176	4,837,606	4,860,080	4,883,767
4,888,627	4,890,143	4,901,127	4,904,609	4,933,740	4,963,951	4,969,027	

# HGT1S14N37G3VLS, HGTP14N37G3VL

## Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

	HGT1S14N37G3VLS, HGTP14N37G3VL	UNITS
Collector to Emitter Breakdown Voltage at 10mA	$BV_{CER}$ 380	V
Emitter to Collector Breakdown Voltage at 10mA	$BV_{ECS}$ 24	V
Collector Current Continuous at $V_{GE} = 5V$ , $T_C = 25^\circ\text{C}$	$I_{C25}$ 25	A
at $V_{GE} = 5V$ , $T_C = 110^\circ\text{C}$	$I_{C110}$ 18	A
Gate to Emitter Voltage (Note 1)	$V_{GEM}$ $\pm 10$	V
Inductive Switching Current at $L = 3\text{mH}$ , $T_C = 25^\circ\text{C}$	$I_{SCIS}$ 15	A
at $L = 3\text{mH}$ , $T_C = 150^\circ\text{C}$	$I_{SCIS}$ 11.5	A
Collector to Emitter Avalanche Energy at $L = 3\text{mH}$ , $T_C = 25^\circ\text{C}$	$E_{AS}$ 340	mJ
Power Dissipation Total at $T_C = 25^\circ\text{C}$	$P_D$ 136	W
Power Dissipation Derating $T_C > 25^\circ\text{C}$	0.91	W/ $^\circ\text{C}$
Storage Junction Temperature Range	$T_{STG}$ -55 to 175	$^\circ\text{C}$
Operating Junction Temperature Range	$T_J$ -55 to 175	$^\circ\text{C}$
Electrostatic Voltage HBM at 250pF, 1500 $\Omega$ All Pin Configurations	ESD 5	kV
Electrostatic Voltage MM at 200pF, 0 $\Omega$ All Pin Configurations	ESD 2	kV
Maximum Lead Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	$T_L$ 300	$^\circ\text{C}$
Package Body for 10s, See Techbrief 334	$T_{PKG}$ 260	$^\circ\text{C}$

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

1. May be exceeded if  $I_{GEM}$  is limited to 10mA.

## Electrical Specifications $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Collector to Emitter Breakdown Voltage	$BV_{CER}$	$I_C = 10\text{mA}$ , $R_G = 1\text{k}\Omega$ , $V_{GE} = 0V$ , $T_J = -55^\circ\text{C}$ to $175^\circ\text{C}$ (Figure 16)	320	350	380	V	
Gate to Emitter Plateau Voltage	$V_{GEP}$	$I_C = 6.5A$ , $V_{CE} = 12V$	-	2.76	-	V	
Gate Charge	$Q_{G(ON)}$	$I_C = 6.5A$ , $V_{CE} = 12V$ , $V_{GE} = 5V$ (Figure 16)	-	27	-	nC	
Collector to Emitter Clamp Breakdown Voltage	$BV_{CE(CL)}$	$I_C = 15A$ , $R_G = 1\text{k}\Omega$	320	350	380	V	
Emitter to Collector Breakdown Voltage	$BV_{ECS}$	$I_C = 10\text{mA}$	24	28	-	V	
Collector to Emitter Leakage Current	$I_{CES}$	$V_{CE} = 300V$ , $V_{GE} = 0V$ (Figure 13)	$T_J = 25^\circ\text{C}$	-	-	40	$\mu\text{A}$
			$T_J = 175^\circ\text{C}$	-	-	250	$\mu\text{A}$
		$V_{CE} = 250V$ , $V_{GE} = 0V$ (Figure 13)	$T_J = 25^\circ\text{C}$	-	-	10	$\mu\text{A}$
			$T_J = 175^\circ\text{C}$	-	-	75	$\mu\text{A}$
Emitter to Collector Leakage Current	$I_{ECS}$	$V_{EC} = -24V$ , $V_{GE} = 0V$ (Figure 13)	$T_J = 25^\circ\text{C}$	-	-	10	mA
			$T_J = 175^\circ\text{C}$	-	-	50	mA
Collector to Emitter On-State Voltage	$V_{CE(ON)}$	$I_C = 6A$ , $V_{GE} = 4.0V$ (Figures 3 through 9)	$T_J = -55^\circ\text{C}$	-	1.3	1.45	V
			$T_J = 25^\circ\text{C}$	-	1.25	1.6	V
		$I_C = 10A$ , $V_{GE} = 4.5V$ (Figures 3 through 9)	$T_J = 25^\circ\text{C}$	-	1.45	1.75	V
			$T_J = 175^\circ\text{C}$	-	1.5	1.9	V
		$I_C = 14A$ , $V_{GE} = 5V$ (Figures 3 through 9)	$T_J = 25^\circ\text{C}$	-	1.6	2	V
			$T_J = 175^\circ\text{C}$	-	1.7	2.3	V
Gate to Emitter Threshold Voltage	$V_{GE(TH)}$	$I_C = 1\text{mA}$ , $V_{CE} = V_{GE}$ (Figure 12)	1.3	1.8	2.2	V	
Gate Series Resistance	$R_1$		-	70	150	$\Omega$	
Gate to Emitter Resistance	$R_2$		10	18	26	k $\Omega$	
Gate to Emitter Leakage Current	$I_{GES}$	$V_{GE} = \pm 10V$	$\pm 310$	$\pm 500$	$\pm 1000$	$\mu\text{A}$	

# HGT1S14N37G3VLS, HGTP14N37G3VL

## Electrical Specifications $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
Gate to Emitter Breakdown Voltage	$BV_{GES}$	$I_{GES} = \pm 2\text{mA}$	$\pm 12$	$\pm 14$	-	V	
Current Turn-On Delay Time - Resistive Load	$t_{d(ON)}$	$I_C = 6.5\text{A}$ , $R_G = 1\text{k}\Omega$ , $V_{GE} = 5\text{V}$ , $R_L = 2.1\Omega$ , $V_{DD} = 14\text{V}$ , $T_J = 150^\circ\text{C}$ (Figure 14)	-	1	4	$\mu\text{s}$	
Current Turn-On Rise Time - Resistive Load	$t_{rl}$	$I_C = 6.5\text{A}$ , $R_G = 1\text{k}\Omega$ , $V_{GE} = 5\text{V}$ , $R_L = 2.1\Omega$ , $V_{DD} = 14\text{V}$ , $T_J = 150^\circ\text{C}$ (Figure 14)	-	3	7	$\mu\text{s}$	
Current Turn-Off Time - Inductive Load	$t_{d(OFF)} + t_{fl}$	$I_C = 6.5\text{A}$ , $R_G = 1\text{k}\Omega$ , $V_{GE} = 5\text{V}$ , $L = 300\mu\text{H}$ , $V_{DD} = 300\text{V}$ , $T_J = 150^\circ\text{C}$ (Figure 14)	-	10	30	$\mu\text{s}$	
Inductive Use Test	$I_{SCIS}$	$L = 3\text{mH}$ , $V_G = 5\text{V}$ , $R_G = 1\text{k}\Omega$ (Figures 1 and 2)	$T_C = 150^\circ\text{C}$	11.5	-	-	A
			$T_C = 25^\circ\text{C}$	15	-	-	A
Thermal Resistance	$R_{\theta JC}$	(Figure 18)	-	-	1.1	$^\circ\text{C/W}$	

## Typical Performance Curves Unless Otherwise Specified

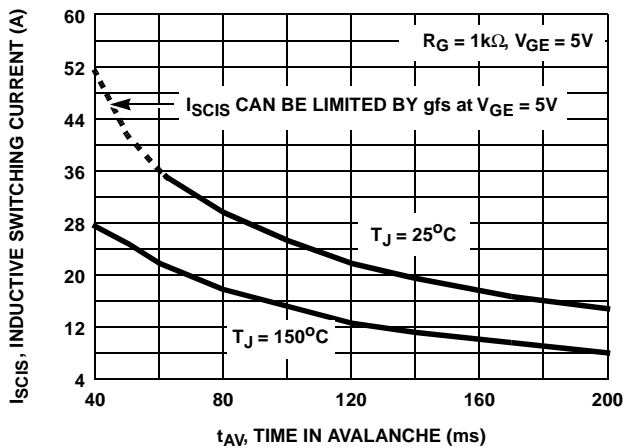


FIGURE 1. SELF CLAMPED INDUCTIVE SWITCHING CURRENT vs TIME IN AVALANCHE

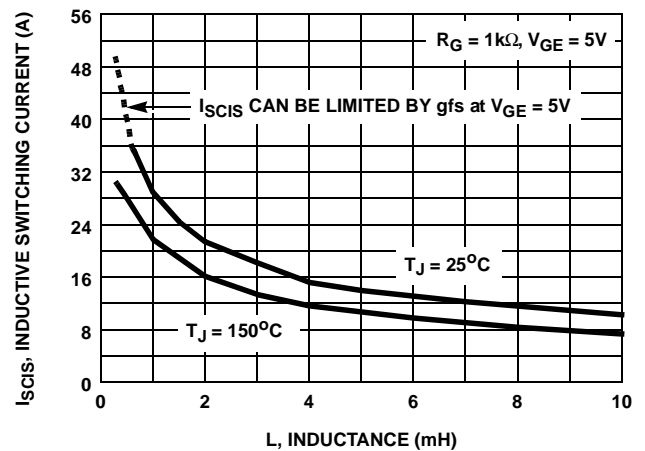


FIGURE 2. SELF CLAMPED INDUCTIVE SWITCHING CURRENT vs INDUCTANCE

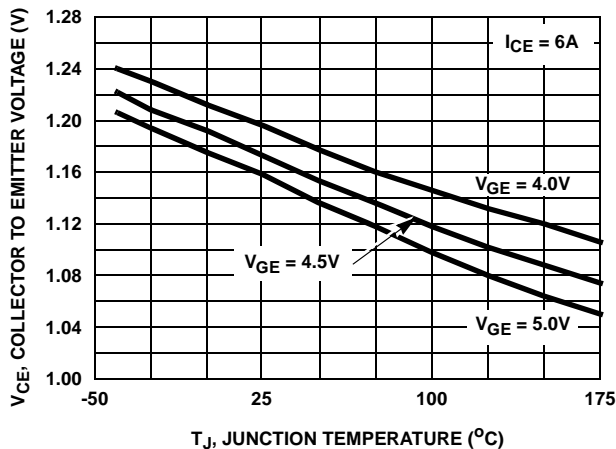


FIGURE 3. COLLECTOR TO EMITTER ON-STATE VOLTAGE vs JUNCTION TEMPERATURE

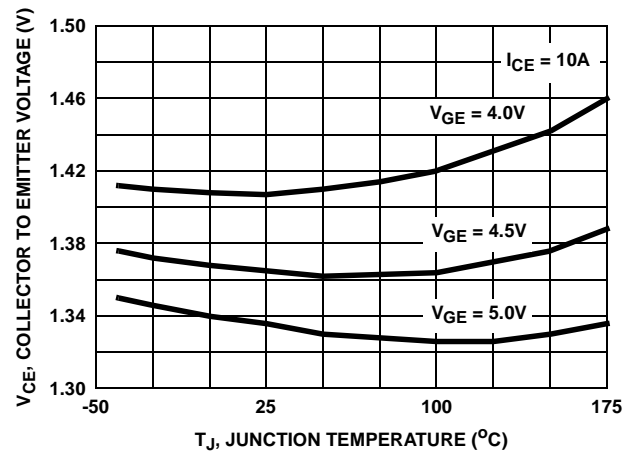


FIGURE 4. COLLECTOR TO EMITTER ON-STATE VOLTAGE vs JUNCTION TEMPERATURE

Typical Performance Curves Unless Otherwise Specified (Continued)

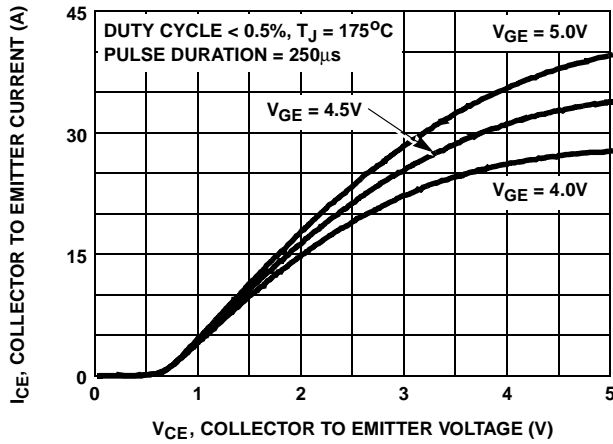


FIGURE 5. COLLECTOR TO EMITTER ON-STATE VOLTAGE

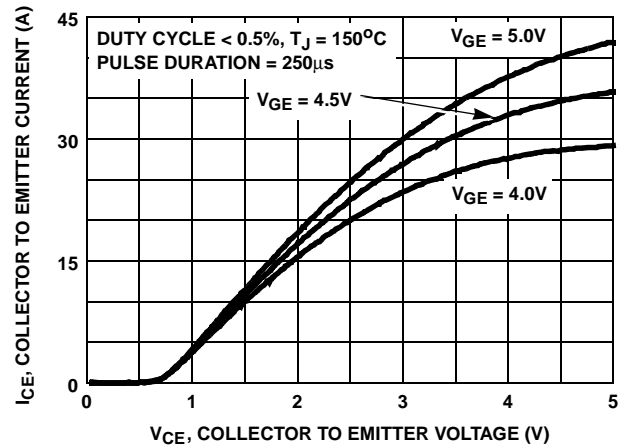


FIGURE 6. COLLECTOR TO EMITTER ON-STATE VOLTAGE

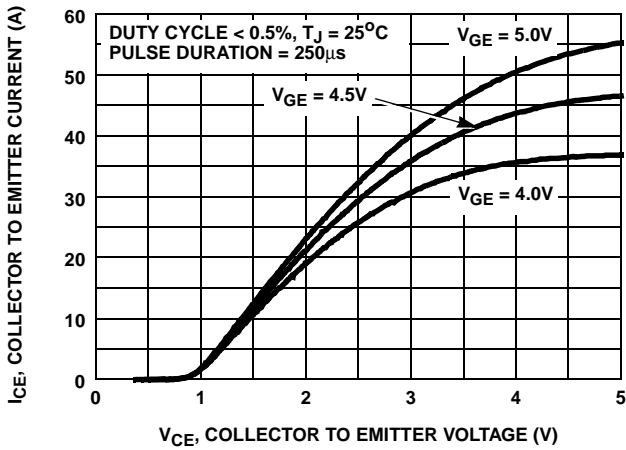


FIGURE 7. COLLECTOR TO EMITTER ON-STATE VOLTAGE

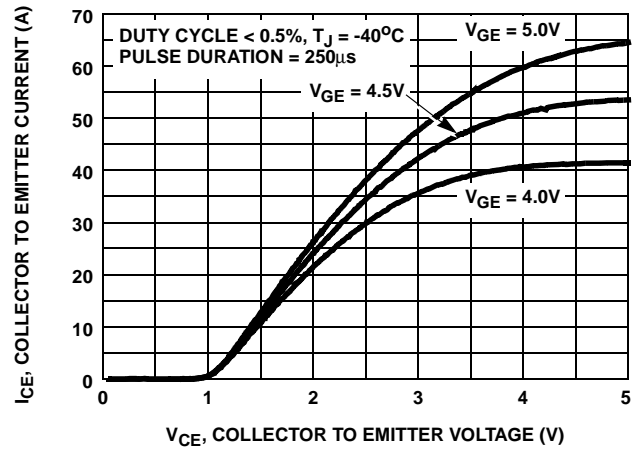


FIGURE 8. COLLECTOR TO EMITTER ON-STATE VOLTAGE

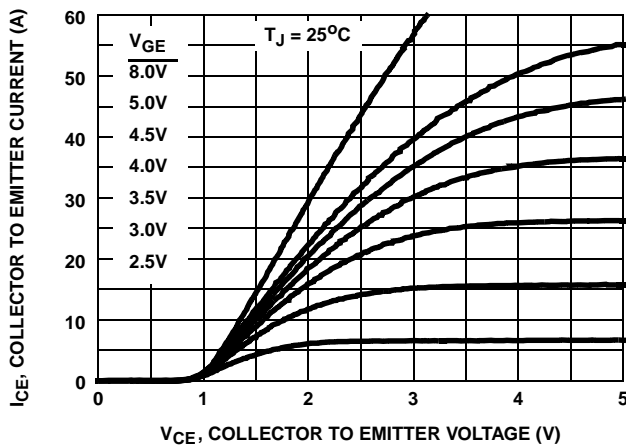


FIGURE 9. COLLECTOR TO EMITTER ON-STATE VOLTAGE

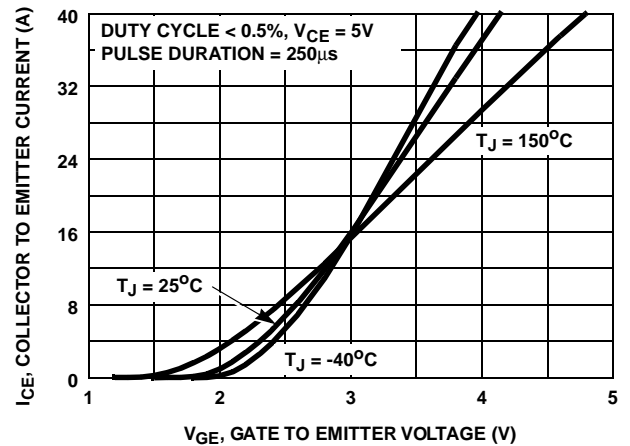


FIGURE 10. TRANSFER CHARACTERISTIC

Typical Performance Curves Unless Otherwise Specified (Continued)

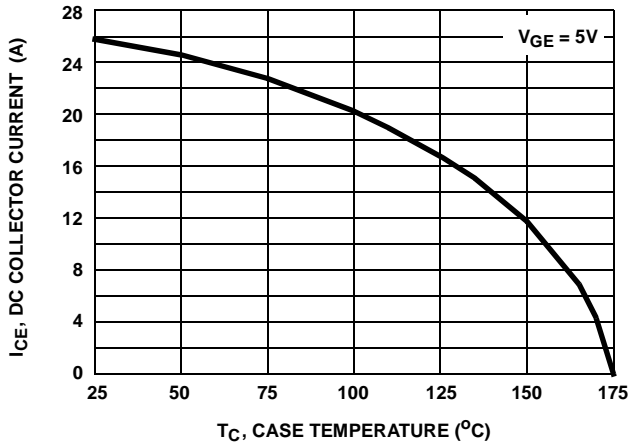


FIGURE 11. DC COLLECTOR CURRENT vs CASE TEMPERATURE

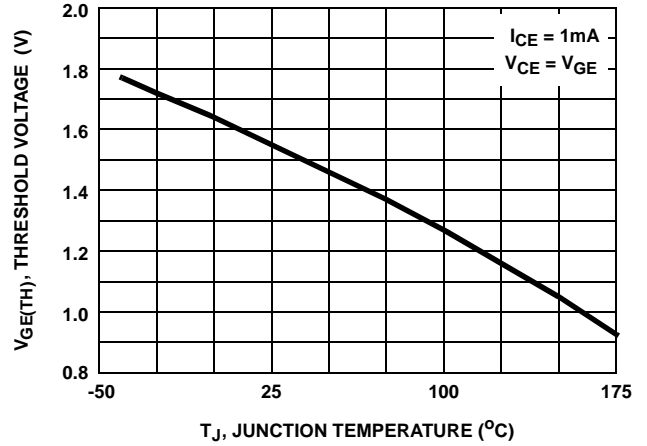


FIGURE 12. THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

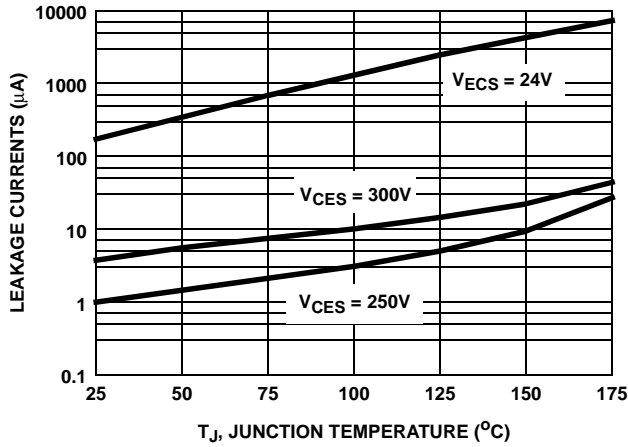


FIGURE 13. LEAKAGE CURRENT vs JUNCTION TEMPERATURE

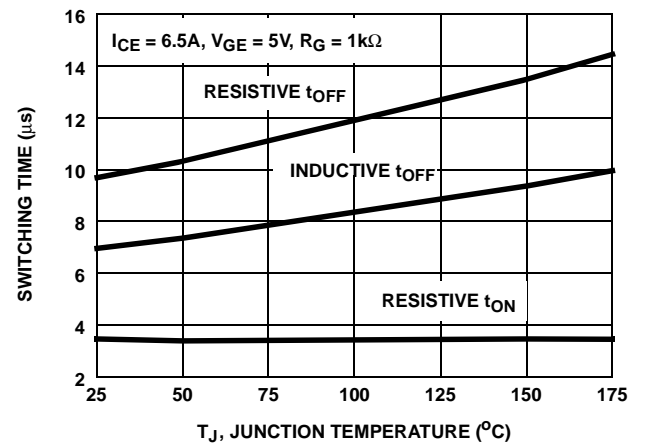


FIGURE 14. SWITCHING TIME vs JUNCTION TEMPERATURE

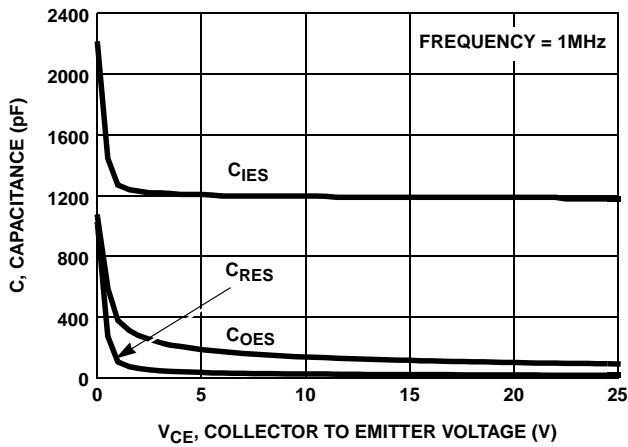


FIGURE 15. CAPACITANCE vs COLLECTOR TO EMITTER VOLTAGE

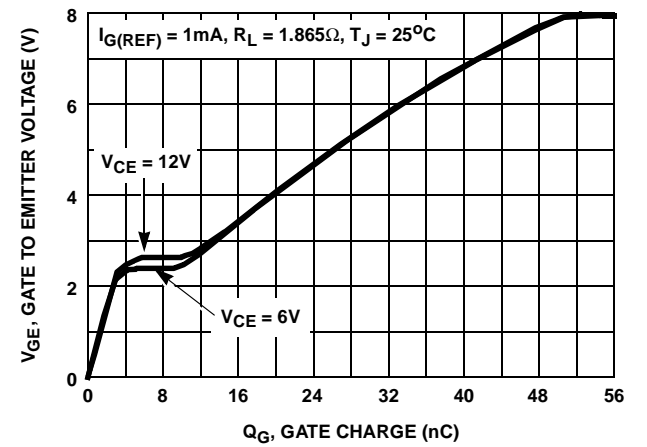


FIGURE 16. GATE CHARGE WAVEFORMS

Typical Performance Curves Unless Otherwise Specified (Continued)

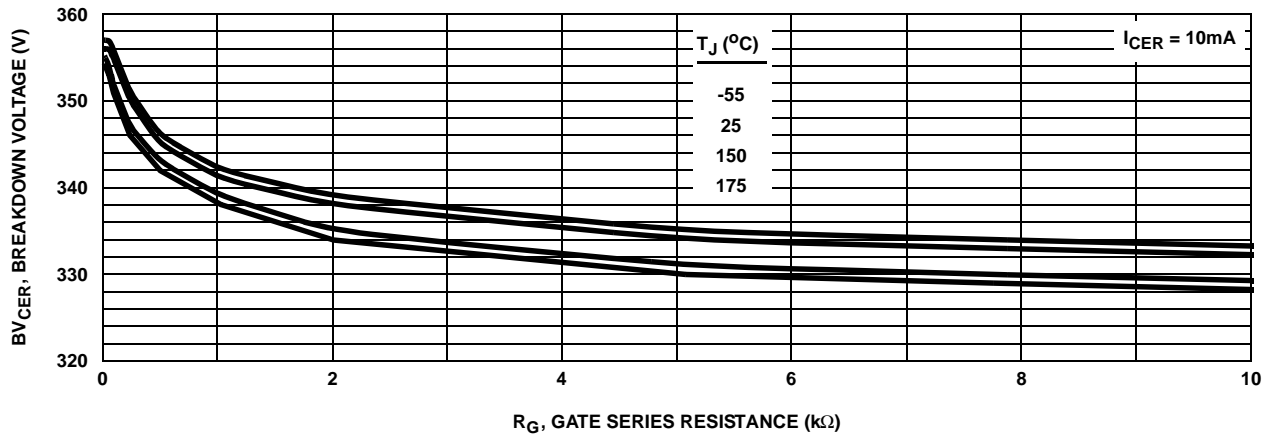


FIGURE 17. BREAKDOWN VOLTAGE vs SERIES GATE RESISTANCE

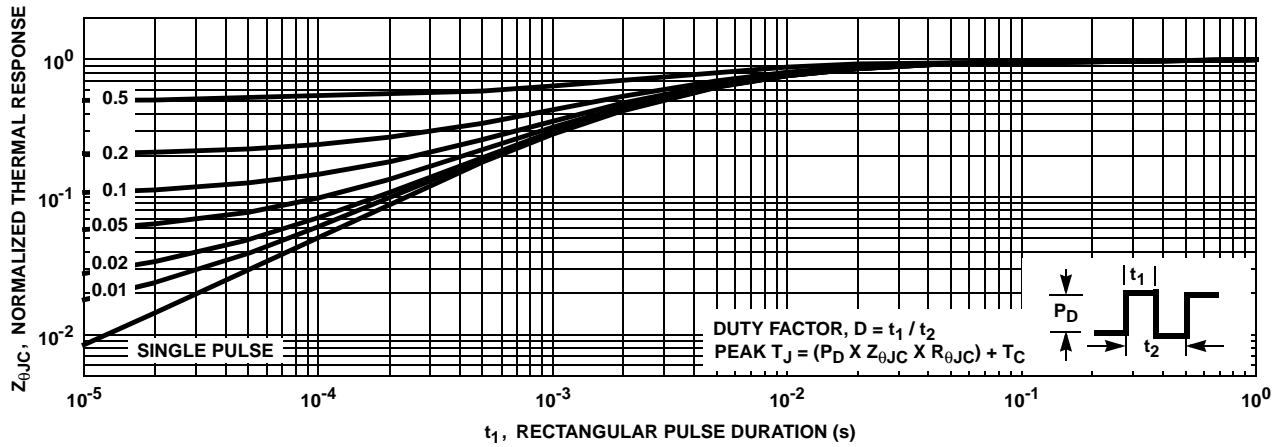


FIGURE 18. IGBT NORMALIZED TRANSIENT THERMAL RESPONSE, JUNCTION TO CASE

Test Circuits

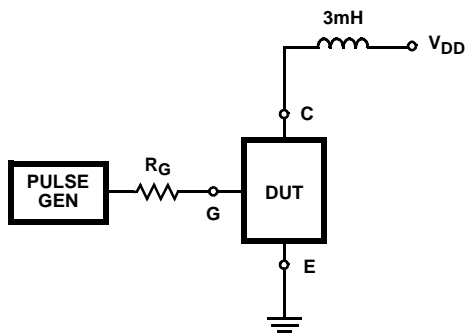


FIGURE 19. INDUCTIVE SWITCHING TEST CIRCUIT

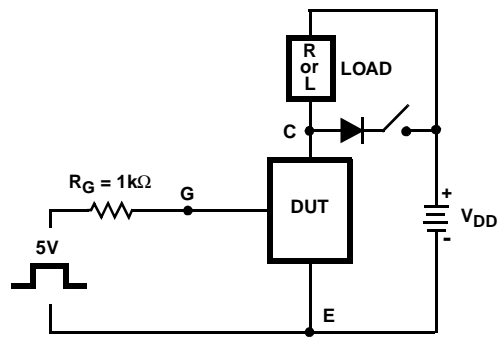


FIGURE 20.  $t_{ON}$  AND  $t_{OFF}$  SWITCHING TEST CIRCUIT



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