HAF2008

Silicon N Channel MOS FET Series
Power Switching

HITACHI

Target specification
ADE-208-707 (Z)
1st. Edition
Dec. 1998

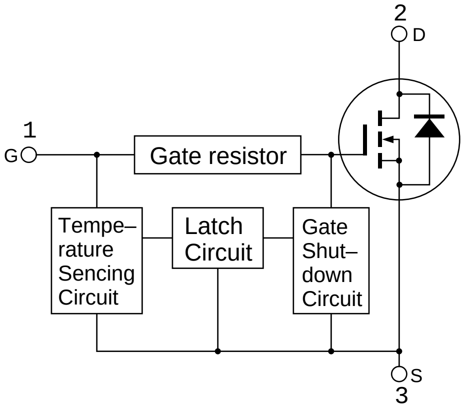
This FET has the over temperature shut–down capability sensing to the junction temperature. This FET has the built–in over temperature shut–down circuit in the gate area. And this circuit operation to shut–down the gate voltage in case of high junction temperature like applying over power consumption, over current etc.

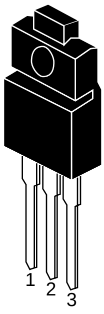
Features

- Logic level operation (4 to 6 V Gate drive)
- High endurance capability against to the short circuit
- Built–in the over temperature shut–down circuit
- Latch type shut–down operation (Need 0 voltage recovery)

Outline

TO–220FM





1. Gate
2. Drain
3. Source

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	(16)	V
Gate to source voltage	V_{GSS}	(–2.5)	V
Drain current	I_D	20	A
Drain peak current	$I_{D(pulse)}$ Note1	40	A
Body-drain diode reverse drain current	I_{DR}	20	A
Channel dissipation	Pch Note2	30	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	–55 to +150	°C

Note: 1. PW ≤ 10µs, duty cycle ≤ 1 %
2. Value at Ta = 25°C

Typical Operation Characteristics

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Input voltage	V_{IH}	3.5	—	—	V	
	V_{IL}	—	—	1.2	V	
Input current (Gate non shut down)	I_{IH1}	—	—	100	µA	Vi = 8V, V_{DS} = 0
	I_{IH2}	—	—	50	µA	Vi = 3.5V, V_{DS} = 0
	I_{IL}	—	—	1	µA	Vi = 1.2V, V_{DS} = 0
Input current (Gate shut down)	$I_{IH(sd)1}$	—	0.8	—	mA	Vi = 8V, V_{DS} = 0
	$I_{IH(sd)2}$	—	0.35	—	mA	Vi = 3.5V, V_{DS} = 0
Shut down temperature	T_{sd}	—	175	—	°C	Channel temperature
Gate operation voltage	V_{op}	3.5	—	12	V	

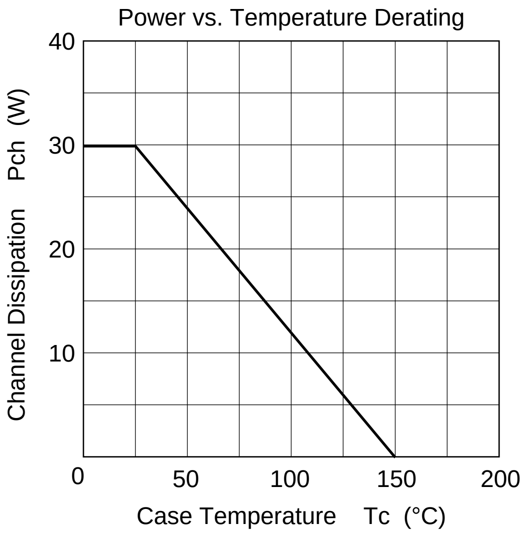
Electrical Characteristics (Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain current	I_{D1}	(25)	—	—	A	V_{GS} = 3.5V, V_{DS} = 2V
Drain current	I_{D2}	—	—	10	mA	V_{GS} = 1.2V, V_{DS} = 2V
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	I_D = 10mA, V_{GS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	(16)	—	—	V	I_G = (300μA), V_{DS} = 0
Gate to source breakdown voltage	$V_{(BR)GSS}$	(–2.5)	—	—	V	I_G = (–100μA), V_{DS} = 0
Gate to source leak current	I_{GSS1}	—	—	100	μA	V_{GS} = 8V, V_{DS} = 0
	I_{GSS2}	—	—	50	μA	V_{GS} = 3.5V, V_{DS} = 0
	I_{GSS3}	—	—	1	μA	V_{GS} = 1.2V, V_{DS} = 0
	I_{GSS4}	—	—	–100	μA	V_{GS} = –2.4V, V_{DS} = 0
Input current (shut down)	$I_{GS(op)1}$	—	0.8	—	mA	V_{GS} = 8V, V_{DS} = 0
	$I_{GS(op)2}$	—	0.35	—	mA	V_{GS} = 3.5V, V_{DS} = 0
Zero gate voltege drain current	I_{DSS}	—	—	10	μA	V_{DS} = 60 V, V_{GS} = 0
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.25	V	I_D = 1mA, V_{DS} = 10V
Static drain to source on state resistance	$R_{DS(on)}$	—	45	60	mΩ	I_D = 10A, V_{GS} = 4V Note3
Static drain to source on state resistance	$R_{DS(on)}$	—	28	40	mΩ	I_D = 10A, V_{GS} = 10V Note3
Forward transfer admittance	$\|y_{fs}\|$	(11)	(17)	—	S	I_D = 10A, V_{DS} = 10V Note3
Output capacitance	Coss	—	(380)	—	pF	V_{DS} = 10V , V_{GS} = 0 f = 1 MHz
Turn-on delay time	$t_{d(on)}$	—	( )	—	μs	I_D = 10A, V_{GS} = 5V
Rise time	t_r	—	( )	—	μs	R_L = 3Ω
Turn-off delay time	$t_{d(off)}$	—	( )	—	μs	
Fall time	t_f	—	( )	—	μs	
Body–drain diode forward voltage	V_{DF}	—	(1.0)	—	V	I_F = 20A, V_{GS} = 0
Body–drain diode reverse recovery time	t_{rr}	—	( )	—	ns	I_F = 20A, V_{GS} = 0 diF/ dt =50A/μs
Over load shut down operation time Note4	t_{os1}	—	( )	—	ms	V_{GS} = 5V, V_{DD} = 12V
	t_{os2}	—	( )	—	ms	V_{GS} = 5V, V_{DD} = 24V

Note: 3. Pulse test

4. Include the time shift based on increasing of channel temperature when operate under over load condition.

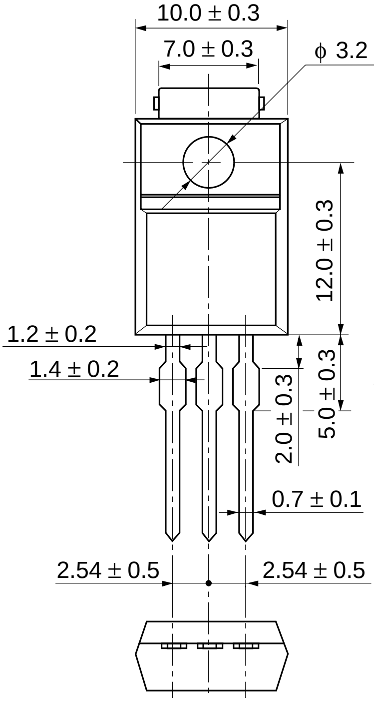
Main Characteristics

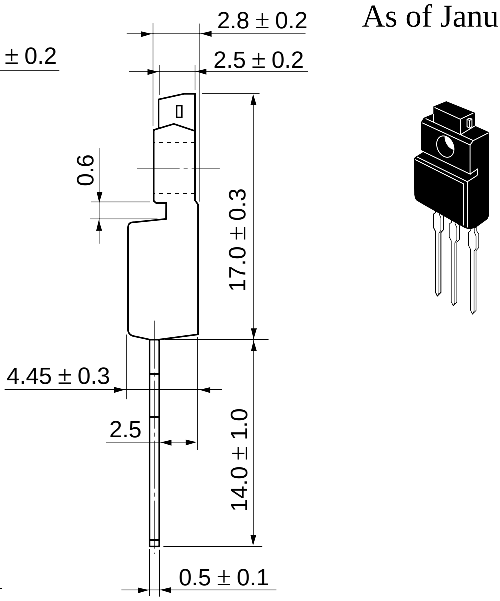


Package Dimensions

As of January, 2001

Unit: mm





Hitachi Code	TO-220FM
JEDEC	—
EIAJ	Conforms
Mass (reference value)	1.8 g

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