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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

Cautions

Keep safety first in your circuit designs!

1. Renesas Technology Corporation puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage.

Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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HAT2024R

Silicon N Channel Power MOS FET High Speed Power Switching

RENESAS

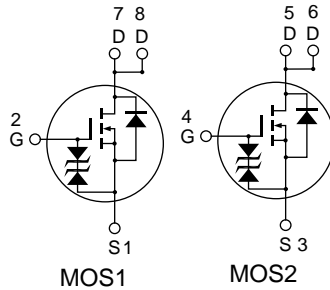
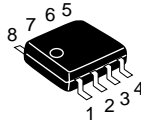
ADE-208-494C (Z)
4th. Edition
Aug. 1997

Features

- Low on-resistance
- Capable of 4 V gate drive
- Low drive current
- High density mounting

Outline

SOP-8



1, 3 S
2, 4 G
5, 6, 7, 8 Dra

Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V _{DSS}	30	V
Gate to source voltage	V _{GSS}	±20	V
Drain current	I _D	5.5	A
Drain peak current	I _{D(pulse)} ^{*1}	44	A
Body to drain diode reverse drain current	I _{DR}	5.5	A
Channel dissipation	Pch ^{*2}	2	W
Channel dissipation	Pch ^{*3}	3	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	-55 to +150	°C

Notes: 1. PW ≤ 10μs, duty cycle ≤ 1 %

2. 1 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

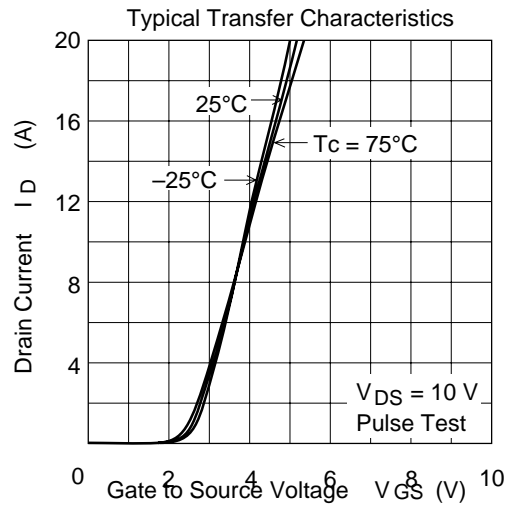
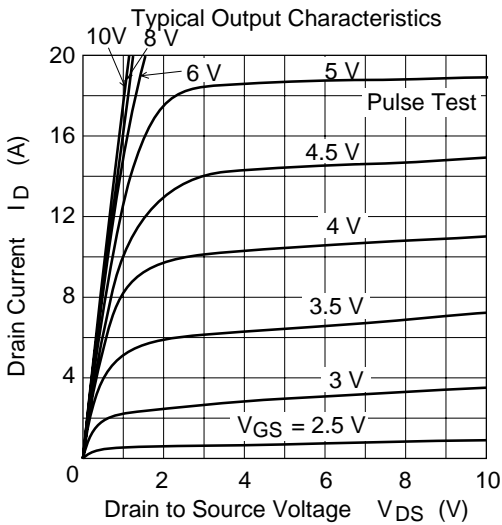
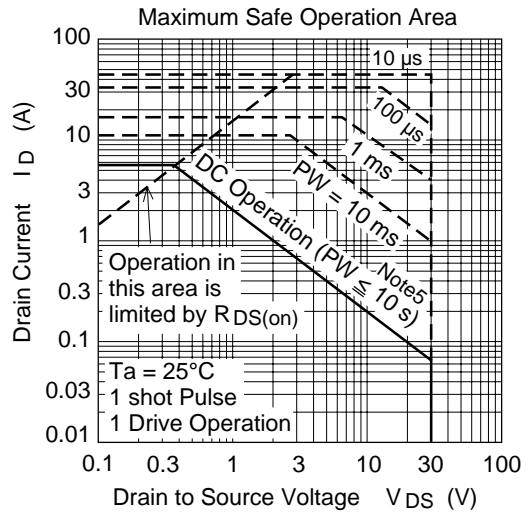
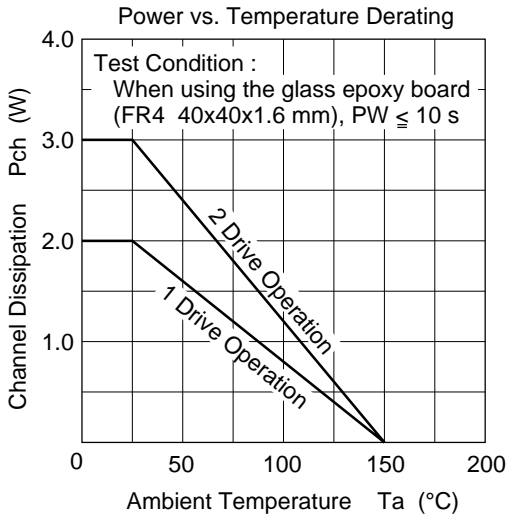
3. 2 Drive operation : When using the glass epoxy board (FR4 40 x 40 x 1.6 mm), PW ≤ 10s

Electrical Characteristics (Ta = 25°C)

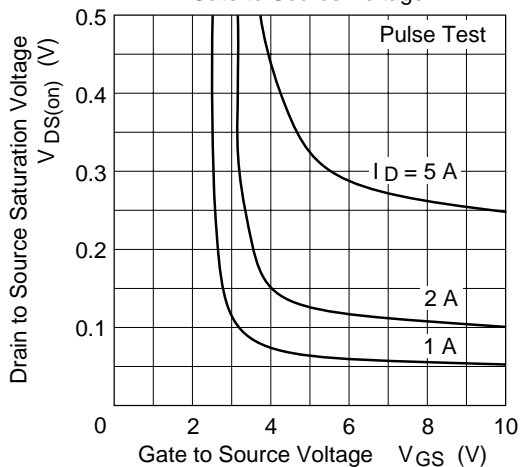
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10\text{mA}$, $V_{GS} = 0$
Gate to source breakdown voltage	$V_{(BR)GSS}$	± 20	—	—	V	$I_G = \pm 100\mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 10	μA	$V_{GS} = \pm 16\text{V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 30\text{V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.0	V	$V_{DS} = 10\text{V}$, $I_D = 1\text{mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	0.05	0.065	Ω	$I_D = 3\text{A}$, $V_{GS} = 10\text{V}^{*1}$
	$R_{DS(on)}$	—	0.078	0.11	Ω	$I_D = 3\text{A}$, $V_{GS} = 4\text{V}^{*1}$
Forward transfer admittance	$ y_{fs} $	3.5	5.5	—	S	$I_D = 3\text{A}$, $V_{DS} = 10\text{V}^{*1}$
Input capacitance	C_{iss}	—	310	—	pF	$V_{DS} = 10\text{V}$
Output capacitance	C_{oss}	—	220	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	100	—	pF	$f = 1\text{MHz}$
Turn-on delay time	$t_{d(on)}$	—	17	—	ns	$V_{GS} = 4\text{V}$, $I_D = 3\text{A}$
Rise time	t_r	—	190	—	ns	$V_{DD} \cong 10\text{V}$
Turn-off delay time	$t_{d(off)}$	—	25	—	ns	
Fall time	t_f	—	60	—	ns	
Body to drain diode forward voltage	V_{DF}	—	0.9	1.4	V	$I_F = 5.5\text{A}$, $V_{GS} = 0^{*1}$
Body to drain diode reverse recovery time	t_{rr}	—	50	—	ns	$I_F = 5.5\text{A}$, $V_{GS} = 0$ $diF/dt = 20\text{A}/\mu\text{s}$

Note: 1. Pulse test

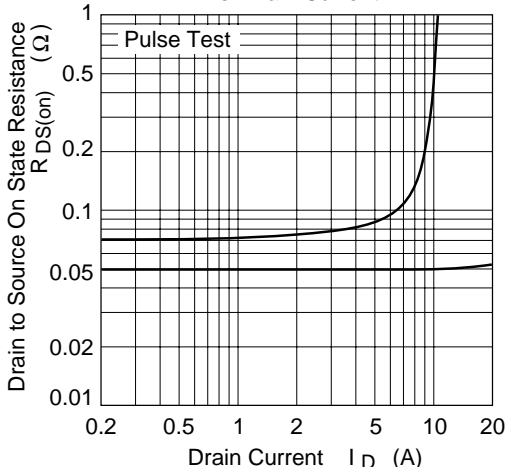
Main Characteristics



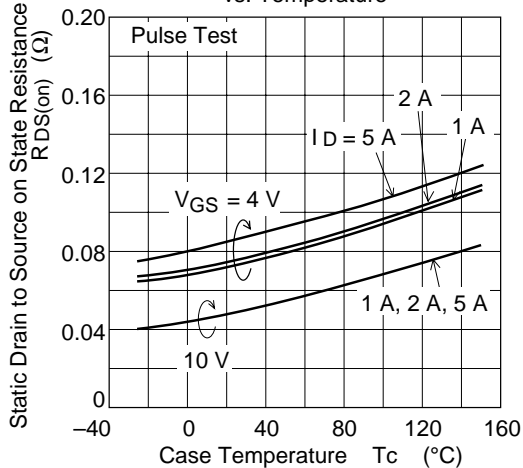
Drain to Source Saturation Voltage vs. Gate to Source Voltage



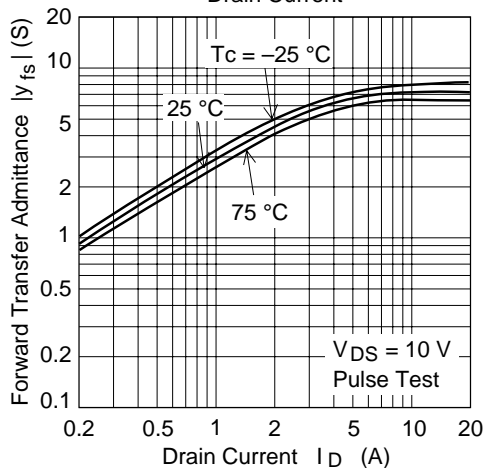
Static Drain to Source on State Resistance vs. Drain Current



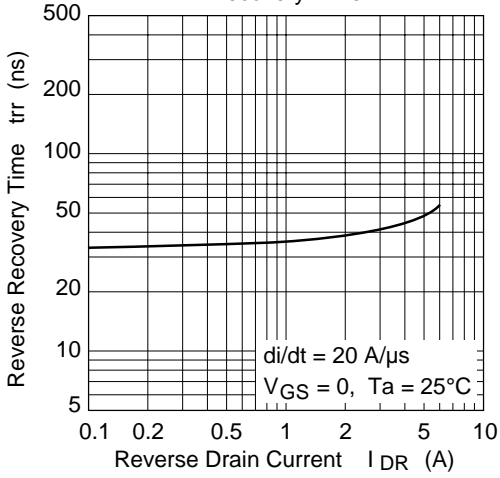
Static Drain to Source on State Resistance vs. Temperature



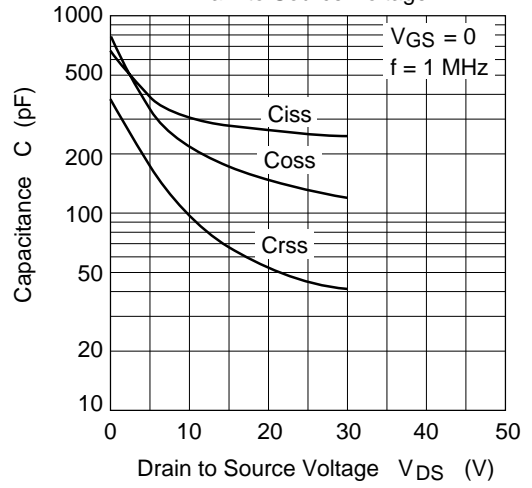
Forward Transfer Admittance vs. Drain Current



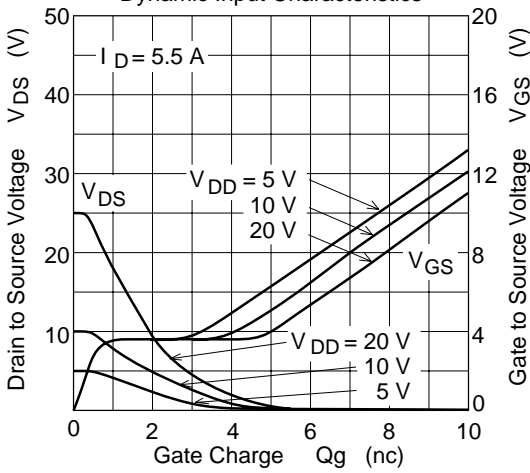
Body-Drain Diode Reverse Recovery Time



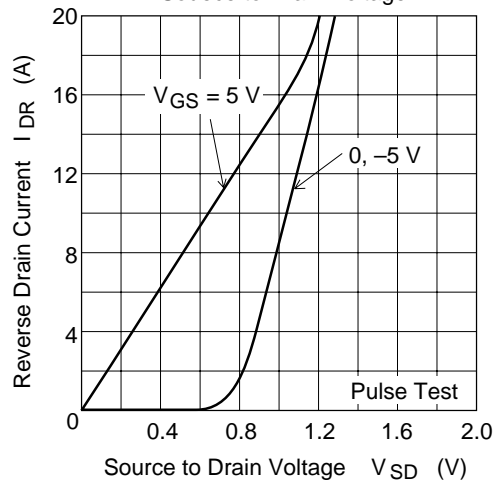
Typical Capacitance vs. Drain to Source Voltage

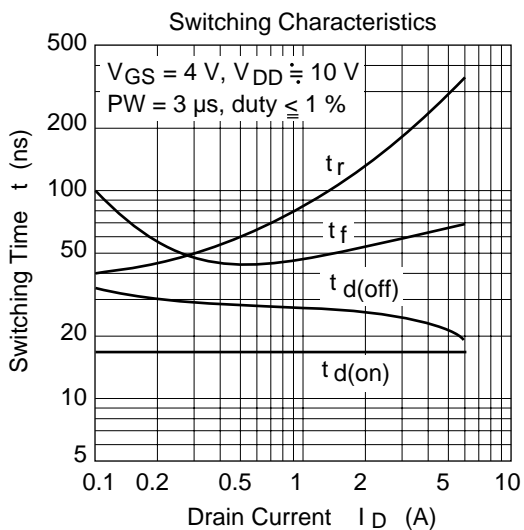


Dynamic Input Characteristics

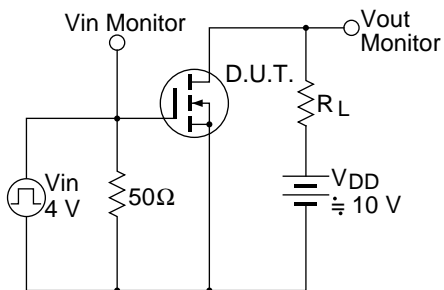


Reverse Drain Current vs. Source to Drain Voltage

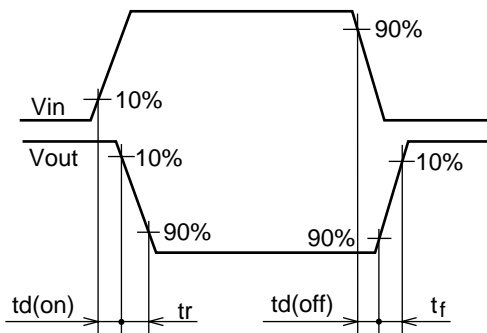


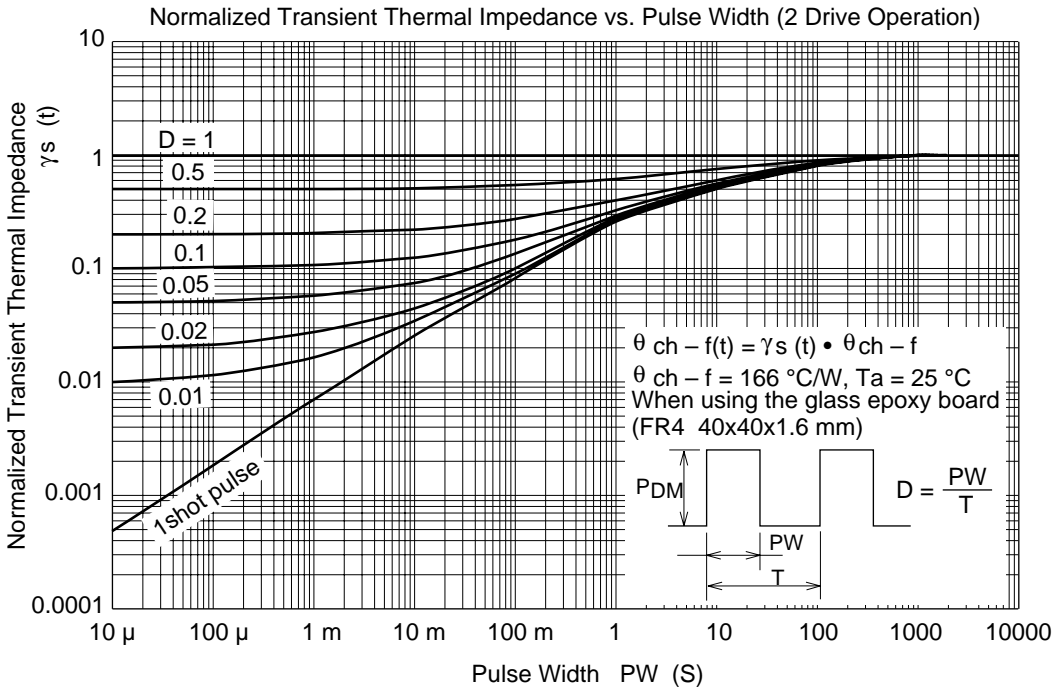
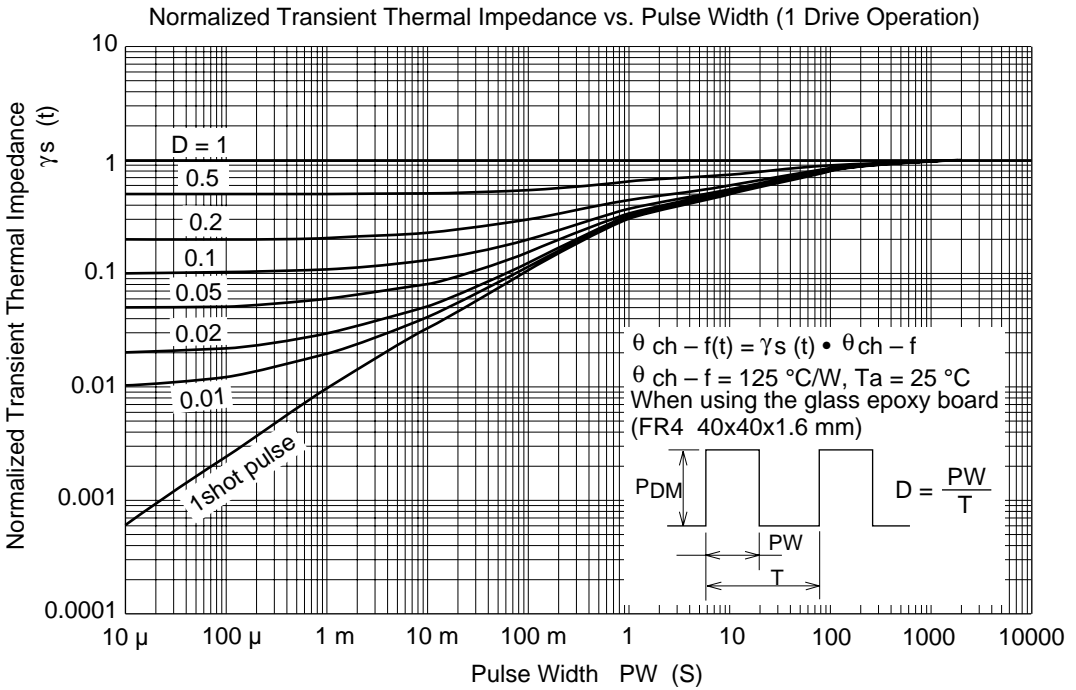


Switching Time Test Circuit



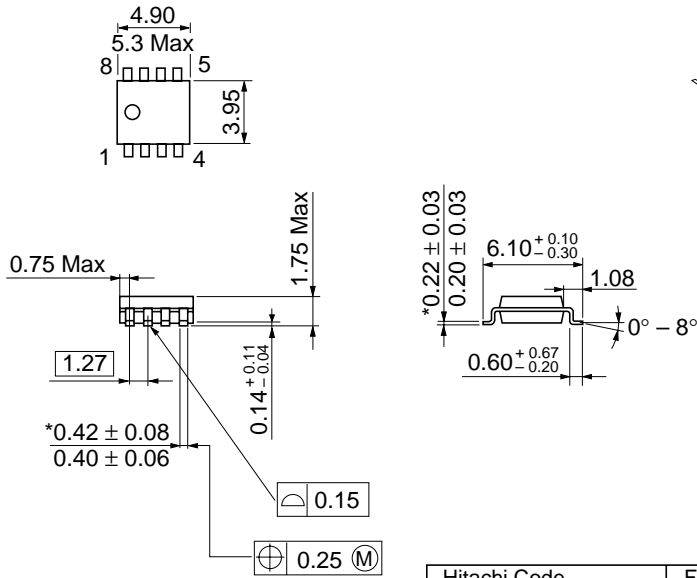
Switching Time Waveform





Package Dimensions

As of January, 2001
Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	FP-8DA
JEDEC	Conforms
EIAJ	—
Mass (reference value)	0.085 g

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