

IRF7700

HEXFET® Power MOSFET

- Ultra Low On-Resistance
- P-Channel MOSFET
- Very Small SOIC Package
- Low Profile (< 1.1mm)
- Available in Tape & Reel

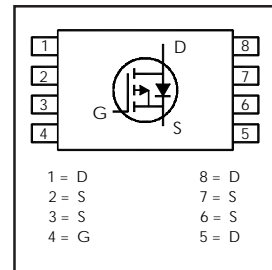
V _{DSS}	R _{DS(on)} max	I _D
-20V	0.015@V _{GS} = -4.5V	-8.6A
	0.024@V _{GS} = -2.5V	-7.3A

Description

HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the ruggedized device design, that International Rectifier is well known for, provides the designer with an extremely efficient and reliable device for use in battery and load management.

The TSSOP-8 package, has 45% less footprint area than the standard SO-8. This makes the TSSOP-8 an ideal device for applications where printed circuit board space is at a premium.

The low profile (<1.1mm) of the TSSOP-8 will allow it to fit easily into extremely thin application environments such as portable electronics and PCMCIA cards.



Absolute Maximum Ratings

	Parameter	Max.	Units
V _{DS}	Drain- Source Voltage	-20	V
I _D @ T _C = 25°C	Continuous Drain Current, V _{GS} @ -4.5V	±8.6	A
I _D @ T _C = 70°C	Continuous Drain Current, V _{GS} @ -4.5V	±6.8	
I _{DM}	Pulsed Drain Current ①	±68	
P _D @T _C = 25°C	Power Dissipation	1.5	W
P _D @T _C = 70°C	Power Dissipation	0.96	
	Linear Derating Factor	0.01	
V _{GS}	Gate-to-Source Voltage	± 12	V
T _J , T _{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

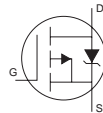
Thermal Resistance

	Parameter	Max.	Units
R _{θJA}	Maximum Junction-to-Ambient③	83	°C/W

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	-20	—	—	V	V _{GS} = 0V, I _D = -250μA
ΔV _{(BR)DSS} /ΔT _J	Breakdown Voltage Temp. Coefficient	—	0.011	—	V/°C	Reference to 25°C, I _D = -1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	—	0.015 0.024	Ω	V _{GS} = -4.5V, I _D = -8.6A ② V _{GS} = -2.5V, I _D = -7.3A ②
V _{GS(th)}	Gate Threshold Voltage	-0.45	—	-1.2	V	V _{DS} = V _{GS} , I _D = -250μA
g _{fs}	Forward Transconductance	-20	—	—	S	V _{DS} = -10V, I _D = -8.6A
I _{DSS}	Drain-to-Source Leakage Current	—	—	-1.0 -25	μA	V _{DS} = -16V, V _{GS} = 0V V _{DS} = -16V, V _{GS} = 0V, T _J = 70°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	-100	nA	V _{GS} = -12V
	Gate-to-Source Reverse Leakage	—	—	100		V _{GS} = 12V
Q _g	Total Gate Charge	—	59	89	nC	I _D = -8.6A
Q _{gs}	Gate-to-Source Charge	—	10	15		V _{DS} = -16V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	19	29		V _{GS} = -5.0V ②
t _{d(on)}	Turn-On Delay Time	—	19	—	ns	V _{DD} = -10V
t _r	Rise Time	—	40	—		I _D = -1.0A
t _{d(off)}	Turn-Off Delay Time	—	120	—		R _G = 6.0Ω
t _f	Fall Time	—	130	—		V _{GS} = -4.5V ②
C _{iss}	Input Capacitance	—	4300	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	880	—		V _{DS} = -15V
C _{rss}	Reverse Transfer Capacitance	—	580	—		f = TBDkHz

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	-1.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	-68		
V _{SD}	Diode Forward Voltage	—	—	-1.2	V	T _J = 25°C, I _S = -1.5A, V _{GS} = 0V ②
t _{rr}	Reverse Recovery Time	—	130	200	ns	T _J = 25°C, I _F = -1.5A
Q _{rr}	Reverse Recovery Charge	—	180	270	nC	di/dt = 100A/μs ②

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Pulse width ≤ 300μs; duty cycle ≤ 2%.

③ When mounted on 1 inch square copper board, t < 10 sec

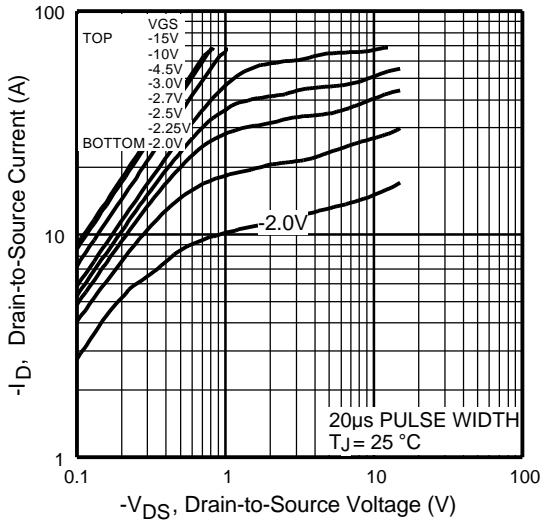


Fig 1. Typical Output Characteristics

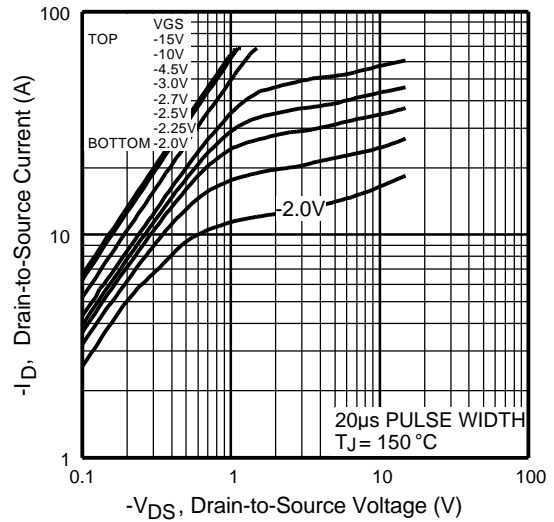


Fig 2. Typical Output Characteristics

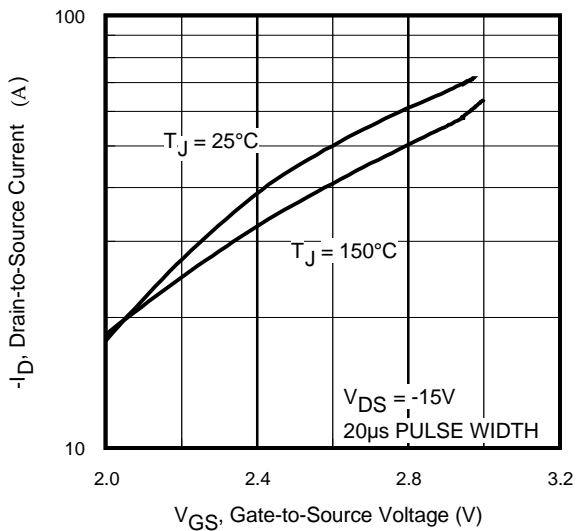


Fig 3. Typical Transfer Characteristics

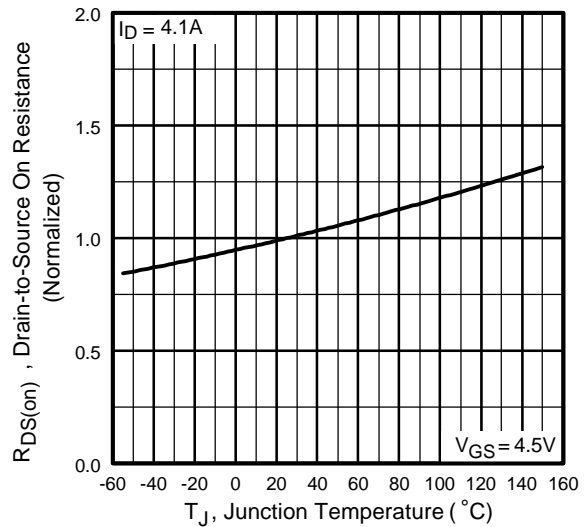


Fig 4. Normalized On-Resistance Vs. Temperature

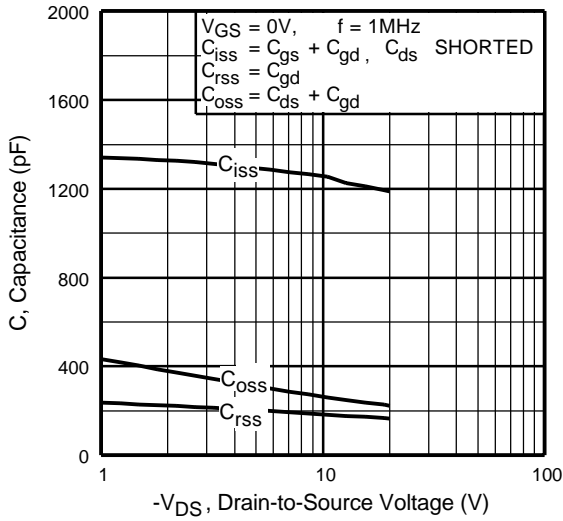


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

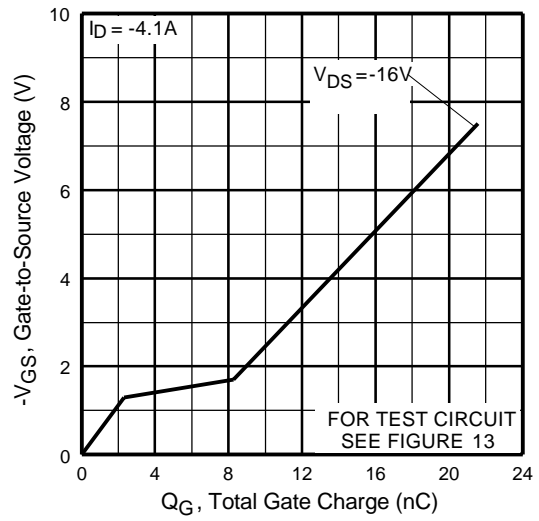


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

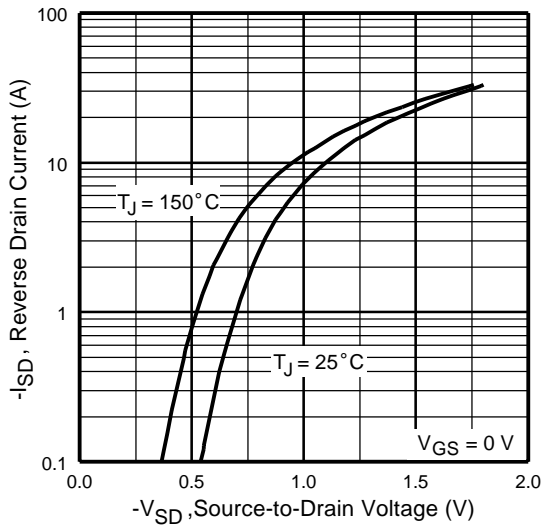


Fig 7. Typical Source-Drain Diode Forward Voltage

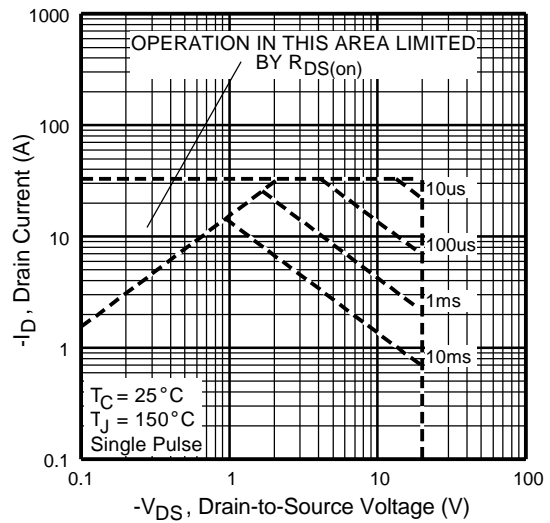


Fig 8. Maximum Safe Operating Area

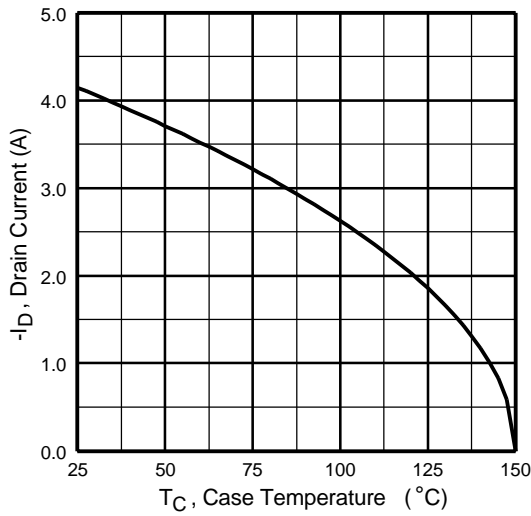


Fig 9. Maximum Drain Current Vs. Case Temperature

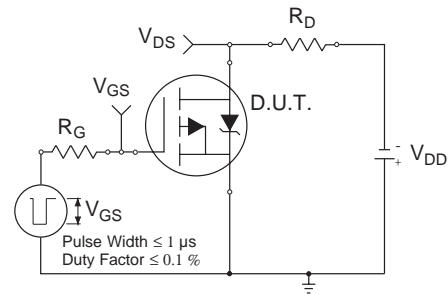


Fig 10a. Switching Time Test Circuit

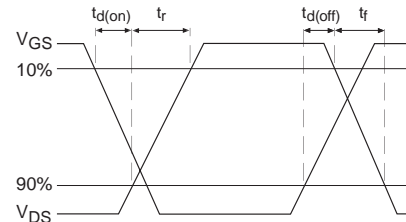


Fig 10b. Switching Time Waveforms

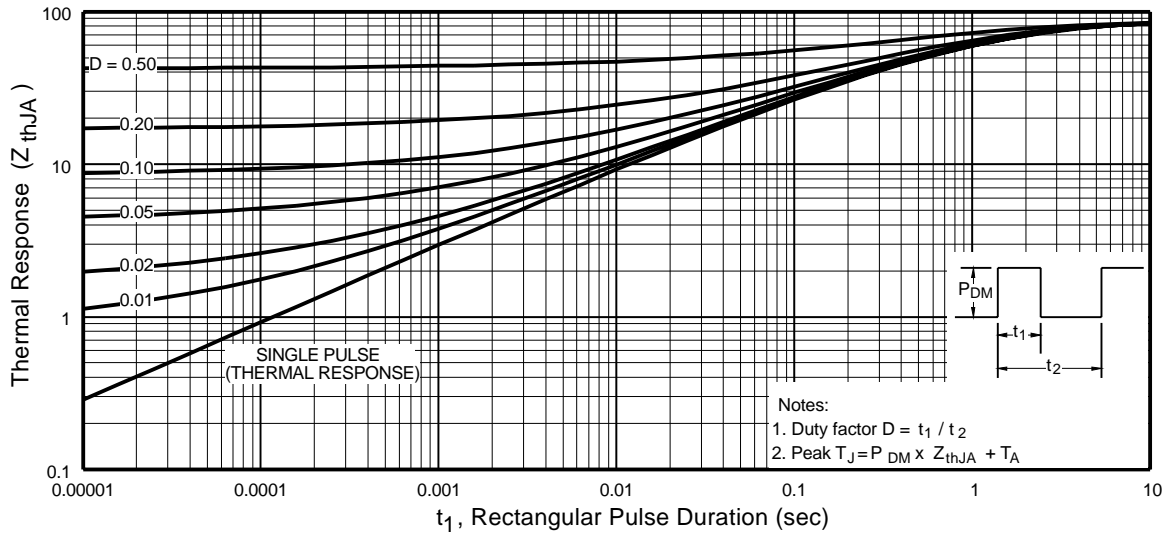


Fig 10. Typical Effective Transient Thermal Impedance, Junction-to-Ambient

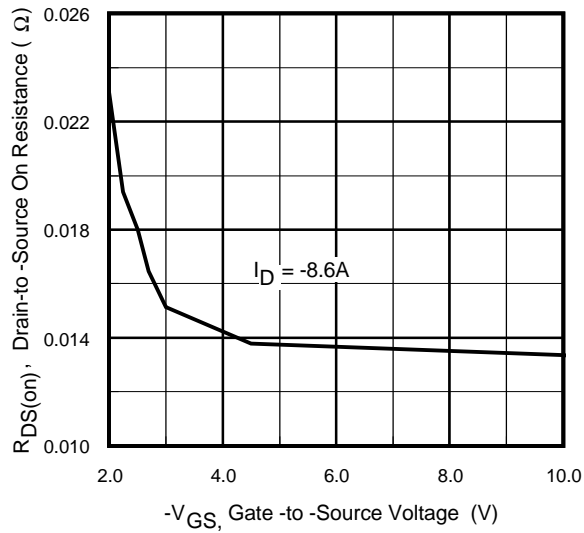


Fig 11. Typical On-Resistance Vs. Gate Voltage

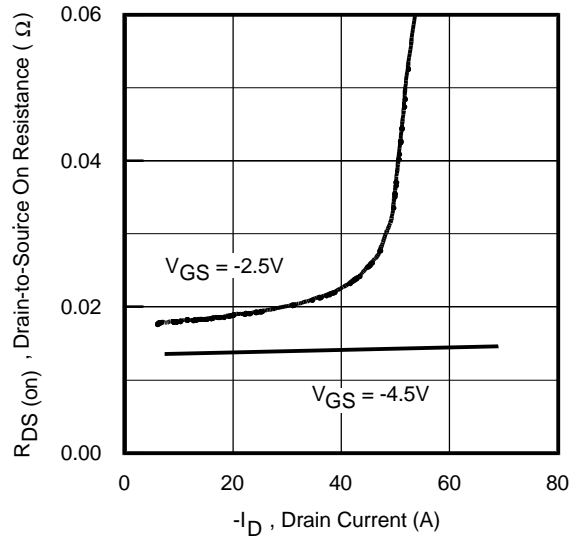


Fig 12. Typical On-Resistance Vs. Drain Current

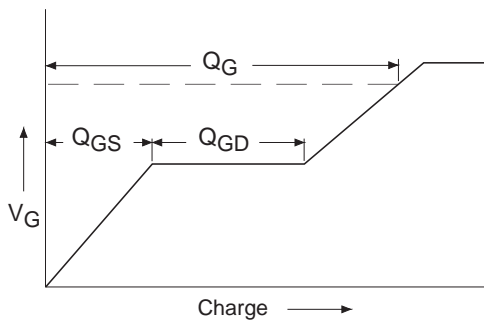


Fig 13a. Basic Gate Charge Waveform

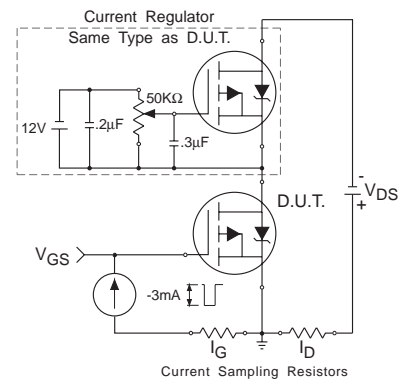


Fig 13b. Gate Charge Test Circuit

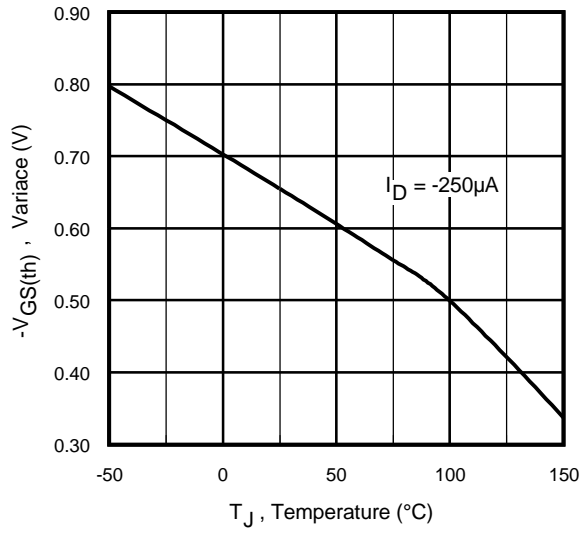


Fig 14. Threshold Voltage Vs. Temperature

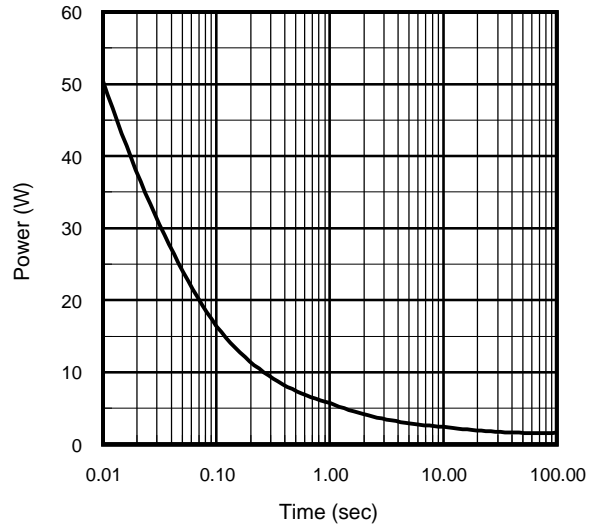
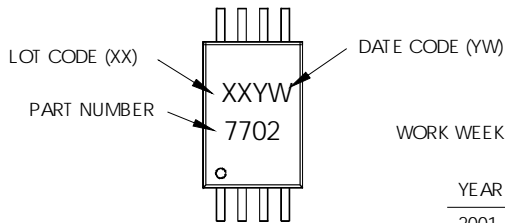


Fig 15. Typical Power Vs. Time

IRF7700

TSSOP-8 Part Marking Information

EXAMPLE: THIS IS AN IRF7702



DATE CODE EXAMPLES:

9503 = 5C
9532 = EF

TABLE 1

WORK WEEK 1-26, NUMERIC YEAR CODE (1,2, ...ETC.)

YEAR	Y	WORK WEEK	W
2001	1	01	A
2002	2	02	B
2003	3	03	C
1994	4	04	D
1995	5		
1996	6		
1997	7		
1998	8		
1999	9		
2000	0	24	X
		25	Y
		26	Z

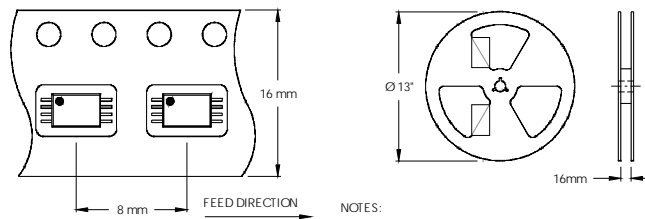
TABLE 2

WORK WEEK 27-52, ALPHANUMERIC YEAR CODE (AB, ...ETC.)

YEAR	Y	WORK WEEK	W
2001	A	27	A
2002	B	28	B
2003	C	29	C
1994	D	30	D
1995	E		
1996	F		
1997	G		
1998	H		
1999	J		
2000	K	50	X
		51	Y
		52	Z

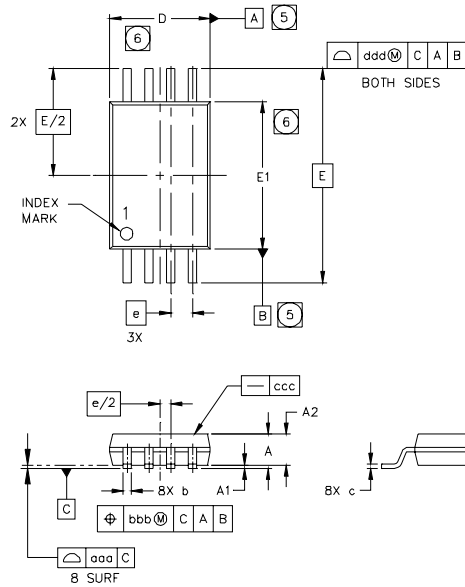
TSSOP-8 Tape and Reel

8LTSSOP (MO-153AA)

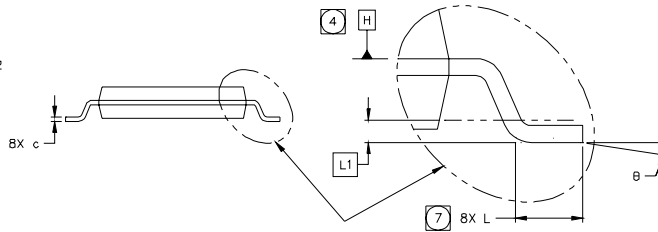


NOTES:
1. TAPE & REEL OUTLINE CONFORMS TO EIA-481 & EIA-541.

TSSOP-8 Package Outline



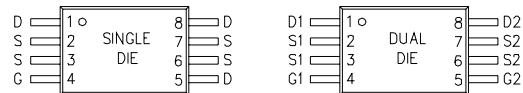
SYMBOL	MO-153AA DIMENSIONS					
	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	---	---	1.20	---	---	.0472
A1	0.05	---	0.15	.0020	---	.0059
A2	0.80	1.00	1.05	.032	.039	.041
b	0.19	---	0.30	.0075	---	.0118
c	0.09	---	0.20	.0036	---	.0078
D	2.90	3.00	3.10	.115	.118	.122
E	6.40 BSC			.251 BSC		
E1	4.30	4.40	4.50	.170	.173	.177
e	0.65 BSC			.0256		
L	0.45	0.60	0.75	.0178	.0236	.0290
L1	0.25 BSC			.010 BSC		
Ø	0°	---	8°	0°	---	8°
aaa	0.10			.0039		
bbb	0.10			.0039		
ccc	0.05			.0019		
ddd	0.20			.0078		



NOTES

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
2. DIMENSIONS ARE SHOWN IN MILLIMETERS AND INCHES.
3. CONTROLLING DIMENSION: MILLIMETER.
4. DATUM PLANE H IS LOCATED AS SHOWN.
5. DATUM A AND B TO BE DETERMINED AT DATUM PLANE H.
6. DIMENSIONS D AND E1 ARE MEASURED AT DATUM PLANE H.
7. DIMENSION L IS THE LEAD LENGTH FOR SOLDERING TO A SUBSTRATE.
8. OUTLINE CONFORMS TO JEDEC OUTLINE MO-153AA.

LEAD ASSIGNMENTS





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