

INTERNATIONAL RECTIFIER

REPETITIVE AVALANCHE RATED AND dv/dt RATED

HEXFET[®] TRANSISTOR

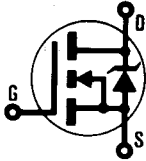
IRFM140

2N7218

JANTX2N7218

JANTXV2N7218

[REF: MIL-S-19500/596]



N-CHANNEL

100 Volt, 0.077 Ohm HEXFET

The HEXFET[®] technology is the key to International Rectifier's advanced line of power MOSFET transistors. The efficient geometry design achieves very low on-state resistance combined with high transconductance.

The HEXFET transistors also feature all of the well established advantages of MOSFETs such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

They are well suited for applications such as switching power supplies and virtually any application where military and/or high reliability is required.

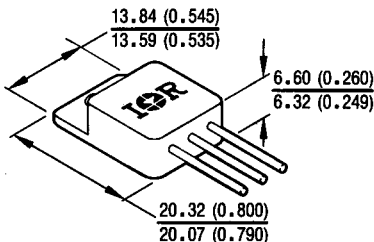
Product Summary

Part Number	V_{DSS}	$R_{DS(on)}$	I_D
IRFM140	100V	0.077 Ω	28A

FEATURES:

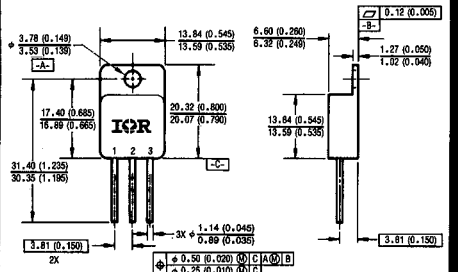
- Repetitive Avalanche Rating
- Isolated and Hermetically Sealed
- Alternative to TO-3 Package
- Simple Drive Requirements
- Ease of Paralleling
- Ceramic Eyelets

CASE STYLE AND DIMENSIONS



CAUTION

BERYLLIA WARNING PER MIL-S-19500
SEE PAGE I-300



- LEGEND
1 DRAIN
2 SOURCE
3 GATE

NOTES:

- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M - 1982.
- 2 ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).

Conforms to JEDEC Outline TO-254AA*
Dimensions in Millimeters and (Inches)

*For leadform configurations see page I-300, fig. 15

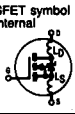


Absolute Maximum Ratings

Parameter	IRFM140, JANTXV, JANTX-, 2N7218	Units
I_D @ $V_{GS} = 10V, T_C = 25^\circ C$	Continuous Drain Current	28
I_D @ $V_{GS} = 10V, T_C = 100^\circ C$	Continuous Drain Current	20
I_{DM}	Pulsed Drain Current ①	112
P_D @ $T_C = 25^\circ C$	Max. Power Dissipation	125
	Linear Derating Factor	1.0
V_{GS}	Gate-to-Source Voltage ²	± 20
E_{AS}	Single Pulse Avalanche Energy ②	250 (See Fig. 12)
I_{AR}	Avalanche Current ①	28 (See E_{AR})
E_{AR}	Repetitive Avalanche Energy ①	12.5 (See Fig. 13)
dv/dt	Peak Diode Recovery dv/dt ③	5.5 (See Fig. 13)
T_J	Operating Junction	-55 to 150
T_{STG}	Storage Temperature Range	
	Lead Temperature	300 (0.063 in. (1.6 mm) from case for 10s)
	Weight	9.3 (typical)


Electrical Characteristics @ $T_J = 25^\circ C$ (Unless Otherwise Specified)

Parameter	Min.	Typ.	Max.	Units	Test Conditions	
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	$V_{GS} = 0V, I_D = 1.0 mA$
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.13	—	$V/^\circ C$	Reference to $25^\circ C, I_D = 1.0 mA$
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.077	Ω	$V_{GS} = 10V, I_D = 20A$ ④
		—	—	0.125		$V_{GS} = 10V, I_D = 28A$
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250 \mu A$
g_{fs}	Forward Transconductance	9.1	—	—	S (⑤)	$V_{DS} \geq 15V, I_{DS} = 20A$ ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	25	μA	$V_{DS} = 0.8 \times \text{Max. Rating}, V_{GS} = 0V$
		—	—	250		$V_{DS} = 0.8 \times \text{Max. Rating}$ $V_{GS} = 0V, T_J = 125^\circ C$
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	$V_{GS} = 20V$
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	30	—	59	nC	$V_{GS} = 10V, I_D = 28A$
Q_{gs}	Gate-to-Source Charge	2.4	—	12		$V_{DS} = 0.5 \times \text{Max. Rating}$
Q_{gd}	Gate-to-Drain ("Miller") Charge	12	—	30.7		See Fig. 6 and 14
$t_{d(on)}$	Turn-On Delay Time	—	—	21	ns	$V_{DD} = 50V, I_D = 20A, R_G = 9.1\Omega$
t_r	Rise Time	—	—	145		
$t_{d(off)}$	Turn-Off Delay Time	—	—	64		See Fig. 11
t_f	Fall Time	—	—	105		
L_D	Internal Drain Inductance	—	8.7	—	nH	Measured from the drain lead, 6 mm (0.25 in.) from package to center of die.
L_S	Internal Source Inductance	—	8.7	—		Measured from the source lead, 6 mm (0.25 in.) from package to source bonding pad.
C_{iss}	Input Capacitance	—	1660	—	pF	$V_{GS} = 0V, V_{DS} = 25V$
C_{oss}	Output Capacitance	—	550	—		$f = 1.0 MHz$
C_{rss}	Reverse Transfer Capacitance	—	120	—		See Fig. 5
C_{DC}	Drain-to-Case Capacitance	—	12	—		





Source-Drain Diode Ratings and Characteristics

Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S Continuous Source Current (Body Diode)	—	—	28	A	Modified MOSFET symbol showing the integral Reverse p-n junction rectifier. 
I_{SM} Pulsed Source Current (Body Diode) ①	—	—	112		
V_{SD} Diode Forward Voltage	—	—	1.5	V	$T_J = 25^\circ\text{C}$, $I_S = 28\text{A}$, $V_{GS} = 0\text{V}$ ④
t_{rr} Reverse Recovery Time	—	—	400	nS	$T_J = 25^\circ\text{C}$, $I_F = 28\text{A}$, $di/dt \leq 100\text{ A}/\mu\text{s}$ ④
Q_{RR} Reverse Recovery Charge	—	—	2.9	μC	$V_{DD} \leq 50\text{V}$
t_{on} Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by $L_S + L_D$.				

Thermal Resistance

Parameter	Min.	Typ.	Max.	Units	Test Conditions
R_{thJC} Junction-to-Case	—	—	1.0	K/W ⑤	
R_{thJS} Case-to-Sink	—	0.21	—		Mounting surface flat, smooth, and greased
R_{thJA} Junction-to-Ambient	—	—	48		Typical socket mount

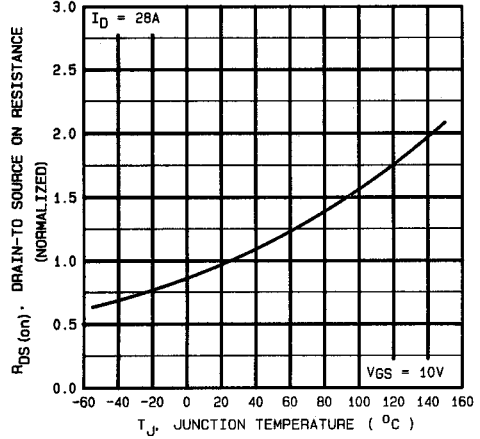
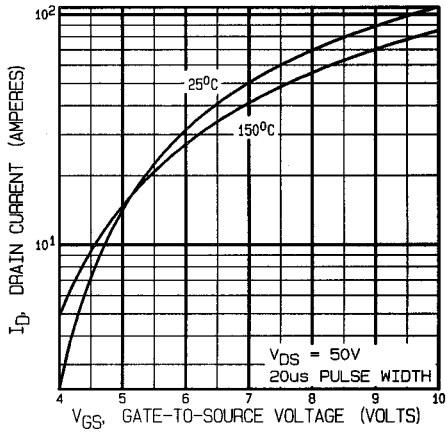
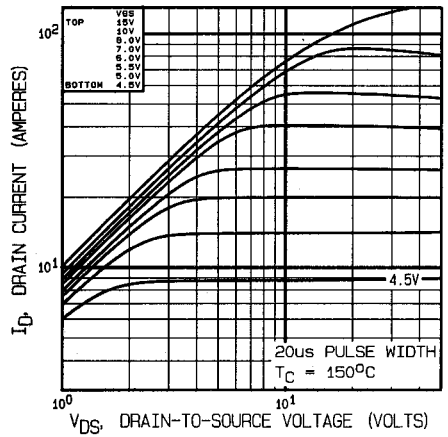
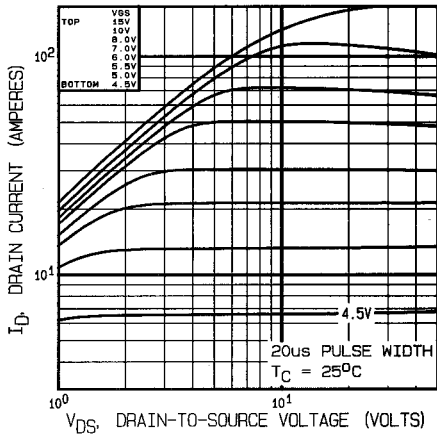
① Repetitive Rating; Pulse width limited by maximum junction temperature (see figure 9) Refer to current HEXFET reliability report

② @ $V_{DD} = 25\text{V}$, Starting $T_J = 25^\circ\text{C}$, $L \geq 470\ \mu\text{H}$, $R_G = 25\Omega$, Peak $I_L = 28\text{A}$

③ $I_{SD} \leq 28\text{A}$, $di/dt \leq 170\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, $T_J \leq 150^\circ\text{C}$ Suggested $R_G = 9.1\ \Omega$

④ Pulse width $\leq 300\ \mu\text{s}$; Duty Cycle $\leq 2\%$

⑤ $K/W = ^\circ\text{C}/\text{W}$
 $W/K = \text{W}/^\circ\text{C}$



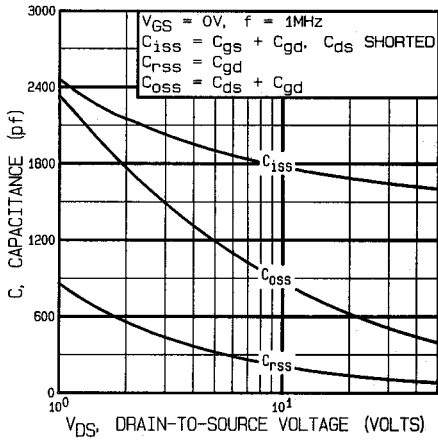


Fig. 5 — Typical Capacitance Vs. Drain-to-Source Voltage

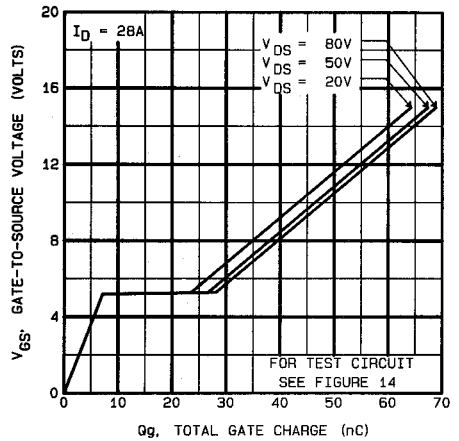


Fig. 6 — Typical Gate Charge Vs. Gate-to-Source Voltage

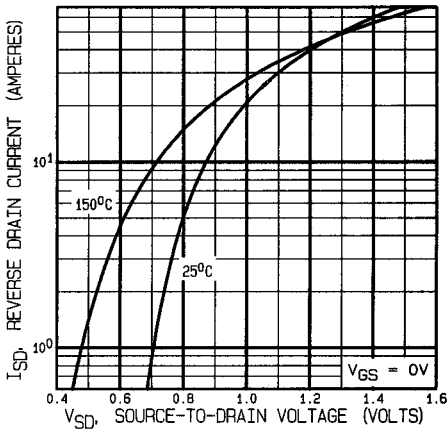


Fig. 7 — Typical Source-Drain Diode Forward Voltage

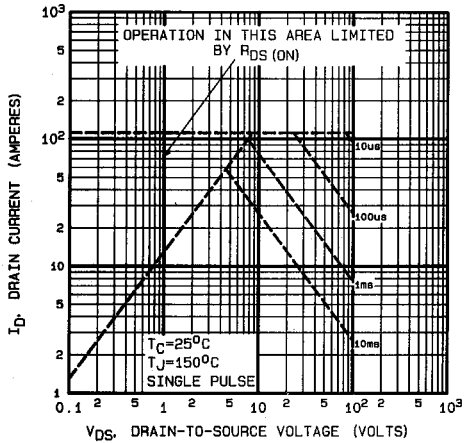


Fig. 8 — Maximum Safe Operating Area

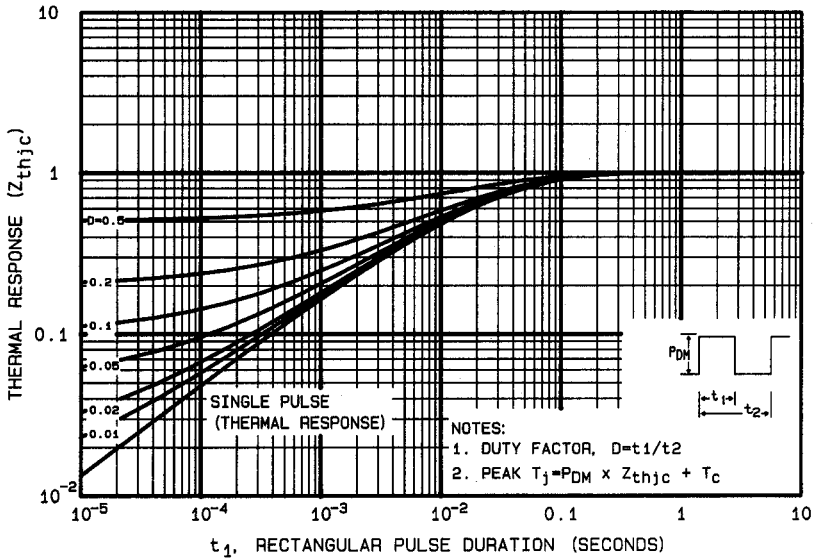


Fig. 9 — Maximum Effective Transient Thermal Impedance, Junction-to-Case Vs. Pulse Duration

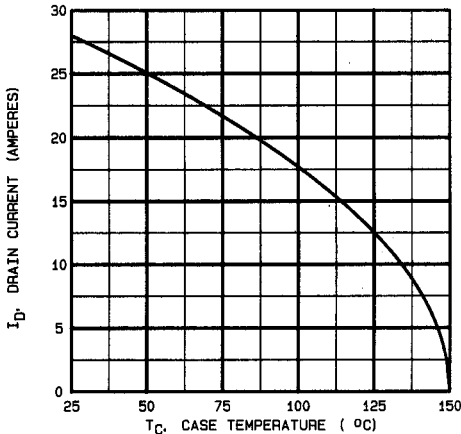


Fig. 10 — Maximum Drain Current Vs. Case Temperature

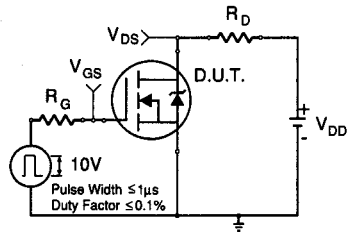


Fig. 11a — Switching Time Test Circuit

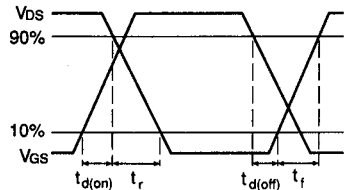


Fig. 11b — Switching Time Waveforms

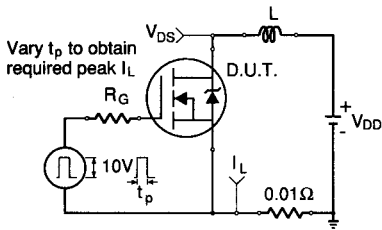


Fig. 12a — Unclamped Inductive Test Circuit

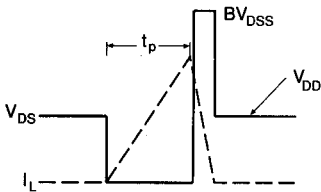


Fig. 12b — Unclamped Inductive Waveforms

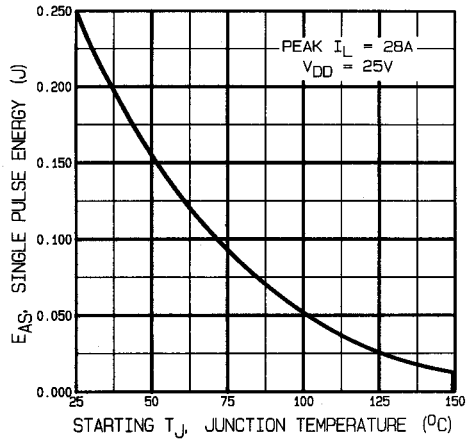


Fig. 12c — Maximum Avalanche Energy Vs. Starting Junction Temperature

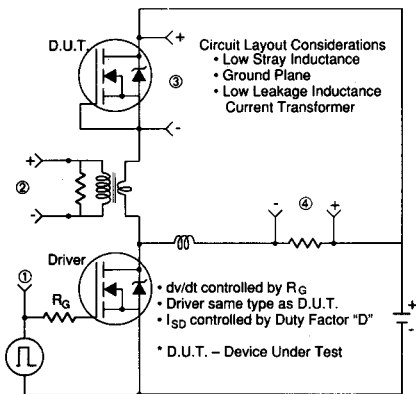
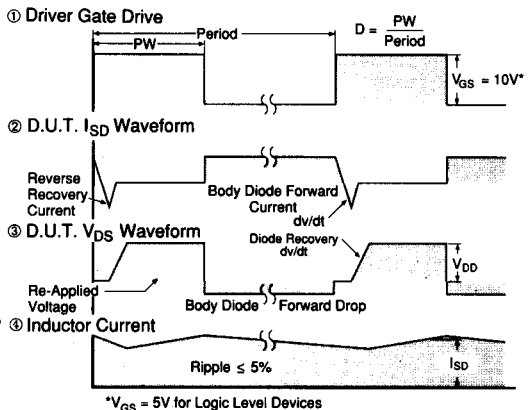


Fig. 13 — Peak Diode Recovery dv/dt Test Circuit



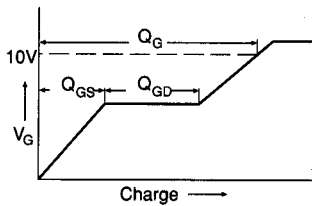


Fig. 14a — Basic Gate Charge Waveform

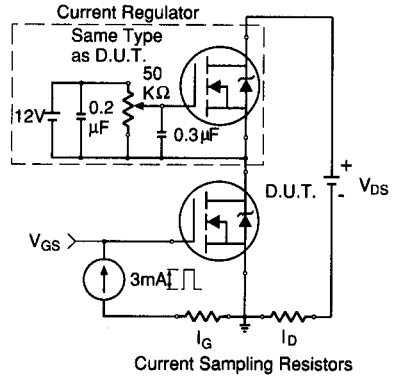


Fig. 14b — Gate Charge Test Circuit

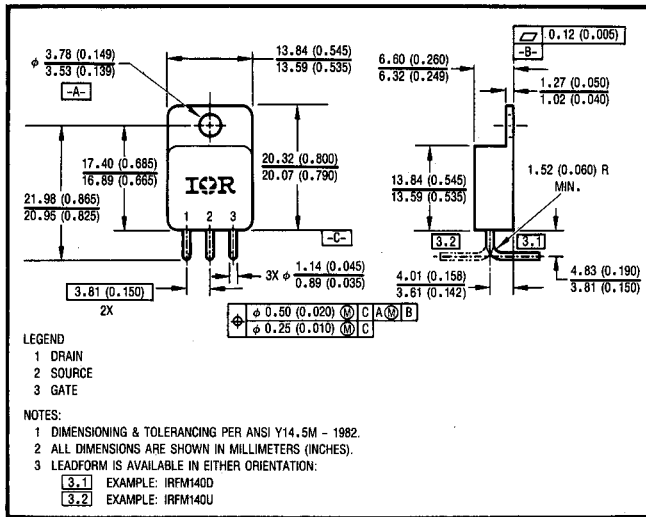


Fig. 15 — Optional Leadforms for Outline TO-254

BERYLLIA WARNING PER MIL-S-19500

Packages containing beryllia shall not be ground, sandblasted, machined, or have other operations performed on them which will produce beryllia or beryllium dust. Furthermore, beryllium oxide packages shall not be placed in acids that will produce fumes containing beryllium.



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