

IRFR3411 IRFU3411

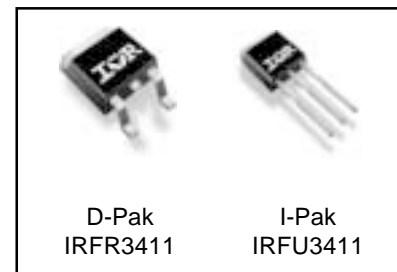
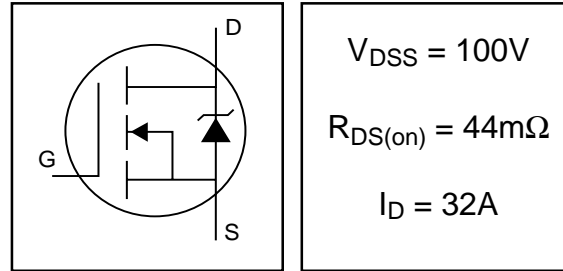
HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

Description

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D-Pak is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead, I-Pak, version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



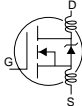
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	32	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	23	
I_{DM}	Pulsed Drain Current ①	110	
$P_D @ T_C = 25^\circ C$	Power Dissipation	130	W
	Linear Derating Factor	0.83	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current ①	16	A
E_{AR}	Repetitive Avalanche Energy ①	13	mJ
dv/dt	Peak Diode Recovery dv/dt ③	7.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		

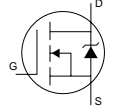
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.2	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DS(on)}	Static Drain-to-Source On-Resistance	—	36	44	mΩ	V _{GS} = 10V, I _D = 16A ④
V _{GS(th)}	Gate Threshold Voltage	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	21	—	—	S	V _{DS} = 50V, I _D = 16A④
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 100V, V _{GS} = 0V
		—	—	250		V _{DS} = 80V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -20V
Q _g	Total Gate Charge	—	48	71	nC	I _D = 16A
Q _{gs}	Gate-to-Source Charge	—	9.0	14		V _{DS} = 80V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	14	21		V _{GS} = 10V, See Fig. 6 and 13
t _{d(on)}	Turn-On Delay Time	—	11	—	ns	V _{DD} = 50V
t _r	Rise Time	—	35	—		I _D = 16A
t _{d(off)}	Turn-Off Delay Time	—	39	—		R _G = 5.1Ω
t _f	Fall Time	—	35	—		V _{GS} = 10V, See Fig. 10 ④
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	1960	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	250	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	40	—		f = 1.0MHz, See Fig. 5
E _{AS}	Single Pulse Avalanche Energy②	—	700⑤	185⑥		mJ

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	33	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode)①	—	—	110		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _S = 16A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	115	170	ns	T _J = 25°C, I _F = 16A
Q _{rr}	Reverse Recovery Charge	—	505	760	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting T_J = 25°C, L = 1.5mH
R_G = 25Ω, I_{AS} = 16A. (See Figure 12)
- ③ I_{SD} ≤ 16A, di/dt ≤ 340A/μs, V_{DD} ≤ V_{(BR)DSS},
T_J ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.

⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to T_J = 175°C .

* When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint dering techniques refer to application note #AN-994.

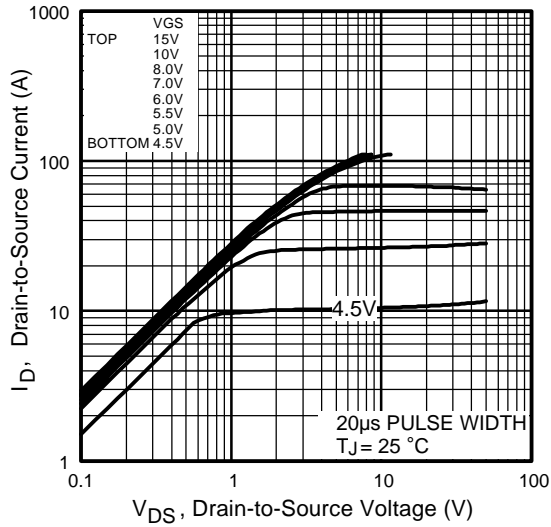


Fig 1. Typical Output Characteristics

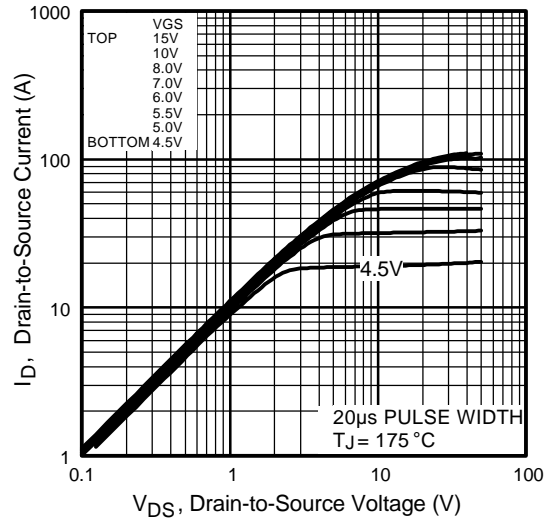


Fig 2. Typical Output Characteristics

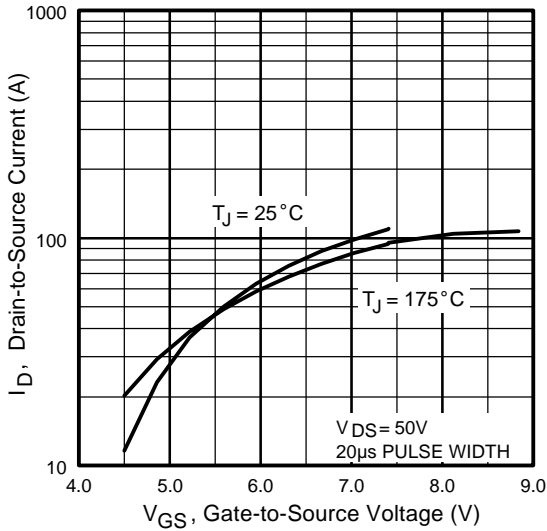


Fig 3. Typical Transfer Characteristics

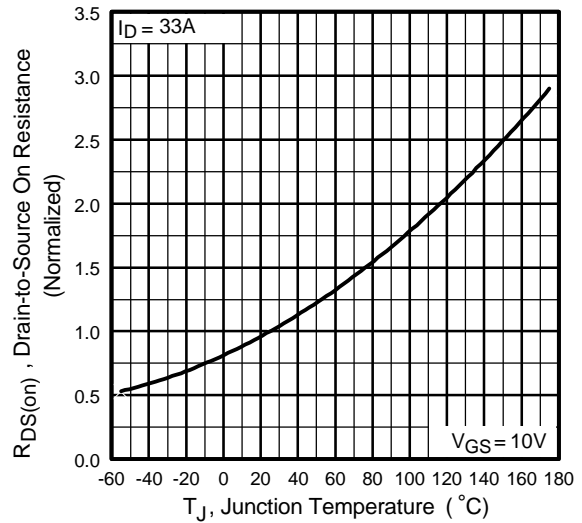


Fig 4. Normalized On-Resistance Vs. Temperature

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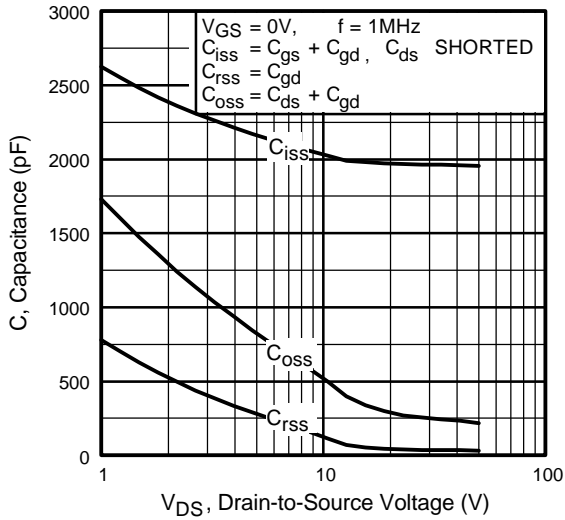


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

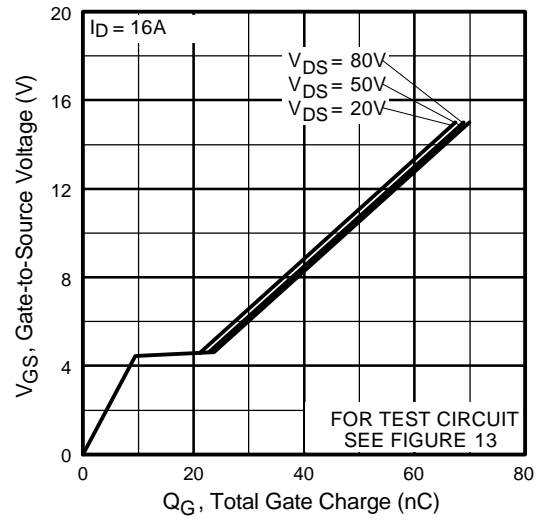


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

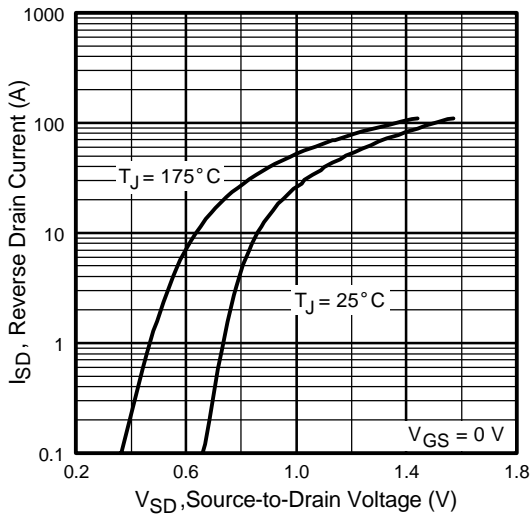


Fig 7. Typical Source-Drain Diode Forward Voltage

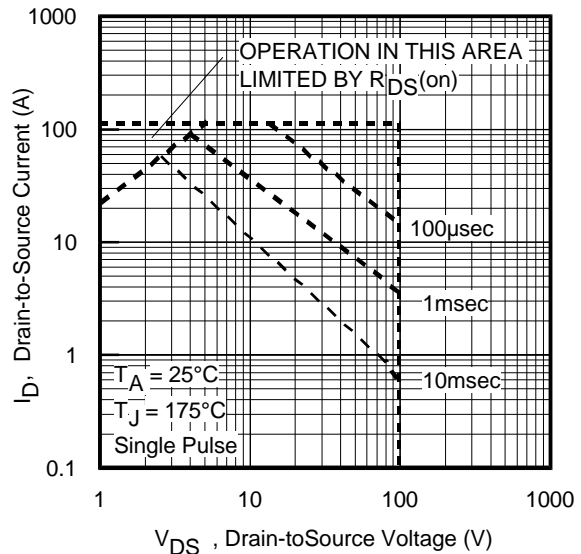


Fig 8. Maximum Safe Operating Area

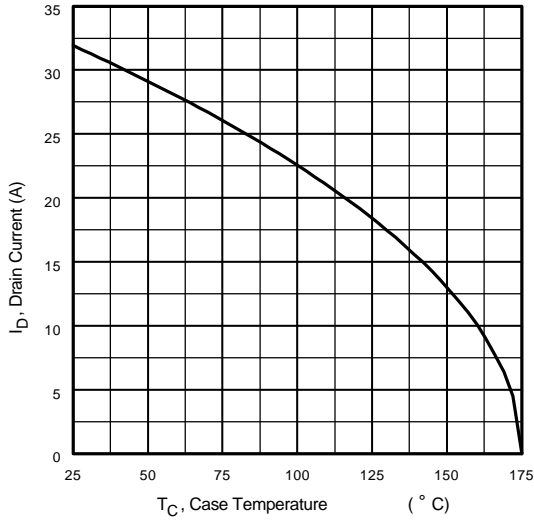


Fig 9. Maximum Drain Current Vs. Case Temperature

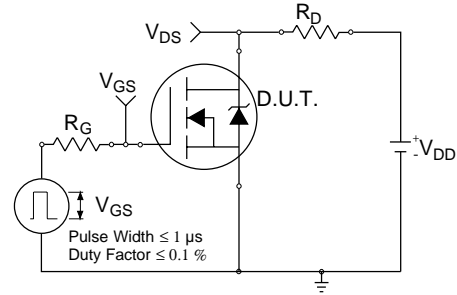


Fig 10a. Switching Time Test Circuit

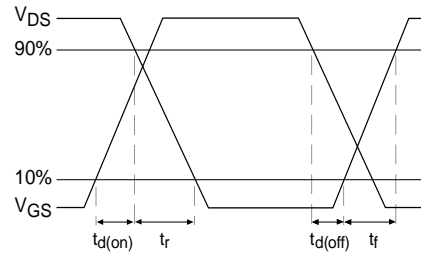


Fig 10b. Switching Time Waveforms

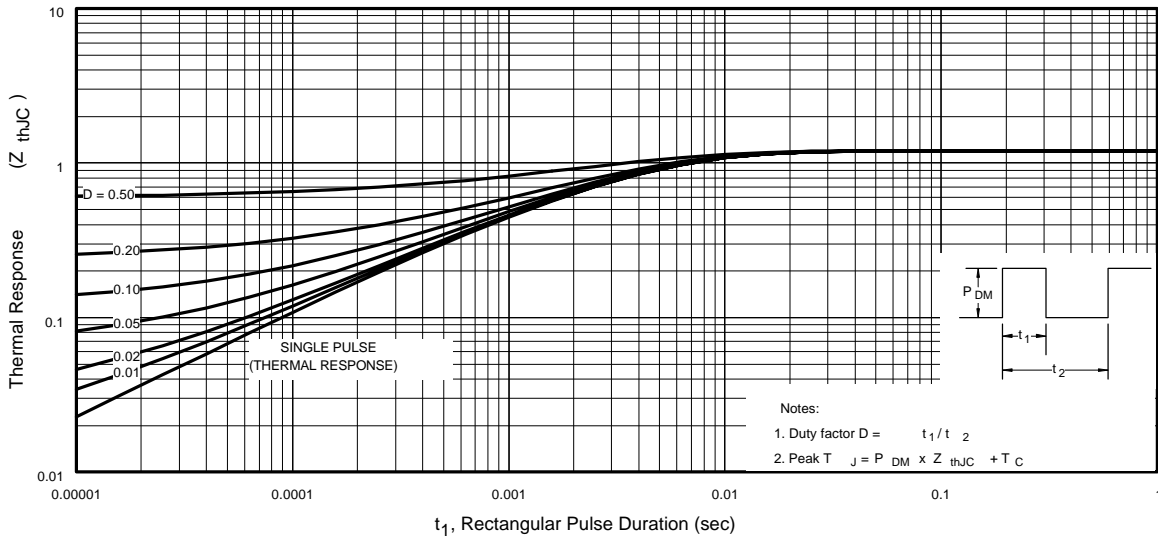


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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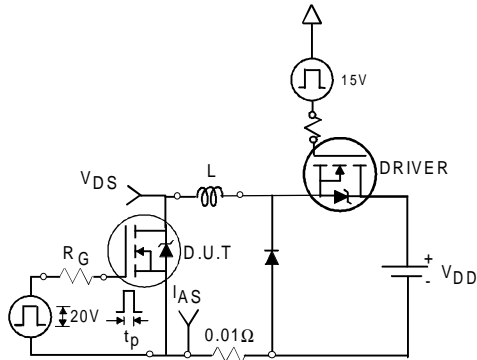


Fig 12a. Unclamped Inductive Test Circuit

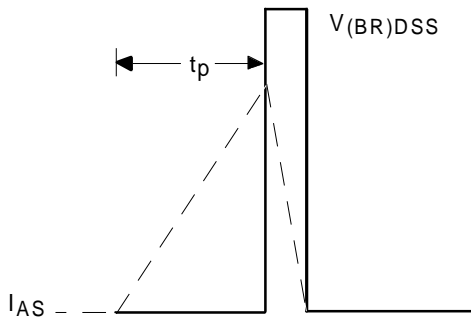


Fig 12b. Unclamped Inductive Waveforms

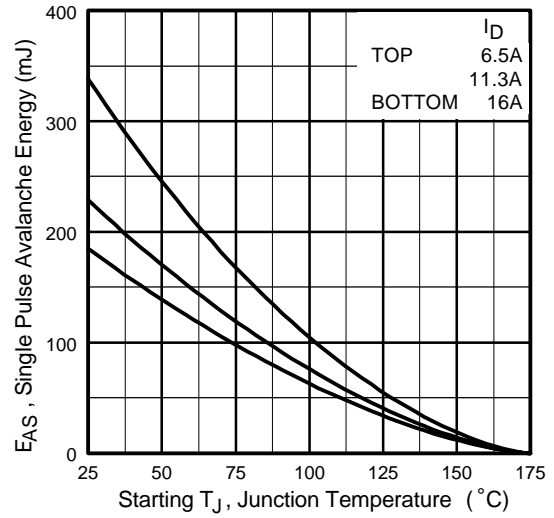


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

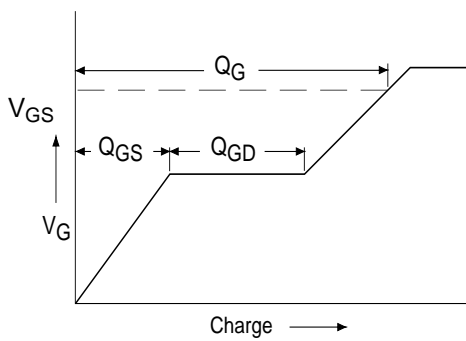


Fig 13a. Basic Gate Charge Waveform

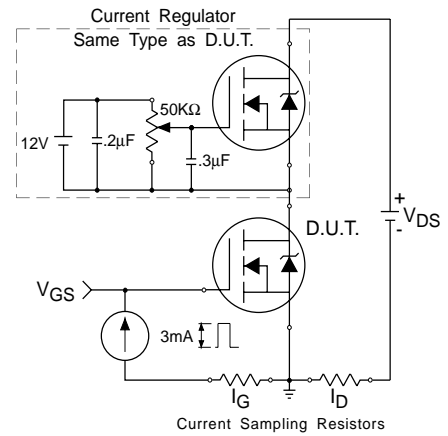
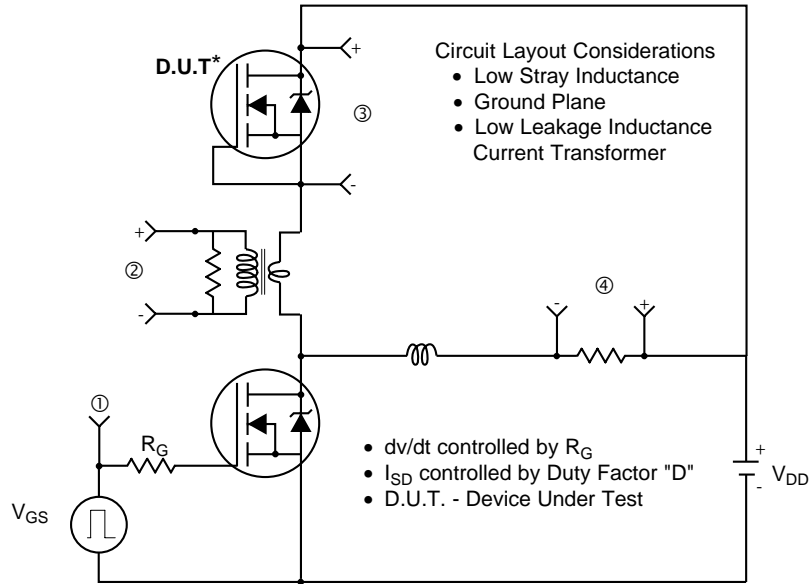
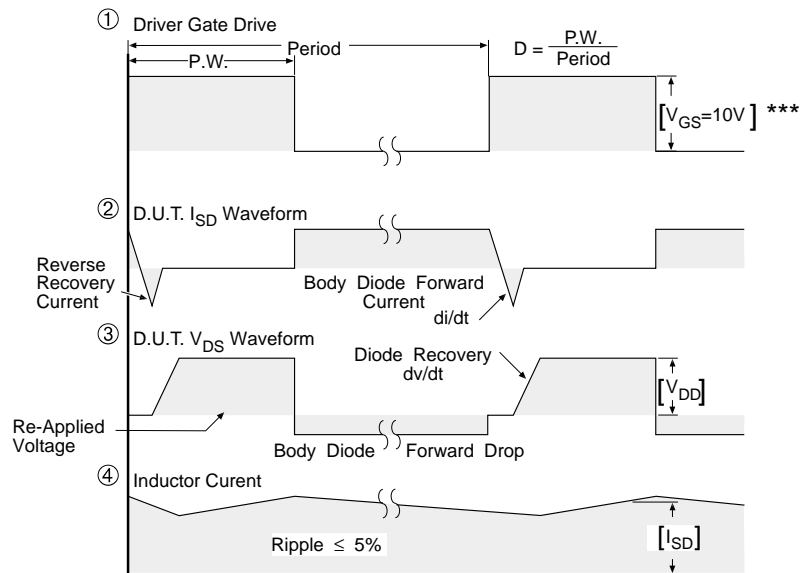


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

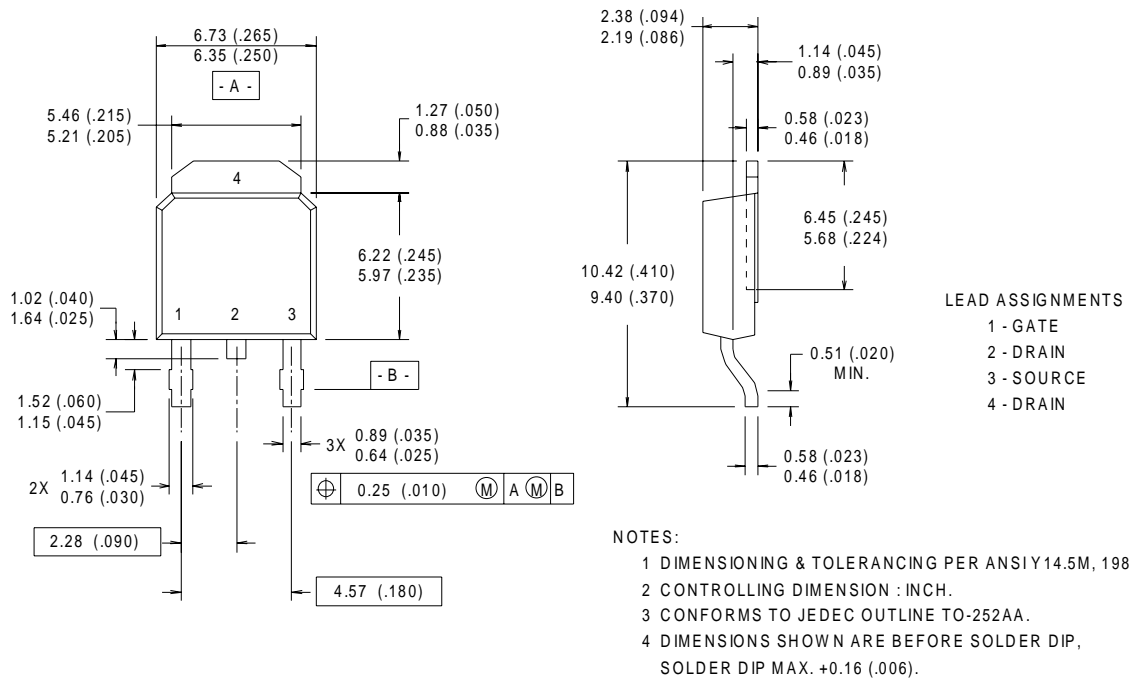
Fig 14. For N-channel HEXFET[®] power MOSFETs

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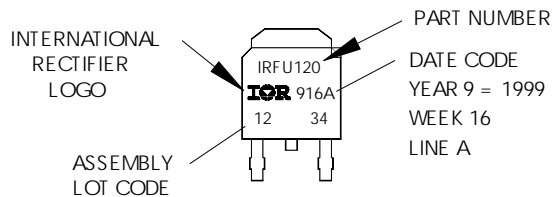
D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



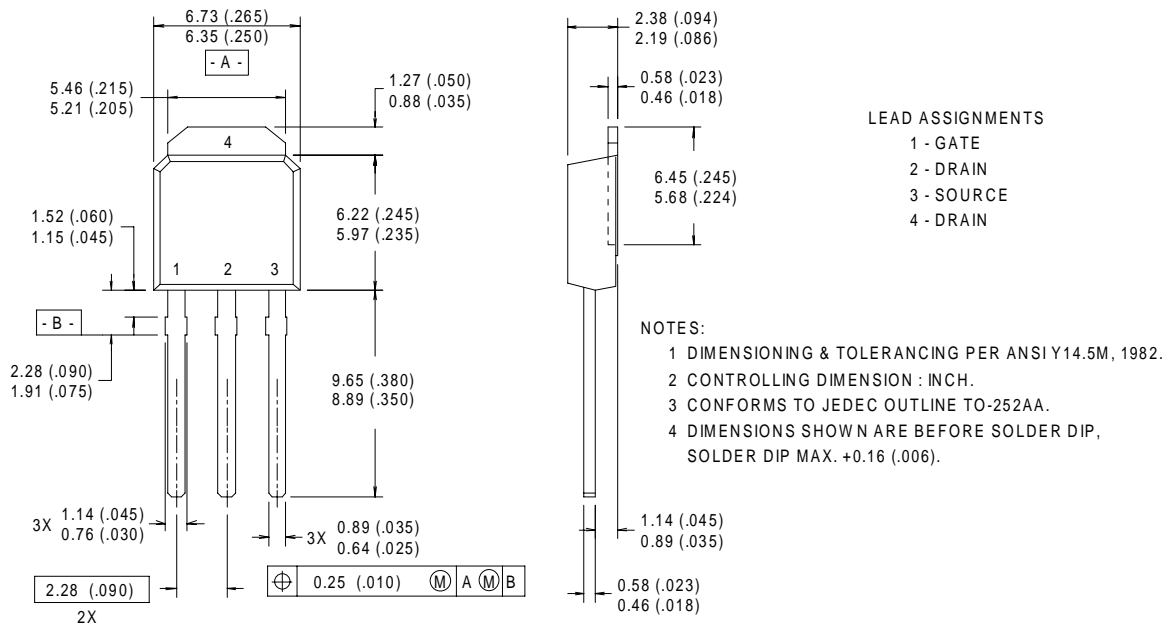
D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



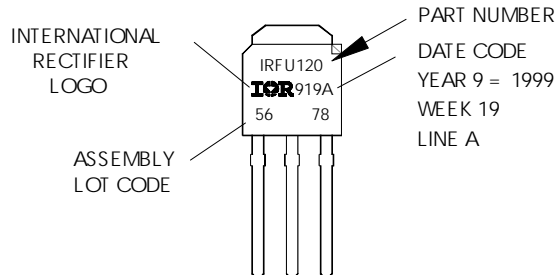
I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
 WITH ASSEMBLY
 LOT CODE 5678
 ASSEMBLED ON WW 19, 1999
 IN THE ASSEMBLY LINE "A"

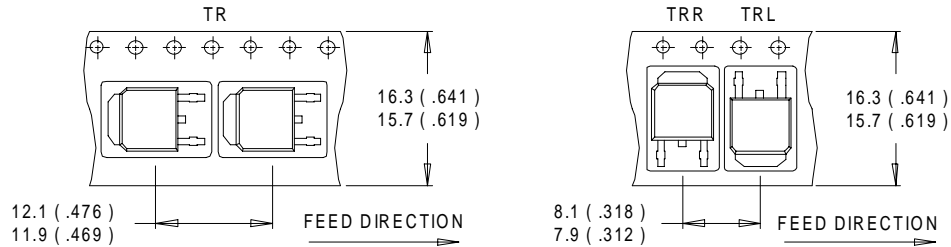


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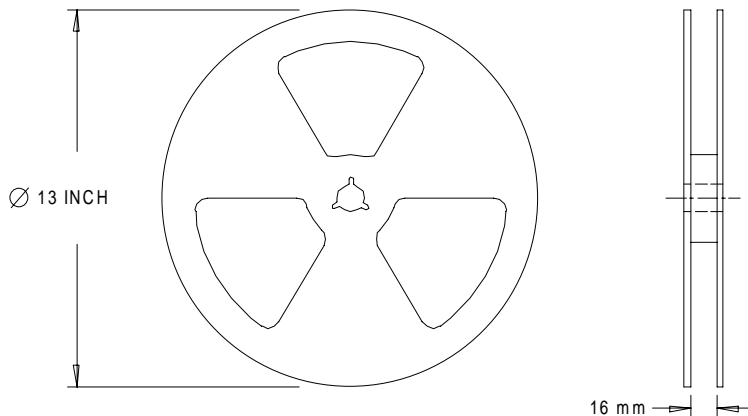
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive [Q101] market.
Qualification Standards can be found on IR's Web site.

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