

**IRFR3518**  
**IRFU3518**

HEXFET® Power MOSFET

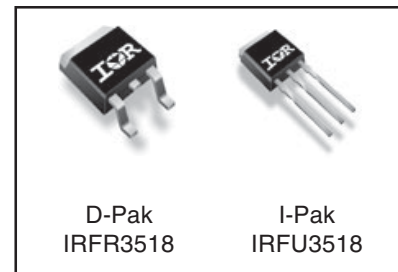
**Applications**

- High frequency DC-DC converters

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on)</sub> max</b>	<b>I<sub>D</sub></b>
<b>80V</b>	<b>29mΩ</b>	<b>30A</b>

**Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C<sub>OSS</sub> to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	<b>Parameter</b>	<b>Max.</b>	<b>Units</b>
V <sub>DS</sub>	Drain-to-Source Voltage	80	V
V <sub>GS</sub>	Gate-to-Source Voltage	± 20	
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	38	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	27	
I <sub>DM</sub>	Pulsed Drain Current ①	150	
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	110	W
	Linear Derating Factor	0.71	W/°C
dv/dt	Peak Diode Recovery dv/dt ②	5.2	V/ns
T <sub>J</sub>	Operating Junction and Storage Temperature Range	-55 to + 175	°C
T <sub>STG</sub>			
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Thermal Resistance**

	<b>Parameter</b>	<b>Typ.</b>	<b>Max.</b>	<b>Units</b>
R <sub>θJC</sub>	Junction-to-Case	—	1.4	°C/W
R <sub>θJA</sub>	Junction-to-Ambient (PCB mount) ③	—	40	
R <sub>θJA</sub>	Junction-to-Ambient	—	110	

Notes ① through ③ are on page 10  
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# IRFR3518/IRFU3518

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## Static @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	80	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.09	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$ ⑥
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	24	29	mΩ	$V_{GS} = 10V, I_D = 18A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	μA	$V_{DS} = 80V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 64V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$

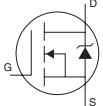
## Dynamic @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$g_{fs}$	Forward Transconductance	34	—	—	S	$V_{DS} = 25V, I_D = 18A$
$Q_g$	Total Gate Charge	—	37	56	nC	$I_D = 18A$ $V_{DS} = 40V$ $V_{GS} = 10V$ ④
$Q_{gs}$	Gate-to-Source Charge	—	11	—		
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	12	—		
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 40V$ $I_D = 18A$ $R_G = 9.1\Omega$ $V_{GS} = 10V$ ④
$t_r$	Rise Time	—	25	—		
$t_{d(off)}$	Turn-Off Delay Time	—	37	—		
$t_f$	Fall Time	—	13	—		
$C_{iss}$	Input Capacitance	—	1710	—	pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 64V, f = 1.0\text{MHz}$ $V_{GS} = 0V, V_{DS} = 0V \text{ to } 64V$ ⑤
$C_{oss}$	Output Capacitance	—	270	—		
$C_{rss}$	Reverse Transfer Capacitance	—	33	—		
$C_{oss}$	Output Capacitance	—	1780	—		
$C_{oss}$	Output Capacitance	—	170	—		
$C_{oss \text{ eff.}}$	Effective Output Capacitance	—	330	—		

## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
$E_{AS}$	Single Pulse Avalanche Energy②	—	160	mJ
$I_{AR}$	Avalanche Current①	—	18	A
$E_{AR}$	Repetitive Avalanche Energy①	—	11	mJ

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	38	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	150		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 18A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	77	—	ns	$T_J = 25^\circ\text{C}, I_F = 18A$
$Q_{rr}$	Reverse Recovery Charge	—	210	—	nC	$di/dt = 100A/\mu s$ ④
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

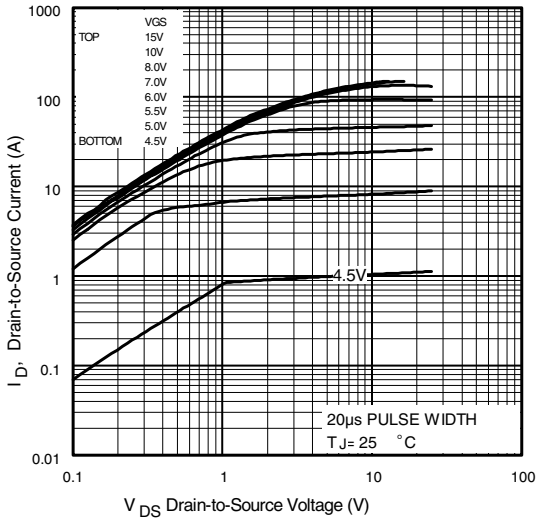


Fig 1. Typical Output Characteristics

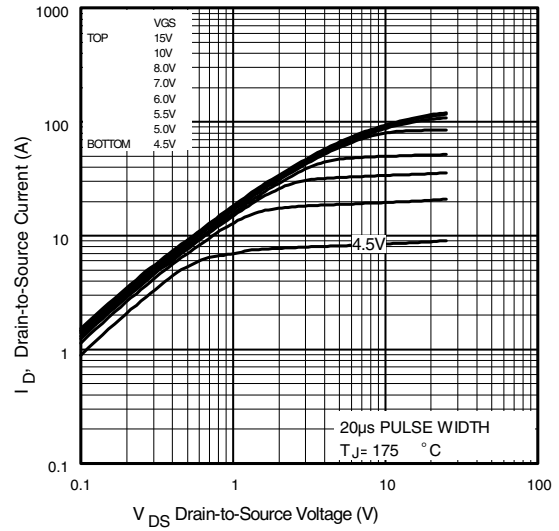


Fig 2. Typical Output Characteristics

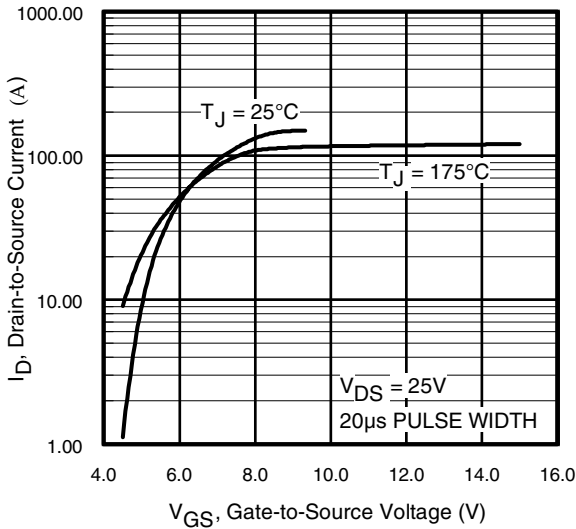


Fig 3. Typical Transfer Characteristics

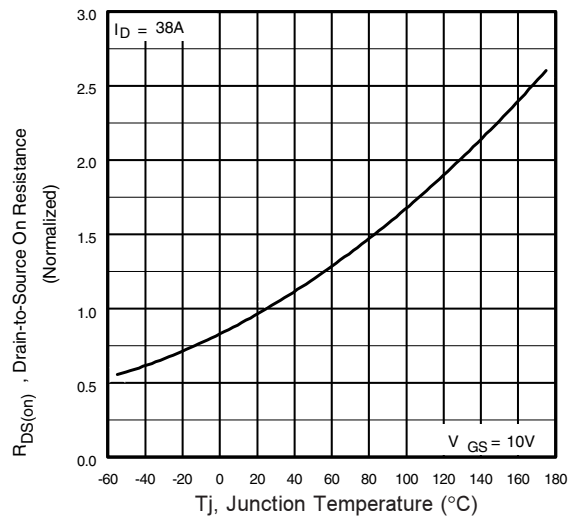
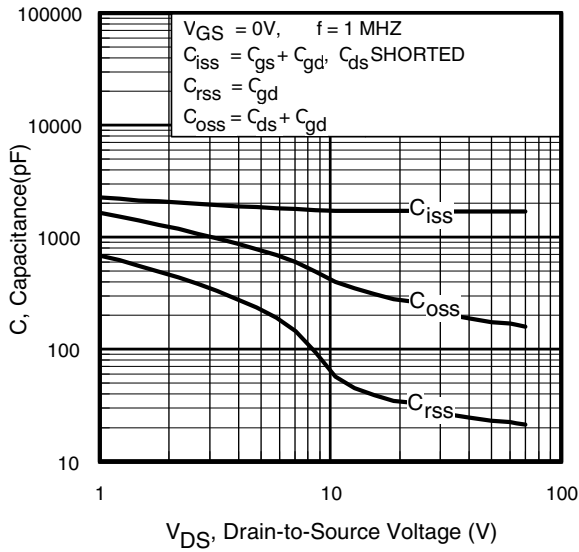


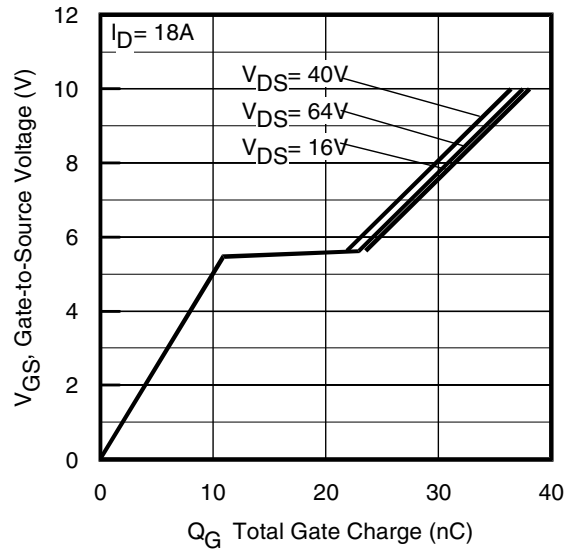
Fig 4. Normalized On-Resistance Vs. Temperature

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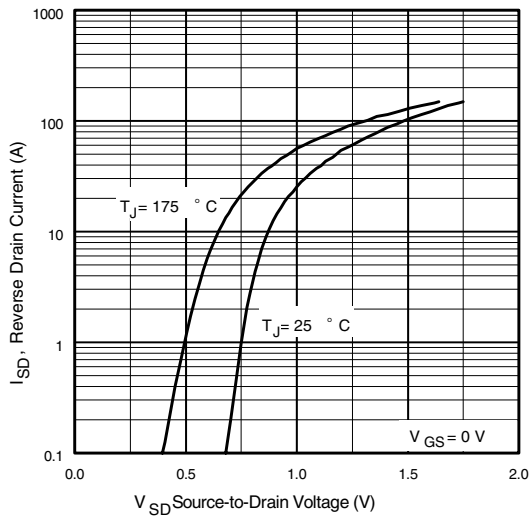
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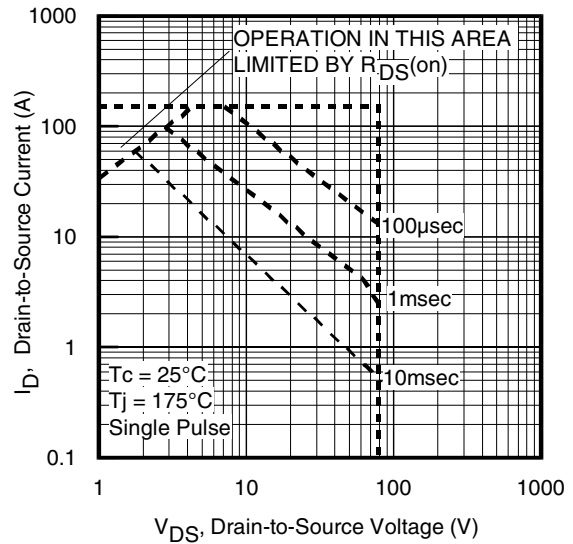
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



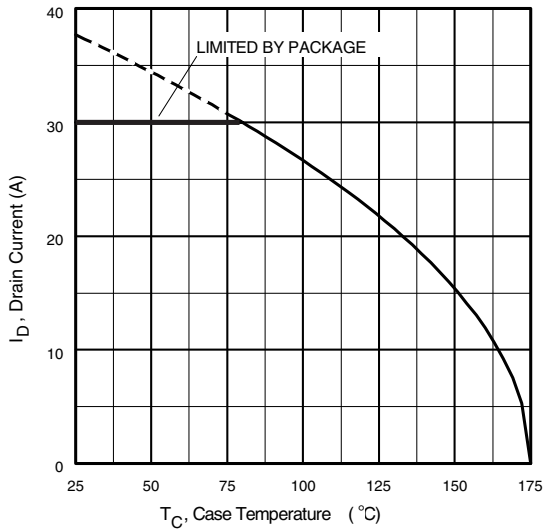
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



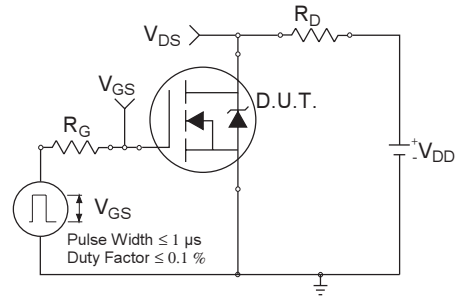
**Fig 7.** Typical Source-Drain Diode Forward Voltage



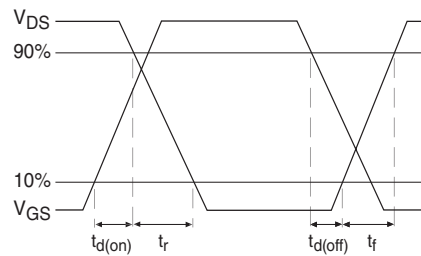
**Fig 8.** Maximum Safe Operating Area



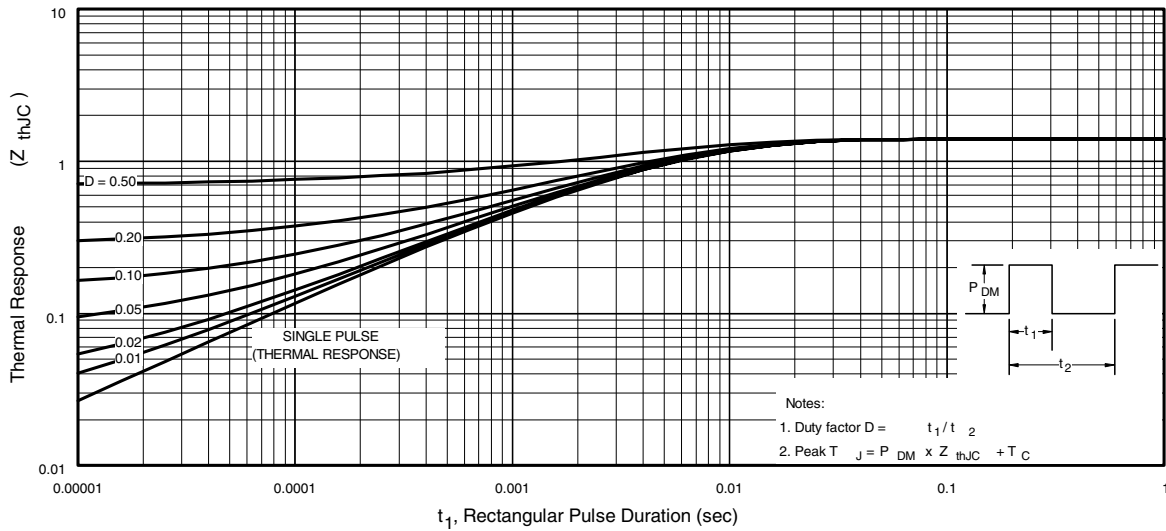
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



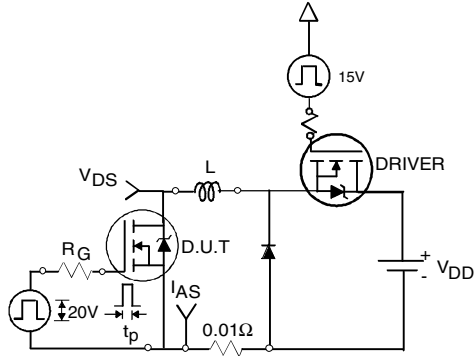
**Fig 10b.** Switching Time Waveforms



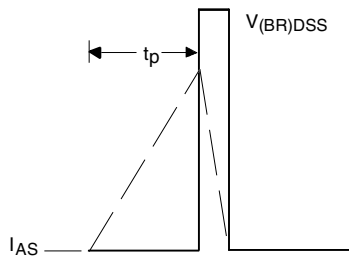
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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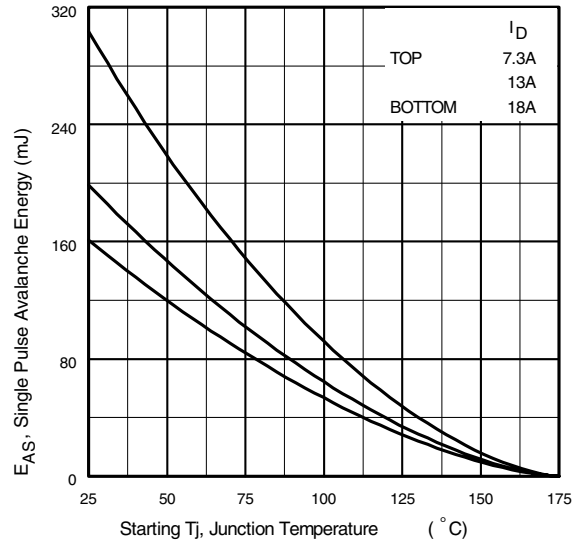
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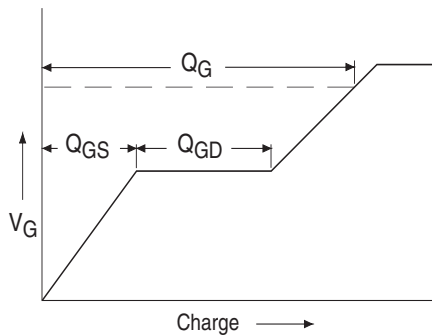
**Fig 12a.** Unclamped Inductive Test Circuit



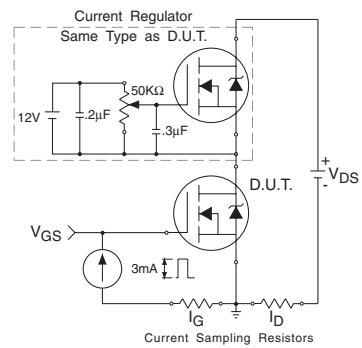
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

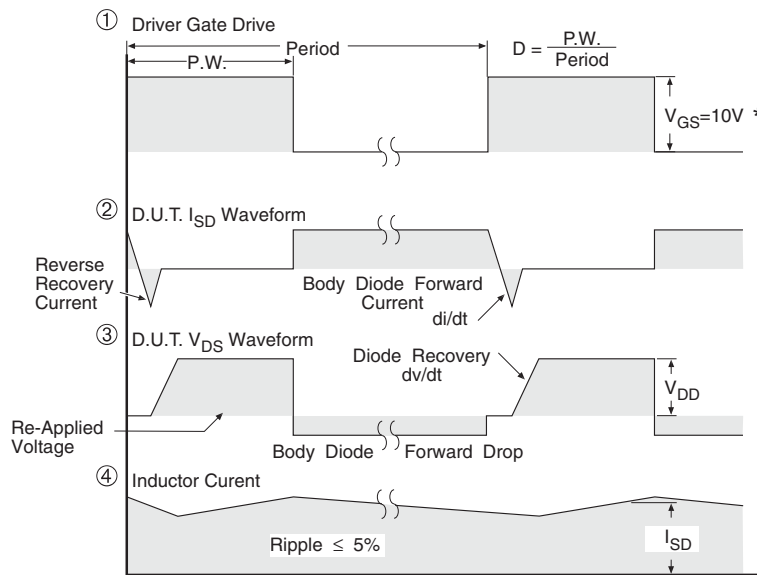
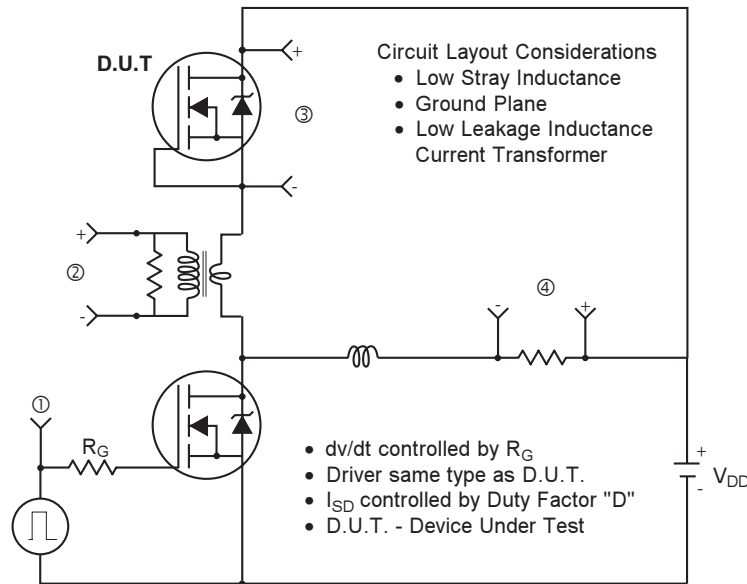


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



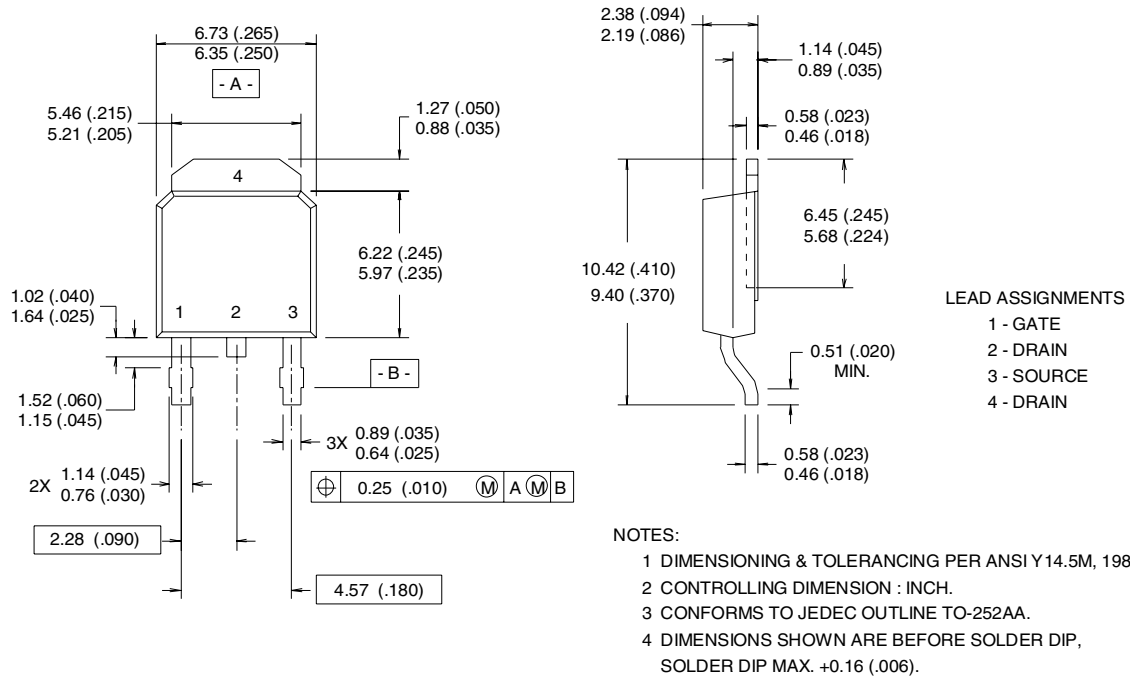
\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

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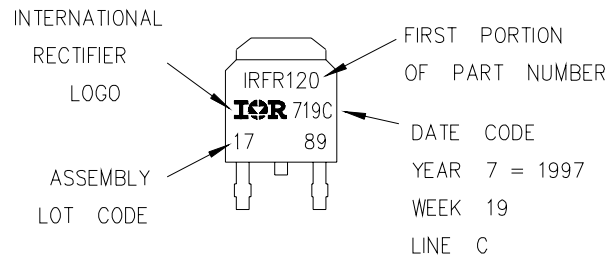
## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



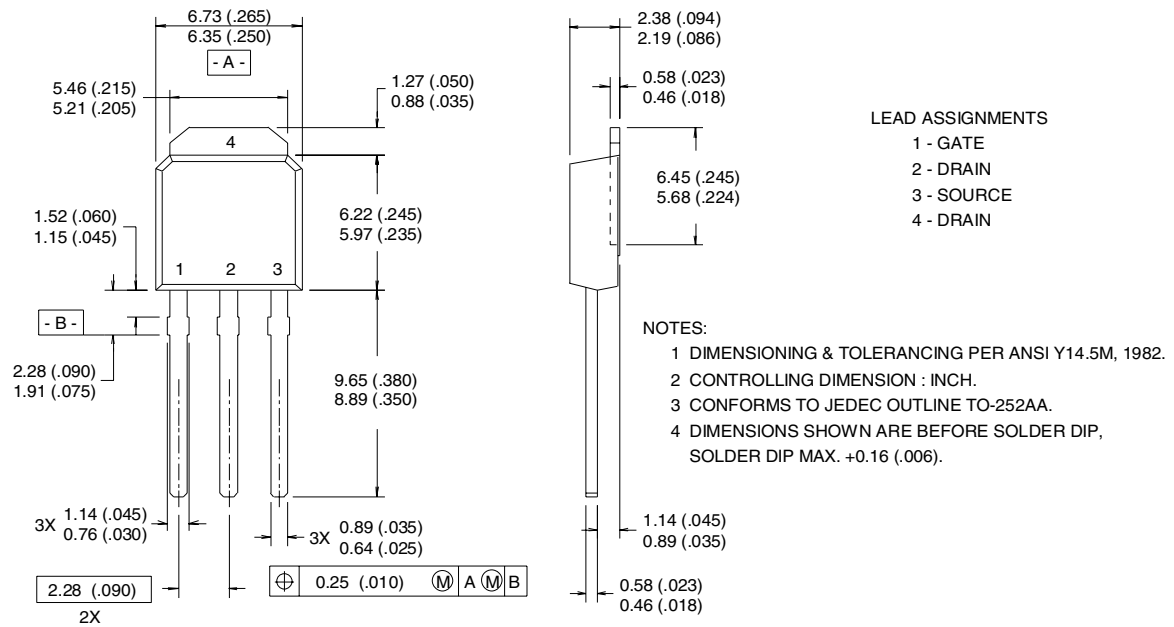
## D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"



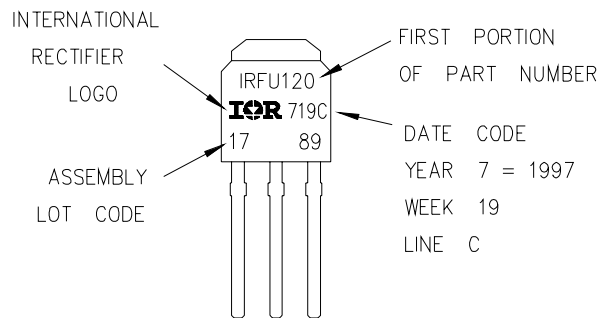
## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



## I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

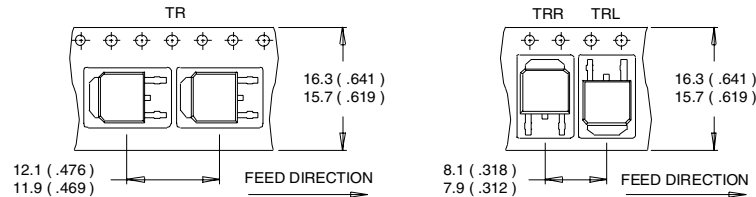


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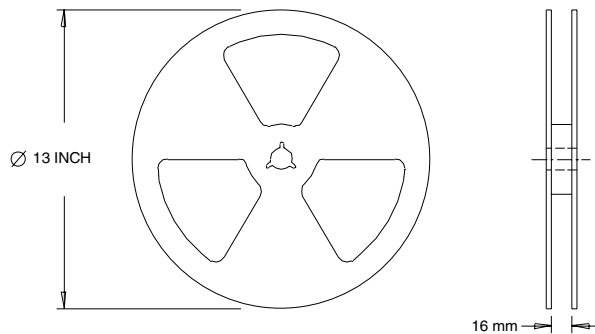
## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)



**NOTES :**

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



**NOTES :**

1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.99\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 18\text{A}$ .
- ③  $I_{SD} \leq 18\text{A}$ ,  $di/dt \leq 360\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$ .
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑥ When mounted on 1" square PCB (FR-4 or G-10 Material).  
For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
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