

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Optimized for SMPS Applications

**Description**

Advanced HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRFZ34VL) is available for low-profile application.

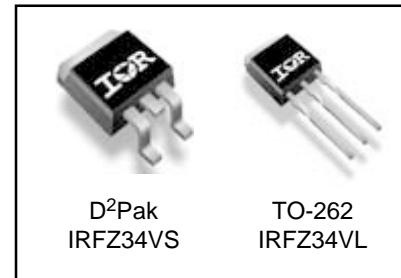
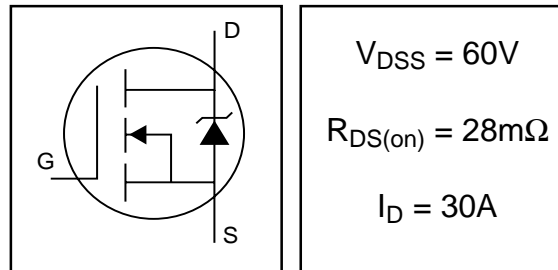
**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}^{\text{⑤}}$	30	A
$I_D @ T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}^{\text{⑤}}$	21	
$I_{DM}$	Pulsed Drain Current ①⑤	120	
$P_D @ T_C = 25^\circ\text{C}$	Power Dissipation	70	W
	Linear Derating Factor	0.46	W/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
$I_{AR}$	Avalanche Current①	30	A
$E_{AR}$	Repetitive Avalanche Energy①	7.0	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	4.5	V/ns
$T_J$	Operating Junction and	-55 to + 175	°C
$T_{STG}$	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case )	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	2.15	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB Mounted)**	—	40	

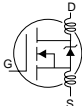
**IRFZ34VS**  
**IRFZ34VL**  
HEXFET® Power MOSFET



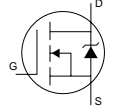
# IRFZ34VS/IRFZ34VL

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IR Rectifier

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	60	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.062	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$ ⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	28	mΩ	$V_{GS} = 10V, I_D = 18A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	15	—	—	S	$V_{DS} = 25V, I_D = 18A$ ④ ⑤
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 60V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 48V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	—	49	nC	$I_D = 30A$
$Q_{gs}$	Gate-to-Source Charge	—	—	12		$V_{DS} = 48V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	18		$V_{GS} = 10V$ , See Fig. 6 and 13 ⑤
$t_{d(on)}$	Turn-On Delay Time	—	10	—	ns	$V_{DD} = 30V$
$t_r$	Rise Time	—	65	—		$I_D = 30A$
$t_{d(off)}$	Turn-Off Delay Time	—	31	—		$R_G = 12\Omega$
$t_f$	Fall Time	—	40	—		$V_{GS} = 10V$ , See Fig. 10 ④ ⑤
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	1120	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	250	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	59	—		$f = 1.0\text{MHz}$ , See Fig. 5 ⑤
$E_{AS}$	Single Pulse Avalanche Energy ② ⑤	—	260	81		mJ

## Source-Drain Ratings and Characteristics

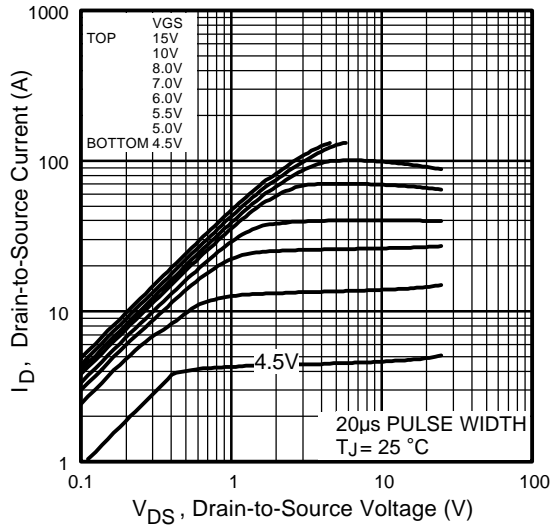
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	30	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	120		
$V_{SD}$	Diode Forward Voltage	—	—	1.6	V	$T_J = 25^\circ\text{C}, I_S = 30A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	70	110	ns	$T_J = 25^\circ\text{C}, I_F = 30A$
$Q_{rr}$	Reverse Recovery Charge	—	99	150	nC	$di/dt = 100A/\mu s$ ④ ⑤
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

### Notes:

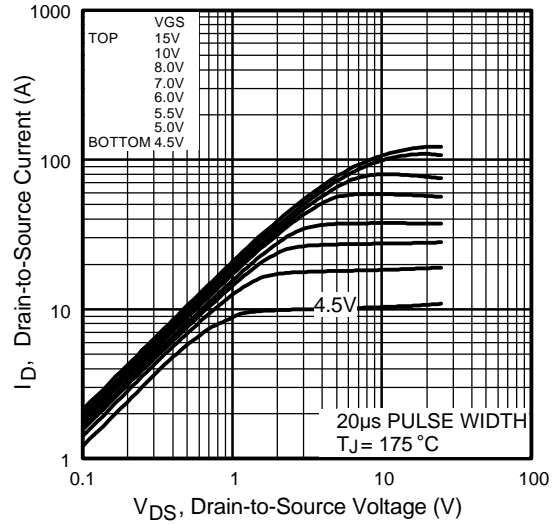
- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )  
 ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 180\mu H$   
 $R_G = 25\Omega$ ,  $I_{AS} = 30A$ . (See Figure 12)  
 ③  $I_{SD} \leq 30A$ ,  $di/dt \leq 250A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$

- ④ Pulse width  $\leq 400\mu s$ ; duty cycle  $\leq 2\%$ .  
 ⑤ Uses IRFZ34V data and test conditions.

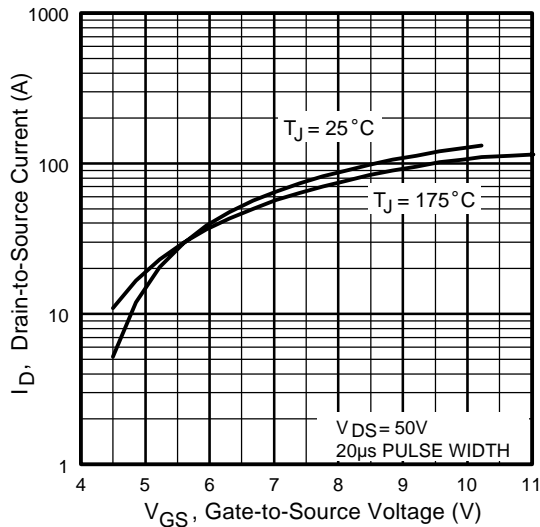
\*\* When mounted on 1" square PCB (FR-4 or G-10 Material ).  
 For recommended footprint and soldering techniques refer to application note #AN-994.



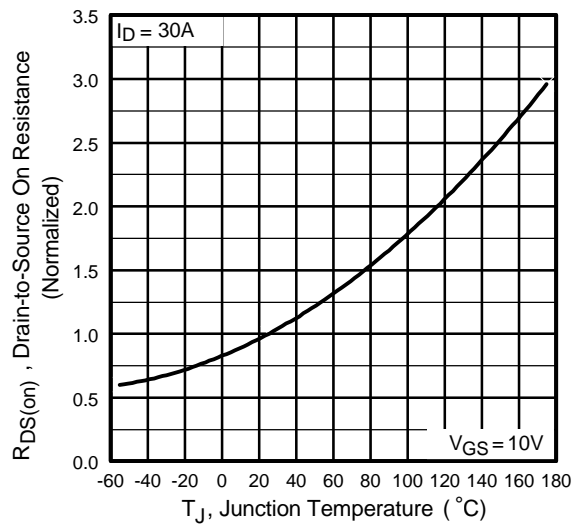
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



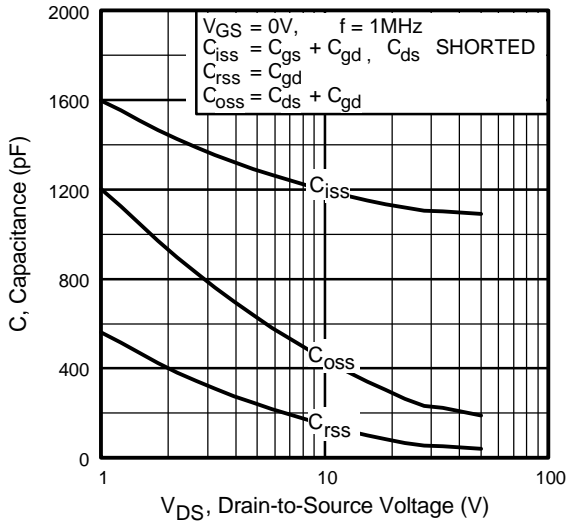
**Fig 3.** Typical Transfer Characteristics



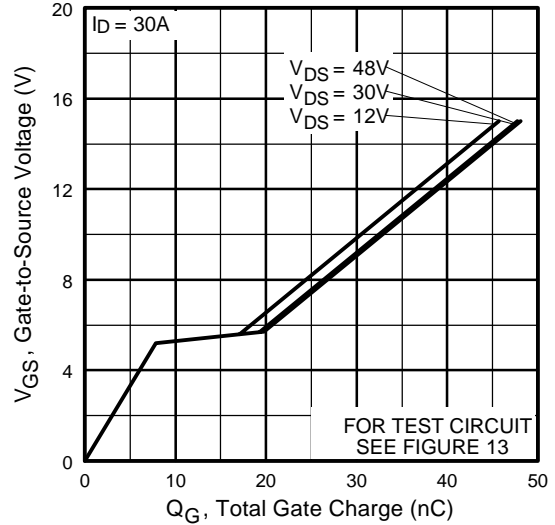
**Fig 4.** Normalized On-Resistance Vs. Temperature

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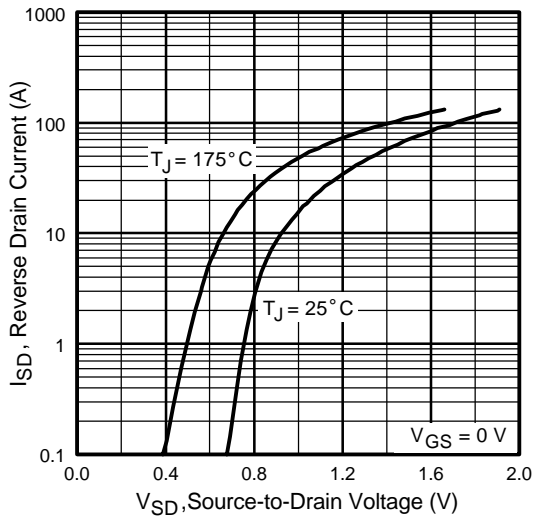
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**IR** Rectifier



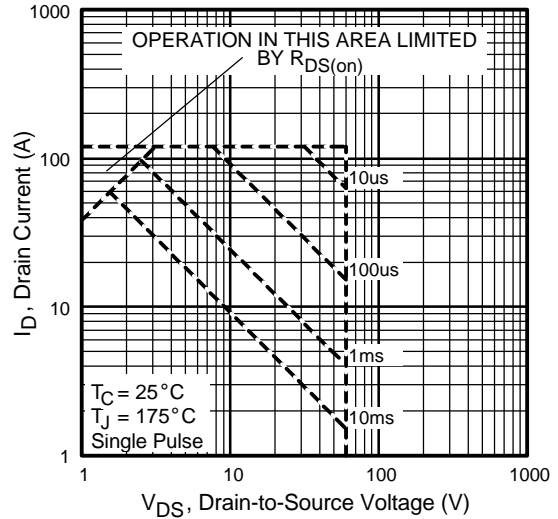
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



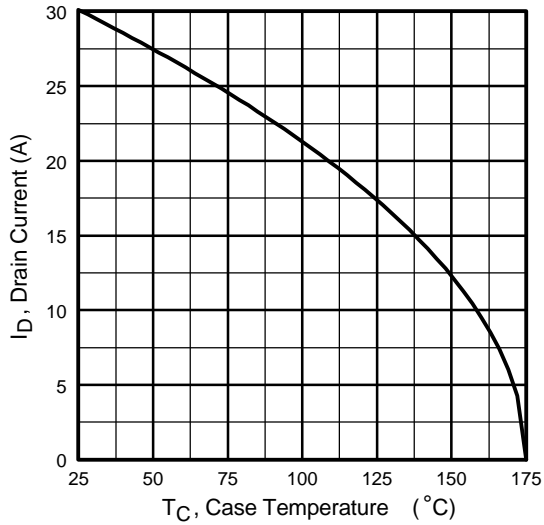
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



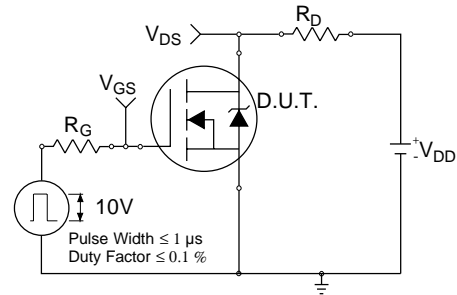
**Fig 7.** Typical Source-Drain Diode Forward Voltage



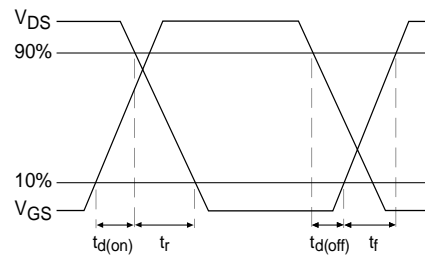
**Fig 8.** Maximum Safe Operating Area



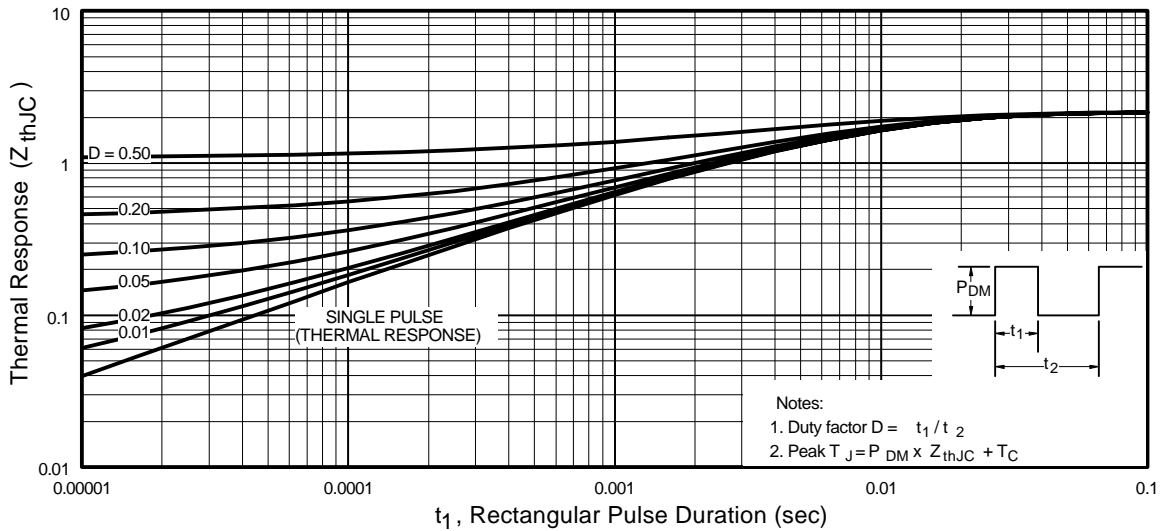
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



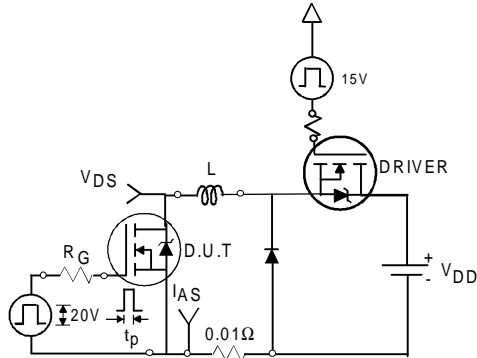
**Fig 10b.** Switching Time Waveforms



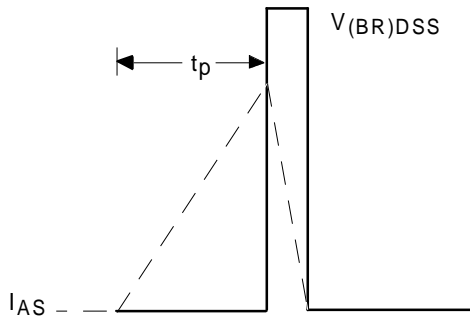
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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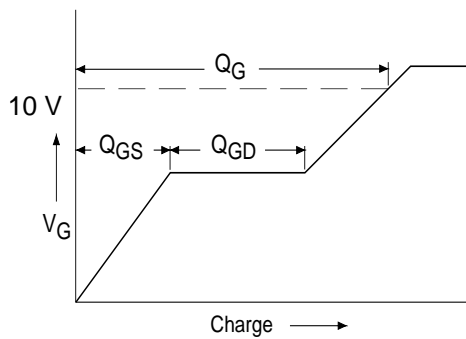
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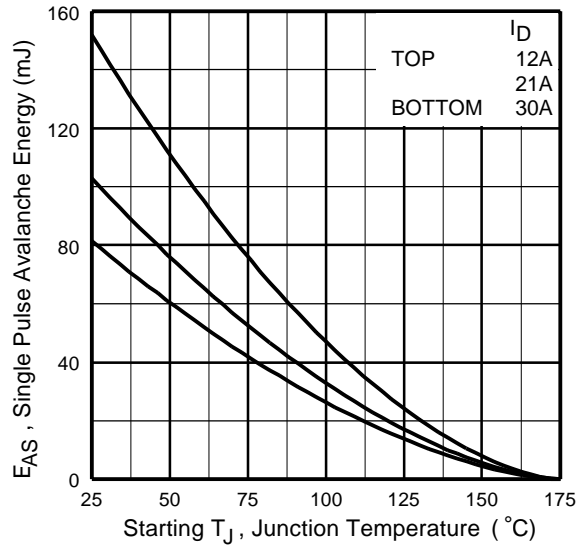
**Fig 12a.** Unclamped Inductive Test Circuit



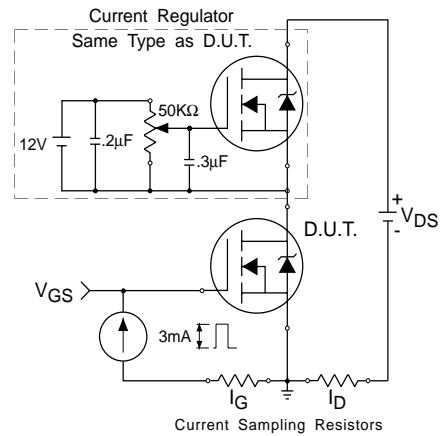
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform

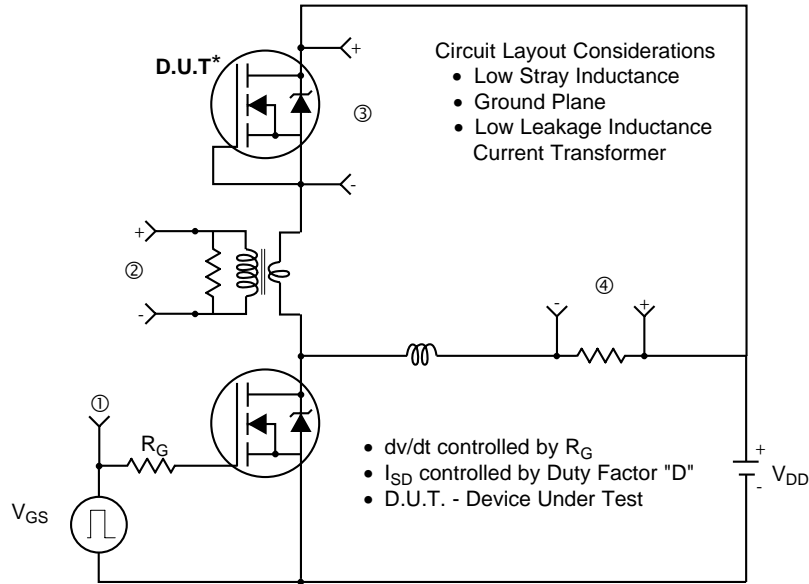


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

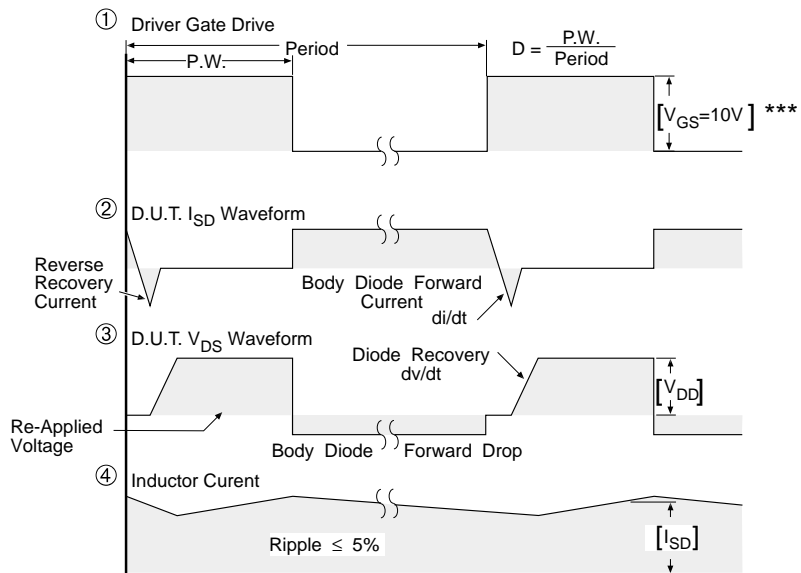


**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity of D.U.T for P-Channel



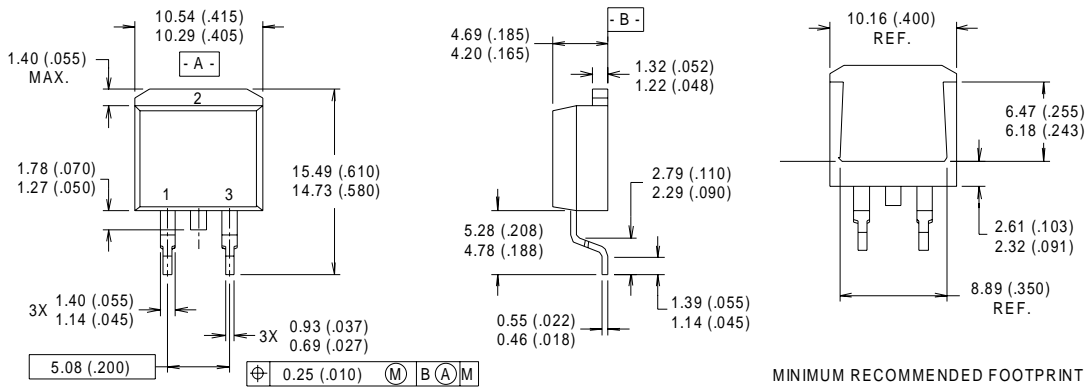
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and 3V Drive Devices

**Fig 14.** For N-channel HEXFET<sup>®</sup> power MOSFETs

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## D<sup>2</sup>Pak Package Outline



**NOTES:**

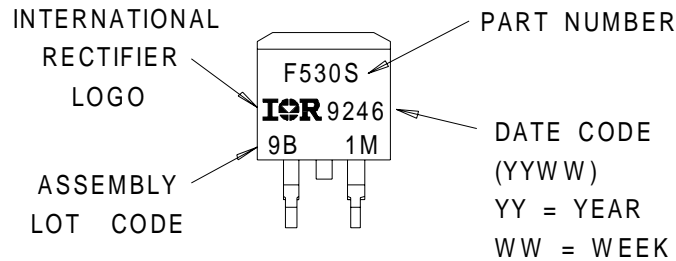
- 1 DIMENSIONS AFTER SOLDER DIP.
- 2 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
- 3 CONTROLLING DIMENSION : INCH.
- 4 HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

**LEAD ASSIGNMENTS**

- 1 - GATE
- 2 - DRAIN
- 3 - SOURCE

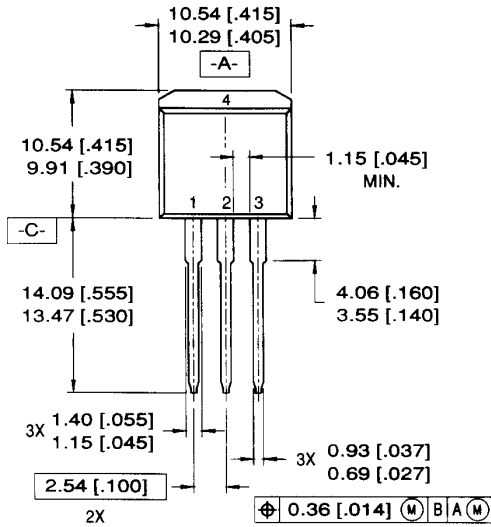
## Part Marking Information

**D<sup>2</sup>Pak**



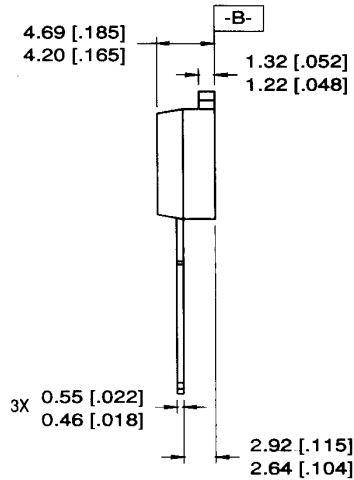
## Package Outline

TO-262 Outline



**LEAD ASSIGNMENTS**

- |           |            |
|-----------|------------|
| 1 = GATE  | 3 = SOURCE |
| 2 = DRAIN | 4 = DRAIN  |



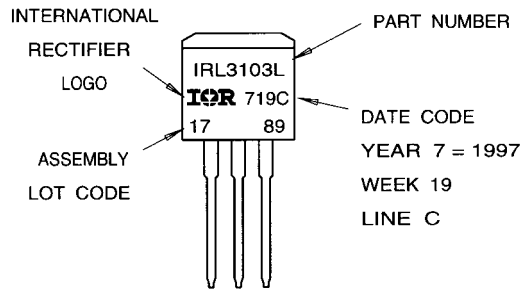
**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

## Part Marking Information

TO-262

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"

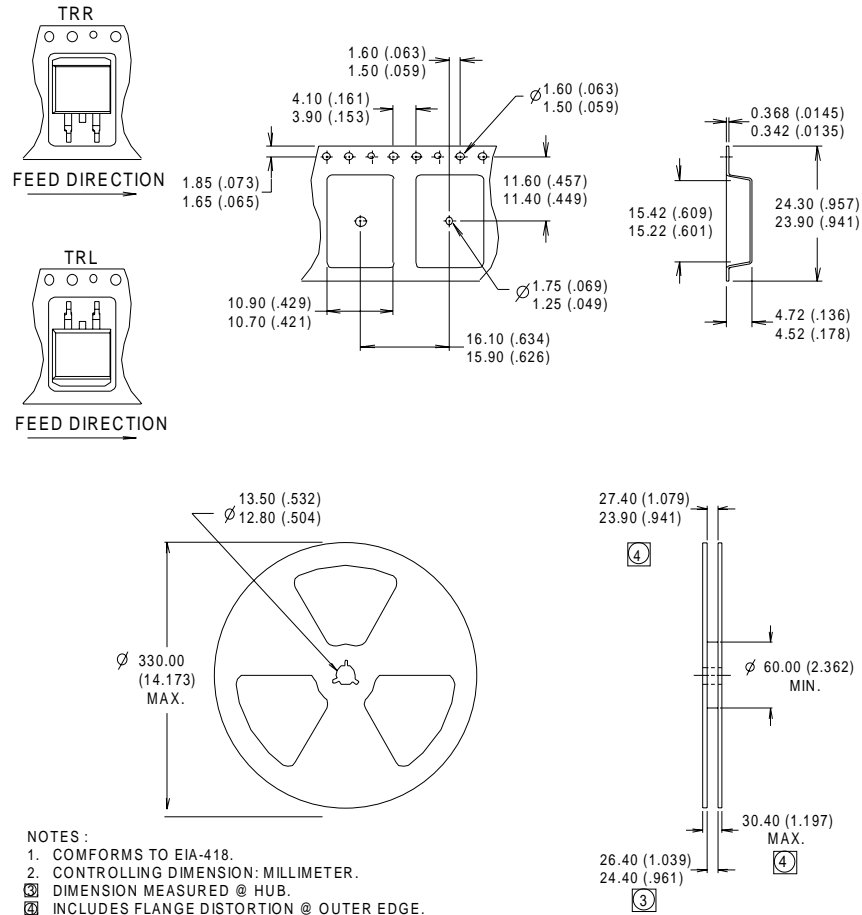


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## Tape & Reel Information

### D<sup>2</sup>Pak



Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

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**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
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